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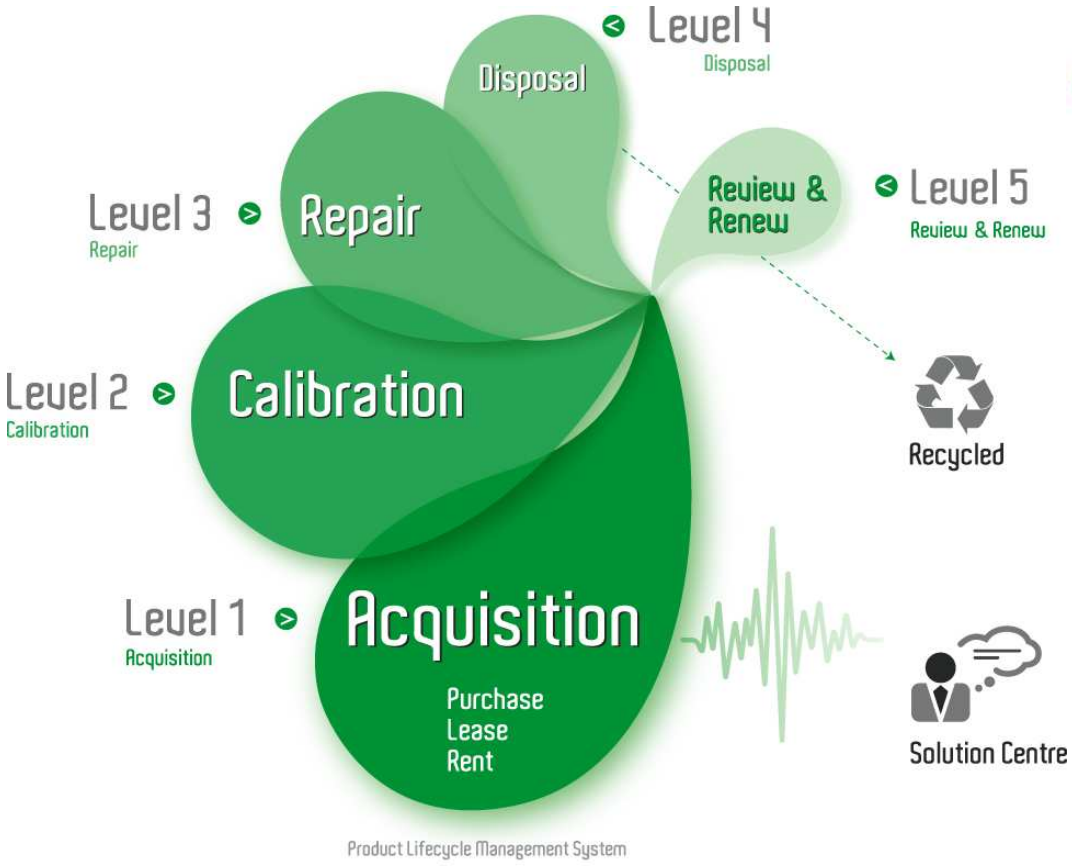

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User Manual

Tektronix

Tektronix Logic Analyzer Family
Version 4.2 Software

071-0863-02

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Preface

This manual contains operating information for the Tektronix Logic Analyzer family. The manual consists of the following sections:

- *Getting Started.* Provides basic information about installing and using the logic analyzer.
- *Operating Basics.* Provides an overview of the logic analyzer connectors, introduces you to the logic analyzer and pattern generator windows, and explains the basic operation of the Tektronix Logic Analyzer.
- *Reference.* Provides detailed information of the logic analyzer. This section is divided according to the window types.
- *Appendix A: Specifications.* Lists the environmental, physical, and electrical properties of the logic analyzer family.
- *Appendix B: TLA700 Symbol File Format.* Provides information about the contents of symbol files using the TLA700 Symbol File format.
- *Appendix C: PG Physical-Logical Conversion*. Provides information on using signals between the LA module, DSO module, and the PG module.
- *Appendix D: TLA700 Module Installation.* Provides installation instructions for logic analyzer modules. Refer to this appendix if you need to install modules in the TLA700 mainframes.
- *Appendix E: Merging Modules.* Provides instructions for merging modules to create wider mainframes for specific applications.
- *Appendix F: Power Cord and Line Fuse Requirements for the Benchtop and Expansion Mainframes.* Provides information on the power and fuse requirements for the benchtop and expansion mainframes.
- *Appendix G: Installing Software.* Provides instructions for reinstalling the system and application software and firmware.
- *Appendix H: User Service.* Provides user service information.

Related Documentation

In addition to this user manual, the following documentation is available for your Tektronix logic analyzer:

- The online help provides information about the user interface, the TLA700 Programmatic Interface (TPI), and the TLAScript interface. To view the online help, select Help Topics from the Help menu. The TLAScript online help provides links to related topics in TPI.
- The TLA7PG2 online help provides information about the pattern generator user interface and the Pattern Generator Programmatic Interface (PPI). To view the online help, select Help Topics from the Help menu in the TLA7PG2 application.
- The online release notes provide last-minute product and software information not included in this manual. Refer to *Release Notes* on page 1–33 for information on viewing the release notes.
- A series of microprocessor support instruction manuals provide operating and service instructions for the individual microprocessor support packages.
- The *TLA7QS QuickStart Training Manual* provides training exercises to help you learn key features of the logic analyzer. The training manual is designed to be used with the TLA7QS QuickStart training board.
- A series of service manuals provide board-level service information for the logic analyzer modules and mainframes.
- A series of probe manuals provide detailed instructions for using individual logic analyzer and pattern generator probes.
- A series of probe labeling instructions provide detailed instructions for labeling the P6810, P6860, and P6880 logic analyzer probes.

Terms Used in this Manual

The following terms are used throughout this manual. Refer to the *Glossary* for information on other logic analyzer terminology.

- **LA Module.** An abbreviation and generic term for the logic analyzer module.
- **DSO Module.** An abbreviation and generic term for the oscilloscope module.
- **PG Module.** An abbreviation and generic term for the pattern generator module.

What's New in This Manual

The Tektronix Logic Analyzer family consists of the TLA600 and TLA700 series logic analyzers, and all of the accessories and supports that can be used with them. This manual includes information on product enhancements, new features, and information on using these to improve your instrument performance and reliability. Specifically, this manual has been updated to include information on the new TLA7Axx logic analyzer modules for the TLA700 series, which have:

- **8 GHz MagniVu Timing acquisition**. You now have 8 GHz MagniVu timing acquisition available on all channels with 16 Kb memory depth per channel. You can view any channel with 125 ps timing resolution to verify digital signal timing. Additional capabilities include adjustable sample rate (125 ps to 1 ns), movable trigger position, and a separate MagniVu trigger action that can be triggered independent of the main module trigger. Minimum detectable pulse widths of 750 ps can be acquired and triggered upon using the MagniVu acquisition technology.
- **2 GHz deep Transitional Timing acquisition**. To capture elusive digital signal timing problems over long time spans, 2 GHz deep time acquisition is available with up to 256 MB memory depth on quarter-channels. 1 GHz deep timing is available on half-channels and 500 MHz deep timing is provided on all channels. Transitional storage is used to only store when data changes and is timestamped with 125 ps resolution.
- **120 to 800 MHz State acquisition**. To enable tracing data flow and program execution of processors and buses 120 to 800 MHz state acquisition is now available. Three state acquisition speeds are provided: 120 MHz (standard), 235 MHz (optional) and 450 MHz (optional) to fit a wide range of processor and bus applications. A comprehensive set of clocking capabilities provide the means to work with virtually any processor or bus including support for high-speed data rates. Plus, advanced support is provided for source synchronous buses to simplify setup and acquisition. A setup/hold window of 650 ps provides accurate data capture from the fastest processors and busses. The window is adjustable in 125 ps increments within a range from +16 ns to –8 ns.
- **Triggering**. Enhancements include a trigger state machine that operates at a 2 ns rate with trigger resources that include 16 states, 16 words/4 range recognizers, two 51-bit counter/timers and 16 transition (edge) recognizers. A key benefit of the MagniVu acquisition technology is that it provides a 500 ps glitch recognizer and a 250 ps setup/hold violation both with 125 ps resolution up to a 16 ns window. A comprehensive set of trigger actions including storage control and sequence actions is also provided. Additional triggering enhancements include a decrement counter function, a force prefill function (used to ensure that memory is fulled before looking for the trigger)

and a Snapshot Recognizer. In the External 2X/4X modes, events up to the maximum data rate of 1.25 Gb/s can be used for triggering.

- **128 KB to 64 MB Memory Depth**. Increased memory depth enables triggering on the symptom of a problem and capturing the cause when they are widely separated in time. Memory depth configurations of 128 KB, 512 KB, 2 MB, 8 MB, and 64 MB are available. Another benefit of the MagniVu acquisition technology is the separate 51-bit, 125 ps resolution time stamp memory that provides automatic and accurate time-correlation over a 3.25 day duration with data from any other module with a typical correlation accuracy of 2 ns.
- **2.0 GHz Analog Multiplexer**. Routes the analog signal of any four logic analyzer channels to either an internal or external DSO, eliminating the need to double-probe signals. Using iView, data from an external DSO can be correlated on the TLA display to quickly track down elusive digital signal quality problems.
- **Low-Capacitance, Connectorless Smart Probing System**. This system combines analog and digital measurements through a single probe connection, providing immediate analog measurements access to all digital signals. Both high-density and general-purpose probes are available and feature an ultra-low 0.7 pF (1.0 pF for GP probes in group configuration) and 1.0 pF total probe input capacitance, respectively. Single-ended and differential logic signals are supported as well. Each probe is a smart probe that, once calibrated, maintains its own individual calibration constraints (deskew, input resistance, and gain/offset) in the probe's internal NVRAM. When plugged into the new TLA7Axx logic analyzer module, the probe calibration constants are loaded and used to provide more accurate measurements.
- **5-Way Module Merging**. This increases the maximum channel count to 680 channels on a single timebase with no tradeoff in performance, thereby allowing the TLA7Axx to be used for the deepest and widest applications. For state applications, you can get up to 340 channels at 128 M depth, at 800 MHz (External 2X) or 170 channels at 258 M depth, at 625 MHz clock/1.25 Gb/s data (External 4X). For deep transitional timing applications, you can get up to 340 channels at 128 M depth, at 1 GHz (Internal 2X) or 170 channels at 256 M depth, at 2 GHz (Internal 4X).
- **Calibration Fixture**. The TLACAL2 calibration fixture provides you with the tools to keep your new TLA7Axx logic analyzer module operating at maximum performance for the most accurate measurements. It also provides you with performance verification and adjustment procedures, including traceable calibration.
- **New CD-RW Drive**. All new TLA60x/61x/62x instruments and TLA715/721 mainframes now come standard with a CD-RW drive that allows you to back up and transport your large setup and data files.

- **iView Integrated View of Your TDS Data on Your TLA Display**. Introduced as part of Version 4.1 TLA Application Software, iView has now been enhanced to include support for the TDS3000/3000B, TDS5000, TDS6000, TDS7000, CSA7000 TDS600C and TDS700 Series oscilloscopes.
- **EasyTrigger**. Introduced as part of Version 4.1 of the TLA Application Software, EasyTrigger has now been enhanced to include support for the TLA7Axx logic analyzer module and its new triggering capabilities. Examples include snapshot recognizer, demux 2X/4X, decrement counter, 16 transition (edge) recognizers and independent MagniVu trigger.
- **Version 4.2 TLA Application Software**. Newest version of TLA600/700 application software has been enhanced to support the TLA7Axx logic analyzer module and requires Windows 2000 Professional (Windows 2000 Service Pack 2 is now standard). Your existing TLA60x/61x/62x instrument or TLA715/721 mainframe can easily be upgraded to Version 4.2 with the appropriate TLA6UP or TLA7UP Field Upgrade Kits. All existing TLA setup and data files are fully forward-compatible with Version 4.2 TLA application software. Version 1.3 of the PatGen Application software and PatGenVu are also included.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 6:00 a.m. - 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

The Tektronix Logic Analyzer family consists of the TLA600 and TLA700 series logic analyzers, and all of the accessories and supports that can be used with them. For more information about availability, contact your Tektronix representative and view the Tektronix website at: www.tektronix.com.

TLA600 Series Logic Analyzers

The TLA600 logic analyzers are a high-performance line of logic analyzers. There are two basic styles: one contains an internal display, and the other uses an external display as shown in Figure 1–1. The TLA600 logic analyzers offer a variety of channel widths and memory depths.

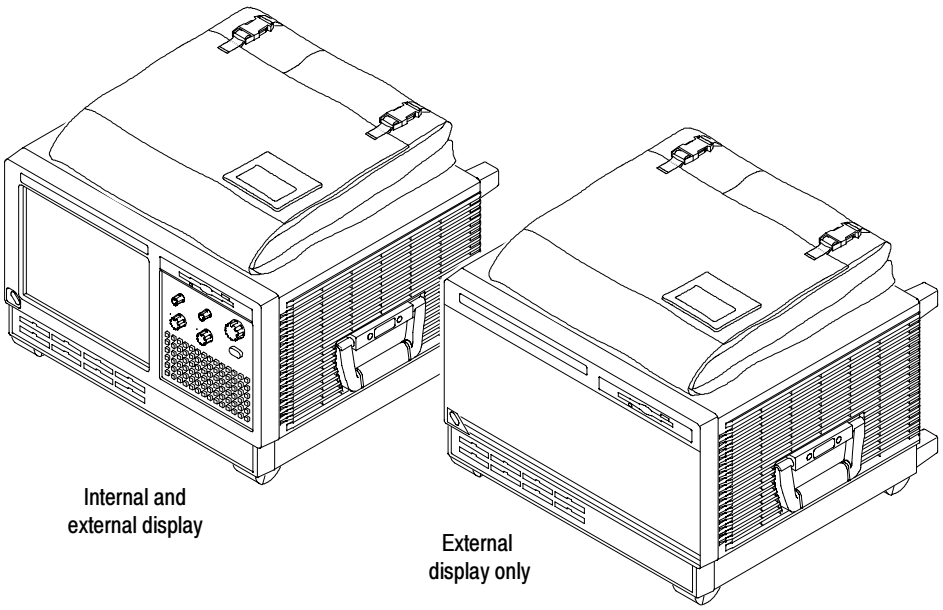


Figure 1-1: TLA600 series logic analyzers

MagniVu is an acquisition technology that provides up to 1000 picosecond timing resolution on all channels and requires no additional probing.

TLA700 Series Logic Analyzers

The TLA700 series logic analyzers combine a high-performance logic analyzer module with an optional digitizing storage oscilloscope (DSO) module and pattern generator module.

There are two styles of mainframes: portable and benchtop. Each mainframe can also include an expansion mainframe that looks similar to the benchtop mainframe and is compatible with both the portable and benchtop mainframes. The portable mainframe and the benchtop mainframe are shown in Figure 1–2 and Figure 1–3.

Several logic analyzer modules are available in various combinations of channel width and memory depth. All of the logic analyzer modules provide simultaneous state and timing measurements through a single probe.

MagniVu, an acquisition technology enabled by the logic analyzers, provides a sampling rate of 500 ps on TLA7Lx/Mx/Px/Qx modules and 125 ps on TLA7Axx modules on all channels without additional probing.

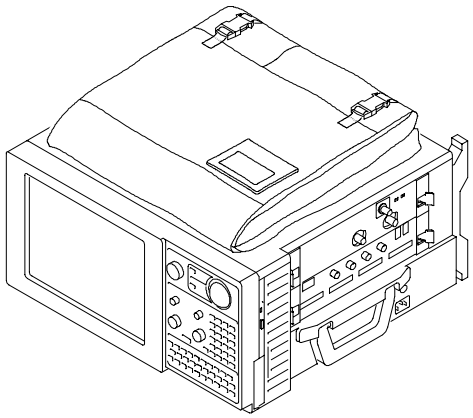


Figure 1-2: TLA700 portable mainframe

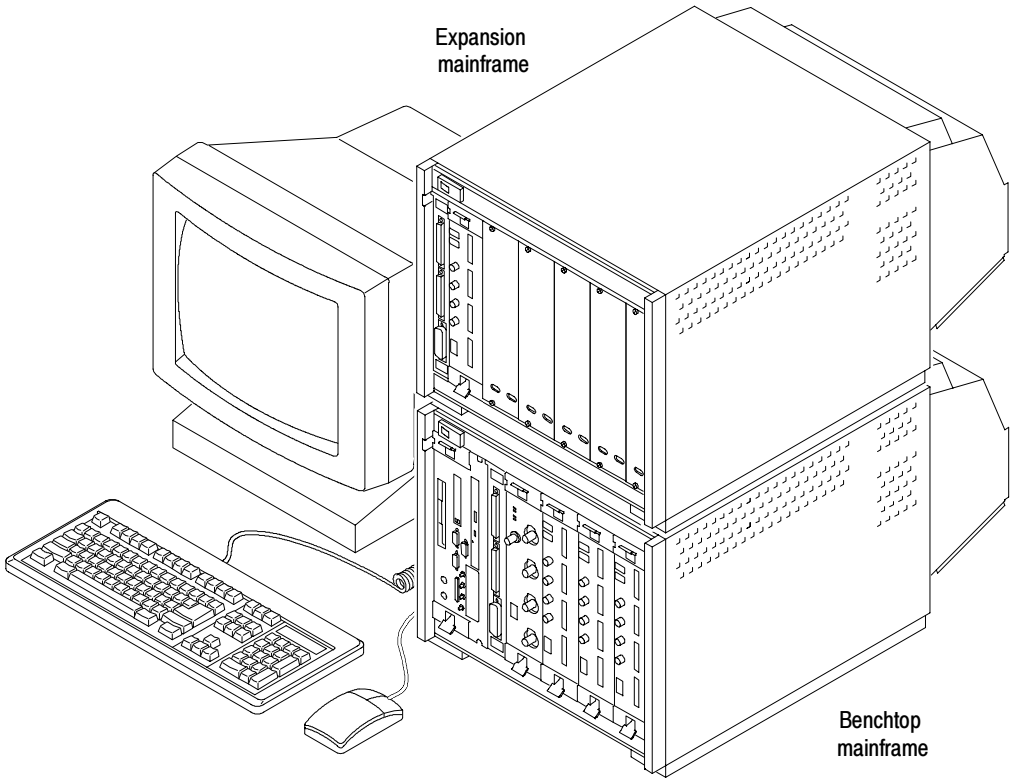


Figure 1-3: TLA700 benchtop mainframe with an expansion mainframe

The DSO module enables digital real-time signal acquisition. Data acquired using this module is time correlated with data from other modules for displays and intermodule triggering and signalling.

The pattern generator module provides multi-channel signals for use in applications such as simulation of missing system elements, erroneous signals for stress testing, and extended analysis for stimulating a device under test.

The Windows operating system allows you to install any PC-compatible, third-party hardware and software on the instrument.

Accessories

For a complete list of accessories, refer to the online help. Select the Contents tab and click the Standard and Optional Accessories icon. Then select one of the topics for more information.

Installation

This section describes the steps needed to install your Tektronix logic analyzer.

Check the Shipping List

Verify that you have received all of the parts of your logic analyzer using the shipping list. You should also verify the following:

- Verify that you have the correct power cords for your geographical area.
- Verify that you have backup copies of the installed software. Store the backup software in a safe location where you can easily retrieve the software for maintenance purposes.
- Verify that you have the correct probes and adapters (and modules if you have a TLA700 series logic analyzer).
- Verify that you have all the standard and optional accessories that you ordered.

***NOTE**. Keep the software packaging available because you will need it to enter the Windows software registration number when you first turn on the logic analyzer.*

- Fill out and return the customer registration card that is packaged with this manual.

Site Considerations

Read this section before installing the logic analyzer. This section describes site considerations, power requirements, and ground connections for your logic analyzer.

***CAUTION.** Allow a two inch (5.1 cm) clearance at the bottom and sides of the instrument to ensure proper cooling.*

TLA600 and TLA714/715 Logic Analyzers. You can use the TLA600 and TLA715 logic analyzers on a bench or on a cart in the normal position (on the bottom feet).

You can also use the logic analyzer while it rests on the rear feet. If you use the instrument while it is resting on the rear feet, make sure that you properly route any cables connected to the rear of the instrument to avoid damaging them.

TLA720/721 Benchtop and TLA7XM Expansion Mainframes. The benchtop and expansion mainframes are designed to operate on a bench or in a rackmount environment.

WARNING. *To avoid personal injury, do not stack more then one expansion mainframe on top of a benchtop mainframe or another expansion mainframe. Always use a rackmount kit to ensure that the expansion mainframes are secure and will not fall.*

If you need to stack more than two benchtop and expansion mainframes, install the mainframes in a rack. Rackmount kits are available from third-party vendors. Please refer to the online help under Standard and Optional Accessories for rackmount kit part numbers.

WARNING. *To avoid personal injury, never lift or move a benchtop or expansion mainframe by yourself. The size and weight of these mainframes requires two people to lift or move them.*

Installing Expansion Mainframes

This section describes how to install a TLA7XM expansion mainframe. If your logic analyzer does not contain any expansion mainframes, you can skip this section. Observe the following guidelines when installing expansion mainframes:

- Do not stack more than one mainframe on top of another mainframe without a rackmount kit.
- The expansion module must be installed in slot 0 of the expansion mainframe.

CAUTION. *Verify that all mainframes are powered off before continuing the installation procedure. If you are installing more than two expansion mainframes, always use a rackmount kit. Contact your local Tektronix representative for information on site considerations for multiple mainframes.*

Installing in a benchtop Mainframe

The expansion module can be installed in any slot of the benchtop mainframe except 0 through 2, which are reserved for the benchtop controller module. If you are only installing one expansion mainframe, you can install the expansion module in slot 12 to keep the expansion cables out of your way.

If you are installing two expansion mainframes, consider installing the two expansion modules next to the benchtop controller module to maximize the number of open slots as shown in Figure 1–5 on page 1–7.

You can configure up to four expansion mainframes with the portable mainframe and up to ten expansion mainframes with a benchtop mainframe.

To install the expansion module:

1. If the expansion module is not already installed in slot 0 of your expansion mainframe, install it now (refer to *Appendix D: TLA700 Module Installation* for detailed module installation instructions).

CAUTION. *To avoid damaging the chassis, do not use the retaining screws to seat the expansion module. These screws are intended for securing the module and reinforcing the grounding.*

2. Manually seat the expansion module by pressing it into place.
3. Use a screwdriver to tighten the retaining screws (maximum of 2.5 in-lbs).

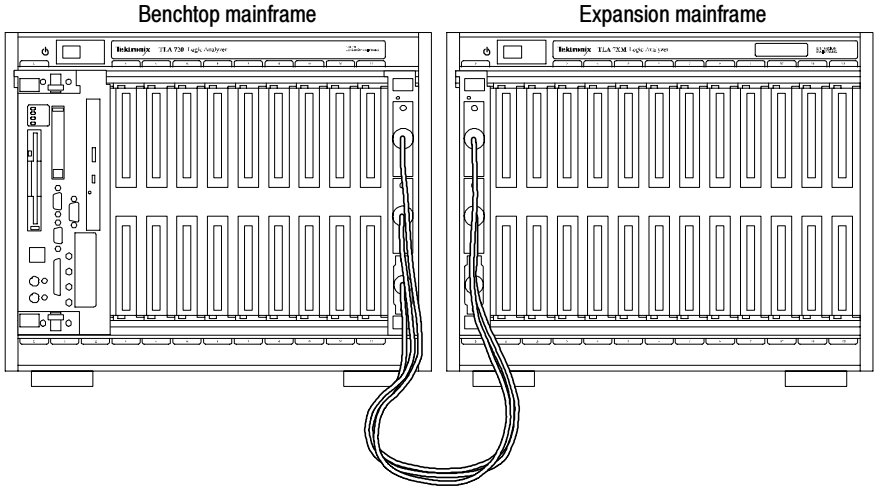


Figure 1-4: Benchtop mainframe and one expansion mainframe

4. Place the EXPANSION 1 label in the outlined area on the upper right side of the expansion mainframe.

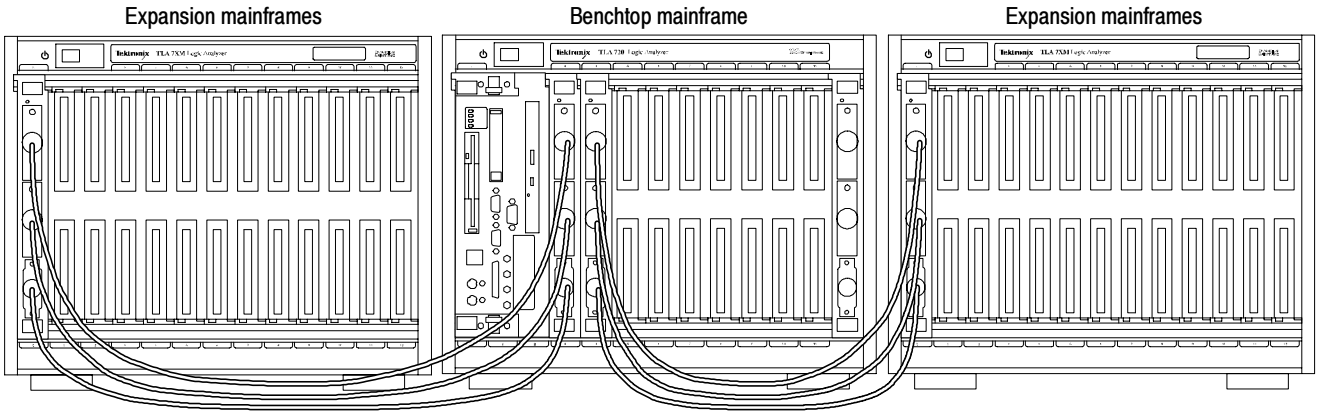


Figure 1-5: Benchtop mainframe and two expansion mainframes

When you install two expansion mainframes, software determines which expansion chassis is expansion 1 and which is expansion 2 by the order in which you install the expansion modules in the benchtop mainframe. The expansion module in the lower numbered slot will be expansion 1, and the expansion module in the higher slot will be expansion 2.

For the setup in Figure 1–5, place the EXPANSION 1 label in the outlined area on the upper right side of the expansion mainframe to the left of the benchtop mainframe. Place the EXPANSION 2 label in the outlined area on the upper right side of the expansion mainframe to the right of the benchtop mainframe.

For information on installing modules see *TLA700 Module Installation* beginning on page D–1.

Installing in a TLA714/715 Mainframe

The expansion module can be installed in any slot of the portable mainframe. If you are installing one or two expansion mainframes, you can install the expansion module in slot 1 as shown in Figure 1–6.

If the expansion module is not already installed in slot 0 of your expansion mainframe, install it now.

CAUTION. *To avoid damage to the chassis, do not use the retaining screws to seat the expansion module. These screws are intended for securing the module and reinforcing the grounding. Manually seat the expansion module by pressing it into place, and then secure it using the retaining screws.*

After seating the modules in place, use a screwdriver to tighten the retaining screws (maximum of 1.0 in-lbs).

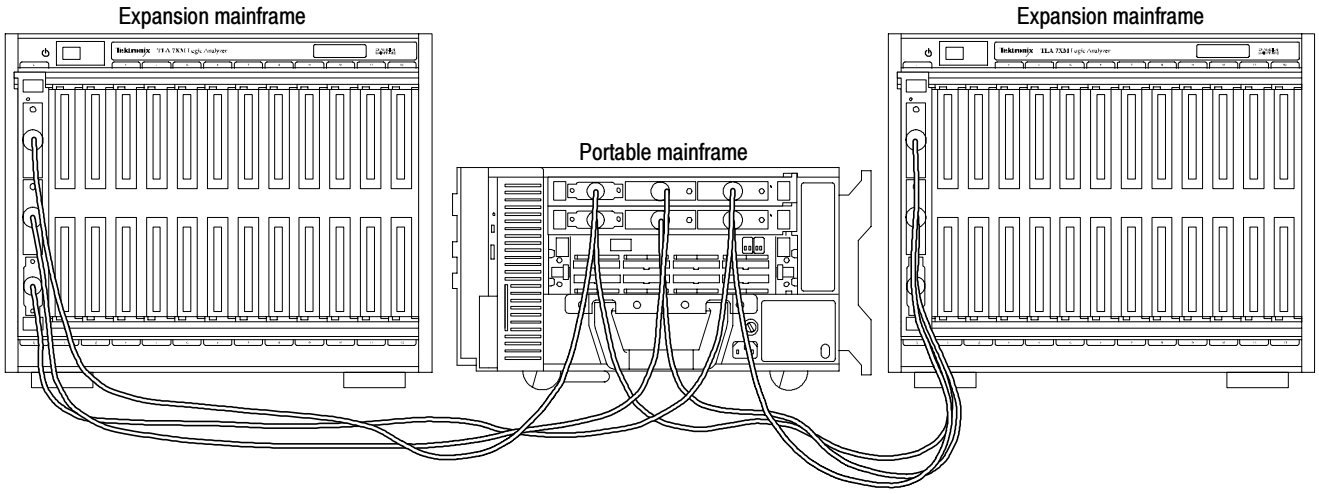


Figure 1-6: Portable mainframe shown with two expansion mainframes

Software determines which expansion chassis is expansion 1 and which is expansion 2 by the order in which the expansion modules are installed. The expansion module in the lower numbered slot will be expansion 1, and the expansion module in the higher slot will be expansion 2.

For the setup in Figure 1-6 place the EXPANSION 1 label in the outlined area on the upper right side of the expansion mainframe to the left of the portable mainframe. Place the EXPANSION 2 label in the outlined area on the upper right side of the expansion mainframe to the right of the portable mainframe.

For information on installing modules see *TLA700 Module Installation* beginning on page D-1.

Installing the Expansion Cables

There are three cables that connect the expansion modules together. To connect the expansion modules together, perform the following procedure:

1. Examine the gray expansion cable to determine if the connectors have labels. If the connectors are not labeled, apply the C labels to each connector.
2. Connect one end of the gray expansion cable to connector C of the expansion module on the expansion mainframe side. Connect the other end of the gray expansion cable to connector C of the expansion module on the benchtop or portable mainframe side.
3. Fasten the expansion cable connector to the expansion module by tightening the two hold-down screws.
4. Examine the two blue expansion cables to determine if the connectors are labeled A and B.

a. If the cables are labeled A and B, select the B cable and proceed to step 5.

b. If the cables are not labeled, select either blue expansion cable and label each connector with the B label. Select the other cable and apply the A labels to each connector.

5. Connect one end of the blue expansion cable to connector B of the expansion module on the expansion mainframe side. Connect the other end of the blue expansion cable to connector B of the expansion module on the benchtop or portable mainframe side.

6. Fasten the expansion cable connector to the expansion module by tightening the two hold-down screws.

7. Connect one end of the blue expansion cable to connector A of the expansion module on the expansion mainframe side. Connect the other end of the blue expansion cable to connector A of the expansion module on the benchtop or portable mainframe side.

8. Fasten the expansion cable connector to the expansion module by tightening the two hold-down screws.

Installing TLA700 Modules

To install additional modules for the TLA700 series logic analyzers, refer to *Appendix D: TLA700 Module Installation* for detailed instructions.

Connecting Accessories

After installing the mainframes and modules, you can connect the accessories such as external monitors, keyboard, and printer.

Connecting Accessories to the TLA600 Series

The accessory connections are the same as those you would make on a personal computer. Connect the accessories to the rear of the instrument. The connection points are shown in Figure 1-7.

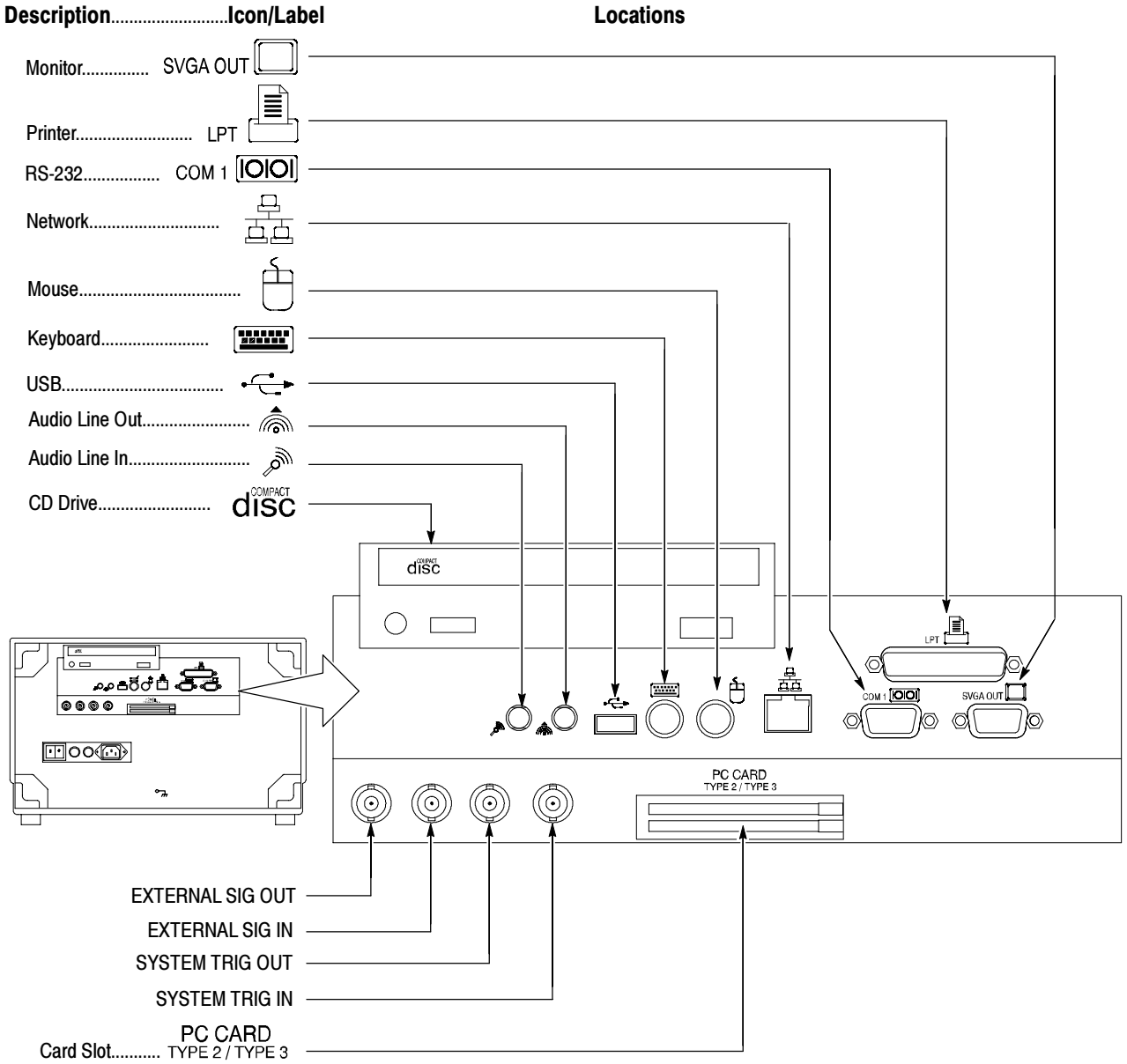


Figure 1-7: TLA600 series accessories connections

Connecting Accessories to the TLA700 Series

The accessory connections are the same as those you would make on a personal computer. The connection points are shown in Figure 1–8. Use the icons that appear in the circled areas as a guide.

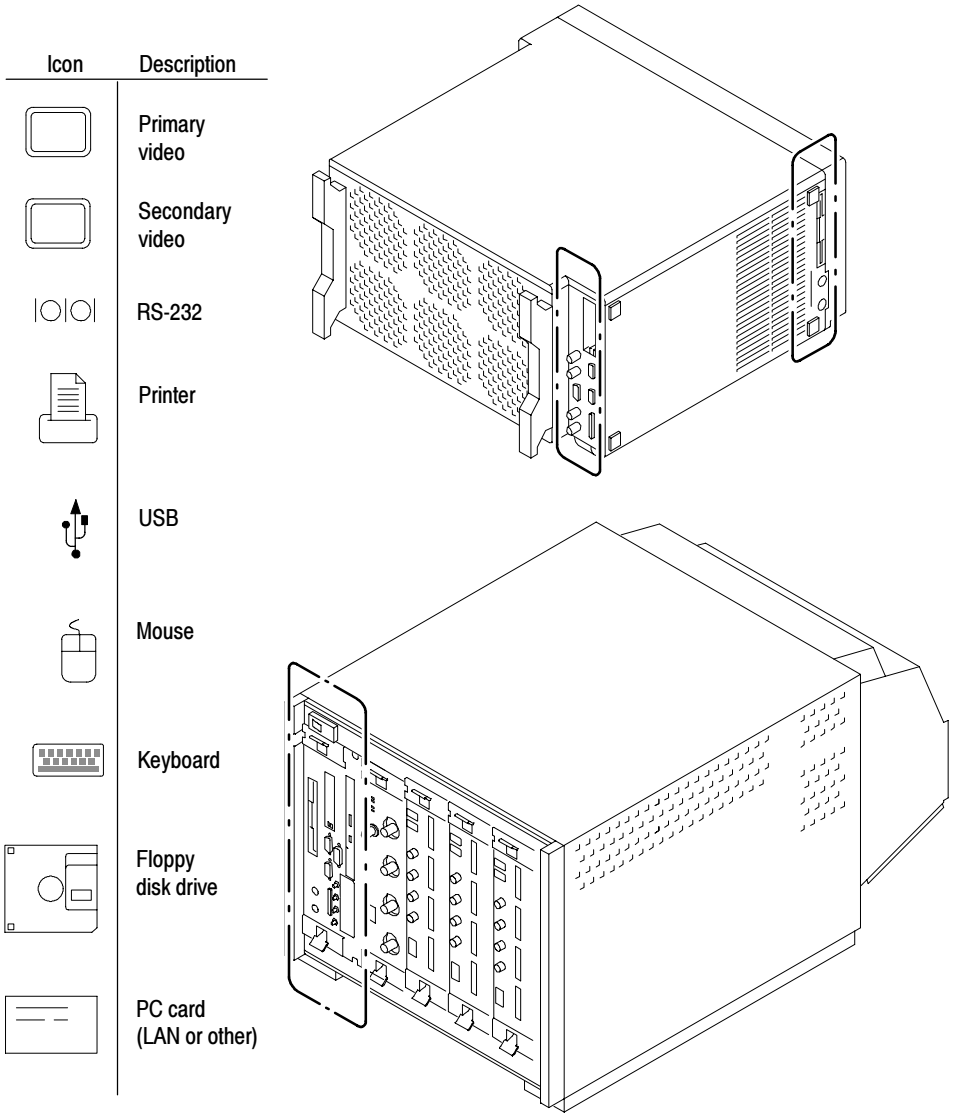


Figure 1-8: TLA700 series accessories connections

***NOTE**. Only TLA715/721 instruments have both primary and secondary video outputs. TLA714/720 instruments are equipped with only one video output.*

Additional Accessory Connection Information

Table 1–1 provides additional information on accessories.

Table 1-1: Additional accessory connection information

Item	Description
Monitor	If you use a non-standard monitor, you may need to change the the Windows display settings to achieve the proper resolution.
Printer	Connect the printer to the ECP (enhanced parallel port) connector directly. If your printer has a DB-25 connector, use the adapter cable that came with your logic analyzer to connect to the ECP connector.

Connecting Probes

Once you have connected all the accessories, you can connect the probes to the instrument. Refer to the appropriate section for your instrument.

For additional information on the individual probes, refer to the instructions that accompanied your probes.

CAUTION. *When attaching the probe to the logic analyzer, you must use care to evenly tighten probe screws until they are snug. First slightly tighten screws, then snug each screw to 4 in-lbs (max). Under tightening the probe screws can result in intermittence. Over tightening can result in stripped screws.*

Connecting Probes to the TLA600 Logic Analyzer

Connect the logic analyzer probes and the optional retaining brackets as shown in Figure 1–9.

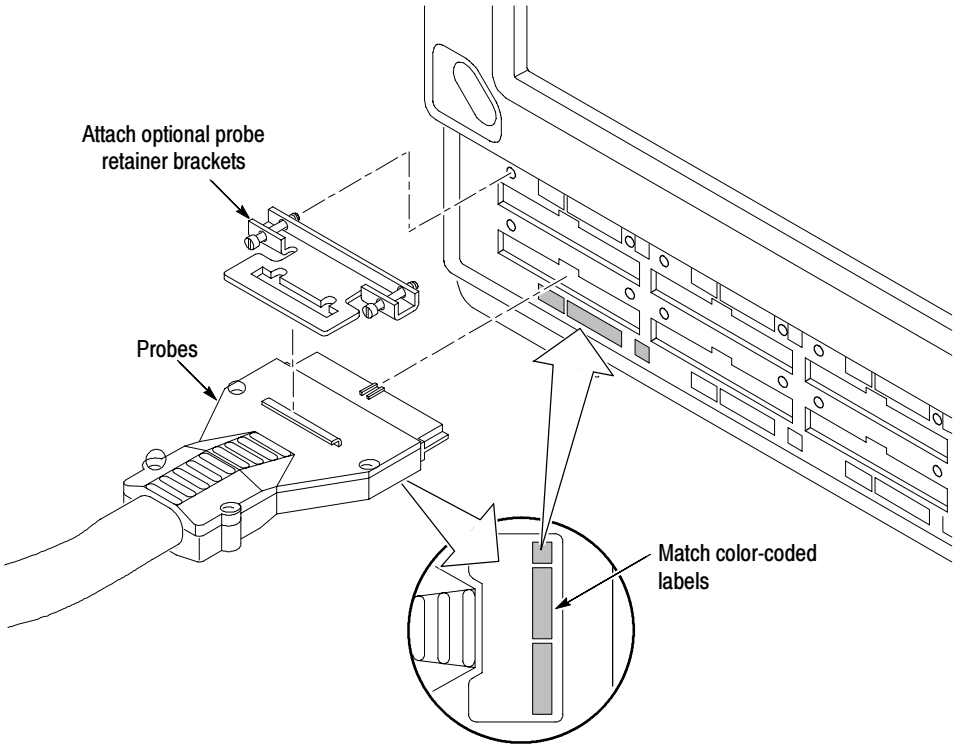


Figure 1-9: Connecting the logic analyzer probes to a TLA600 logic analyzer

Connecting Probes to the TLA700 LA Module

Connect the logic analyzer probes and the optional retaining brackets as shown in Figure 1–10 and Figure 1–11 .

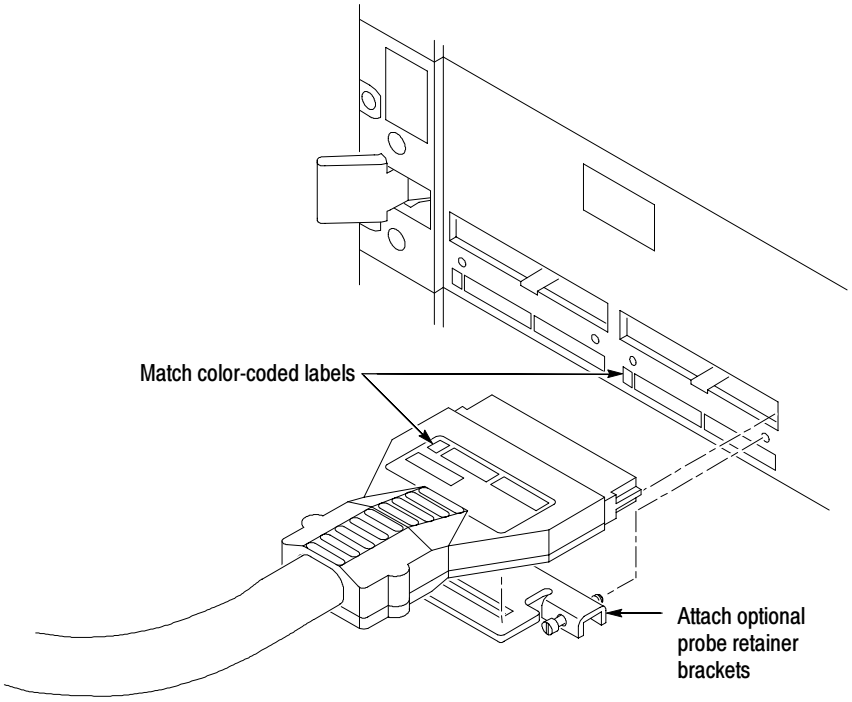


Figure 1-10: Connecting the logic analyzer probes to the TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, and TLA7Qx modules

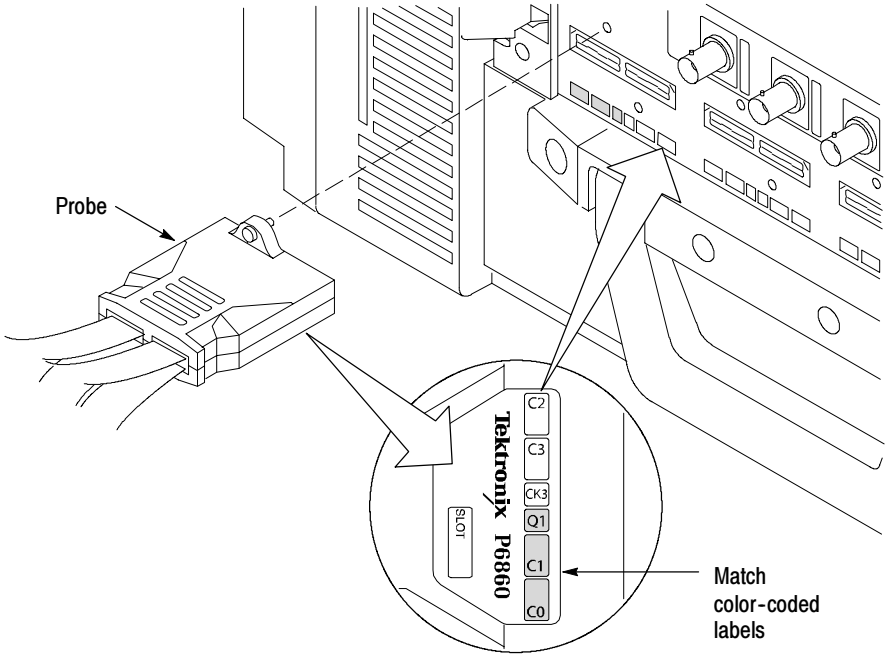


Figure 1-11: Connecting the logic analyzer probes to the TLA7Axx module

Configuring the Pattern Generator Probe

Some of the TLA Pattern Generator probes require series termination resistors to provide impedance matching for the pattern generator and the system under test. Determine the impedance matching for your application, and then refer to the TLA7PG2 Probe Instruction Manual for information about how to change the series termination resistors.

Connecting the Pattern Generator Probes

Power down the logic analyzer before connecting the pattern generator probe.

Connect the pattern generator probe as shown in Figure 1-12. The probe cable is reversible. You can connect the probe cable in either direction.

CAUTION. *To prevent damage to the pattern generator module or probe, do not connect or disconnect the probe cables while the logic analyzer is powered on.*

Although the pattern generator probe cable appears to be a SCSI cable, it is not compatible with a SCSI cable; do not use a SCSI cable with the pattern generator module, or use the pattern generator probe cable with a SCSI instrument.

The probe is fragile, handle carefully.

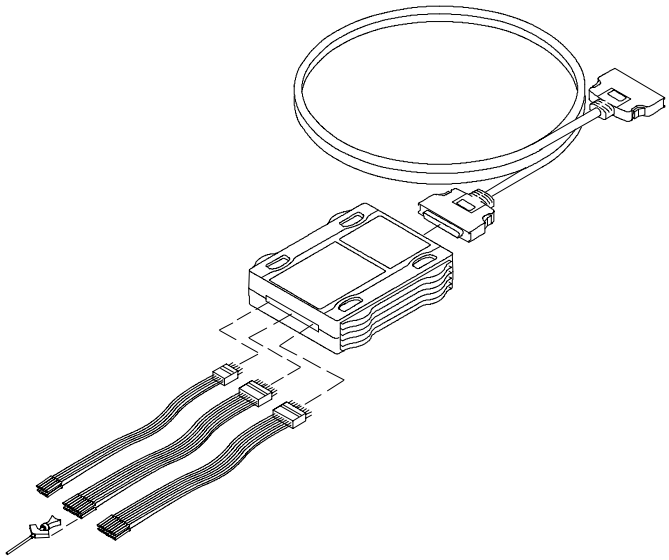


Figure 1-12: Connecting the pattern generator probes

First Time Operation

The first time your logic analyzer is turned on, you will see a TLA Final Setup icon on your desktop. Double-click the icon to launch the application for the first time. The TLA application will automatically start every time you power on the instrument.

If you have a TLA700 series logic analyzer with a pattern generator software and module installed, the pattern generator application will also automatically start.

Turning On the TLA600 Series Logic Analyzer

Follow these steps to turn on the logic analyzer for the first time:

CAUTION. *Connect the keyboard, mouse, and other accessories before applying power to the logic analyzer.*

Connecting the accessories after turning on the logic analyzer can damage the accessories.

1. Check that the line fuses are correct for your application. The instrument uses two fuses; both fuses must be the same. See Table 1-2.

Table 1-2: TLA600 series line fuses

Line voltage	Rating	Tektronix part number
90 V to 132 V operation	8 A, fast blow, 250 V	159-0046-xx
207 V to 250 V operation	6.3 A, fast blow, 250 V	159-0381-xx

2. Connect the power cord. See Figure 1–13.

3. If you have an external monitor, connect the power cord and turn on the monitor.

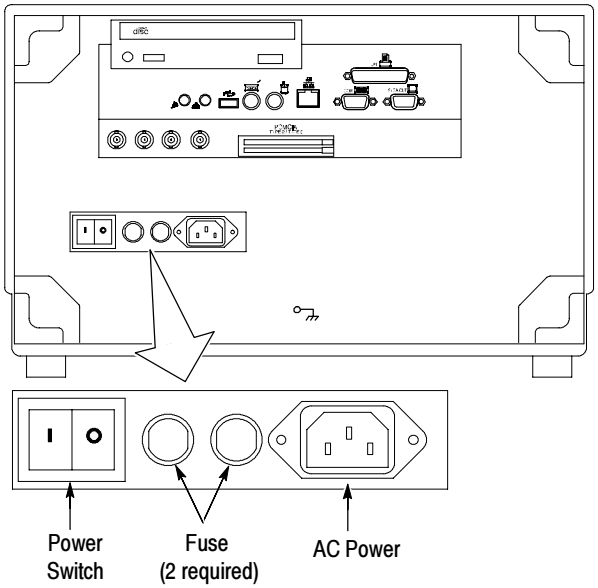


Figure 1-13: Line fuse and power cord connector locations

4. Turn on the logic analyzer as follows:

   a. Press the On/Standby switch to turn on the logic analyzer (see Figure 1–14 for the switch location).

   b. Wait for the logic analyzer to complete power-on self-tests, start Windows, and start the TLA application.

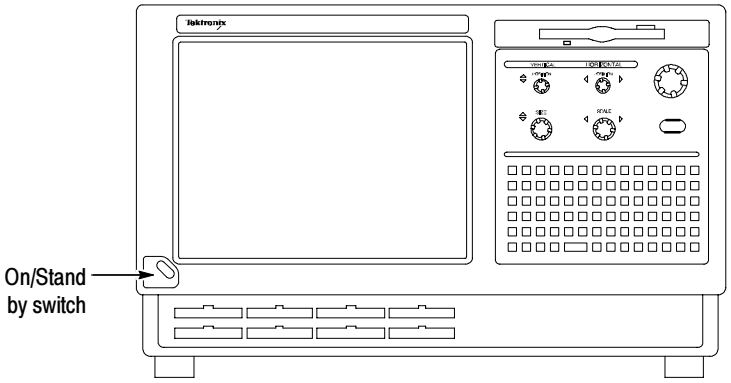


Figure 1-14: On/Standby switch locations

Turning On the TLA700 Series Logic Analyzer

Follow these steps to turn on the logic analyzer for the first time:

CAUTION. *To avoid damaging the accessories, connect the keyboard, mouse, and other accessories before applying power to the mainframe.*

1. Check that the line fuse is correct for your application. See Table 1–3.
2. Connect the power cord. See Figure 1–15.
3. If you have an external monitor, connect the power cord and turn on the monitor.

Table 1-3: TLA700 series line fuses

Line voltage	Rating	Tektronix part number
Portable mainframe		
90 V to 132 V operation	8 A, fast blow, 250 V	159-0046-xx
207 V to 250 V operation	6.3 A, fast blow, 250 V	159-0381-xx
Benchtop mainframe		
90 V to 132 V operation	20 A, slow blow, 250 V	159-0379-xx
103 V to 250 V operation	15 A, fast blow, 125 V	159-0256-xx
207 V to 250 V operation	6.3 A, fast blow, 250 V	159-0381-xx

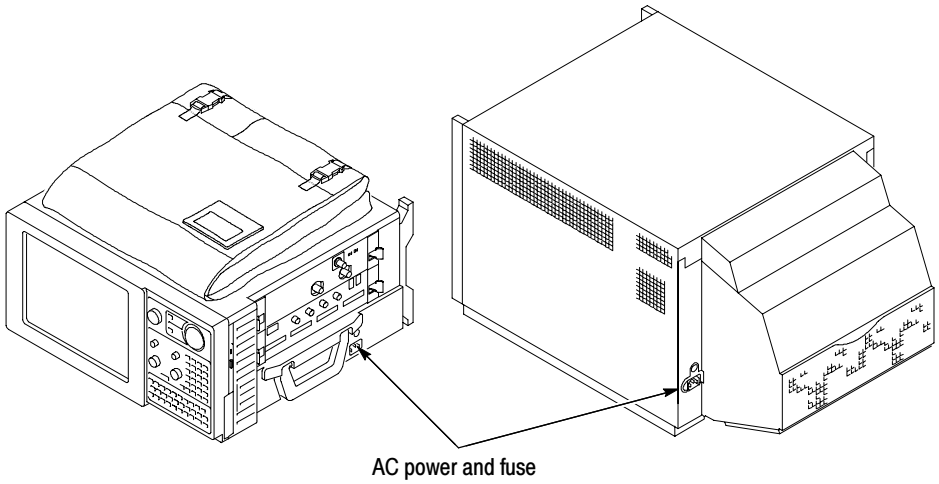


Figure 1-15: Line fuse and power cord connector locations

CAUTION. *To avoid overloading the power distribution system, if you have four or more modules in your mainframe, you must determine the correct fuse and power cord combination.*

Although the benchtop mainframe can use the power cord with the 15 A plug, mainframes operating at low line (90 VAC) with four or more instrument modules may require the power cord with the 20 A plug.

See Appendix F: Power Cord and Line Fuse Requirements for the Benchtop Mainframe *for further information.*

4. Turn on the mainframe as follows:

a. Press the On/Standby switch to turn on the mainframe (see Figure 1–16 for the switch location).

b. Wait for the mainframe to complete power-on self-tests, start Windows, and start the TLA700 application.

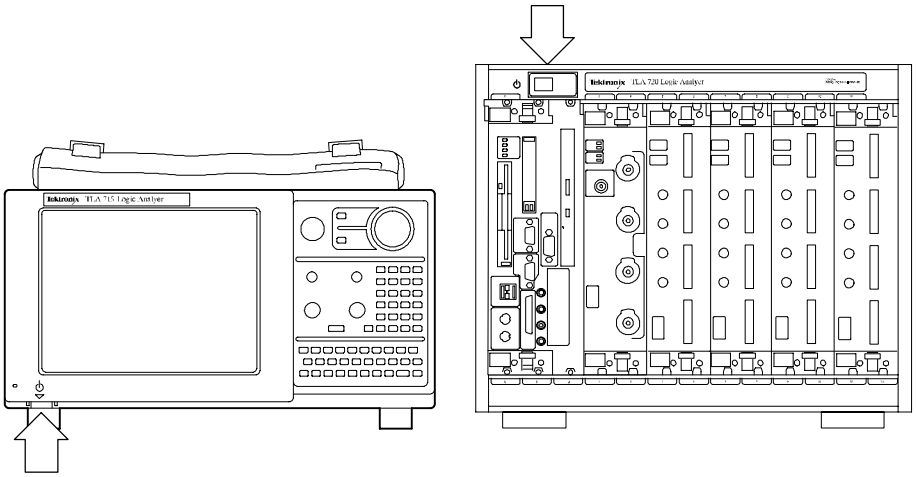


Figure 1- 16: On/Standby switch locations

Powering On the Mainframes

The expansion mainframe automatically powers on when the connected benchtop or portable mainframe powers on. If everything is properly connected and operational, you will see the expansion mainframe and the installed modules in the System window.

If the expansion mainframe and the installed modules do not display in the System window, see Table H–1 beginning on page H–10 for troubleshooting suggestions.

NOTE*. You must have a module installed in the expansion mainframe before the expansion mainframe is recognized by the resource manager and appears in the System window.*

Turning Off the TLA700 Series Mainframe

Both the TLA714/715 portable mainframe and the TLA720/721 benchtop mainframe have a built-in soft power-down function that safely powers down the mainframe when you press the On/Standby switch.

The expansion mainframe automatically powers down when the benchtop or portable mainframe is turned off.

Performing the Incoming Inspection

Incoming inspection consists of verifying the basic operation of the logic analyzer. The power-on diagnostics check the basic functionality. These diagnostics run every time you turn on the logic analyzer.

You can also verify more detailed functionality by running the self calibration and extended diagnostics.

***NOTE**. Allow the mainframe and modules to warm up for 30 minutes before running the self calibration.*

To run self-calibration and diagnostics, perform the following:

1. Disconnect any probes attached to the modules.
2. Select the System menu and point to Calibration and Diagnostics.
3. Run the self calibration followed by the extended diagnostics by selecting the proper tab. Results of the tests display on the individual property page.

To run self calibration and external diagnostics for a pattern generator, perform the following:

1. Select the Pattern Generator System menu and point to Calibration and Diagnostics.
2. Run the self calibration followed by the extended diagnostics by selecting the proper tab. Results of the tests display on the individual property page.

***NOTE**. The time required to run the self calibration on the logic analyzer modules depends on the number of acquisition channels. Modules with a large number of channels may take several minutes to run the self calibration.*

Checking the Logic Analyzer Probes (Optional)

Connect the logic analyzer probes to a signal source, start an acquisition, and verify that the acquired data is displayed in either the listing or waveform windows.

***NOTE**. If you connect probes to any channels other than the A2 and A3 groups, you must define the groups and channels in the Setup window before acquiring data on other probe channels.*

Checking the DSO Probes (Optional)

Connect the oscilloscope probes to the Probe Compensation connector on the front panel of the DSO module. You can then run the Calibrate Probe function in each vertical setup page for the module.

Checking the Pattern Generator Probes (Optional)

Set up a simple pattern generator program to output a signal to the probes. Connect an oscilloscope probe to the probe outputs and verify that the signal is present at the probe outputs.

Checking the Mainframe (Optional)

To check the mainframe diagnostics not covered by the TLA Application software, run the TLA700 Mainframe Diagnostics located under the Windows Start menu under the Tektronix TLA700 programs. Exit the TLA Application before running the external diagnostics.

Checking the P68xx Probes

To check the P68xx probes, connect the probes to a signal source, start an acquisition, and verify that the acquired data is displayed in either the listing or waveform windows.

If available, use the TLACAL2 fixture to run the performance verification. For further details, refer to the performance verification procedure in the *TLA7Axx Logic Analyzer Module Service Manual.*

Backing Up User Files

Back up your user files on a regular basis. Use the Windows back up tools or copy the files to floppy disks, to a network drive, or to another media. Always keep a backup copy of files that you access on a regular basis.

Removing the Replaceable Hard Disk Drive (TLA700 Series Only)

CAUTION. *To avoid permanently damaging the hard disk drive, do not remove it while the instrument is powered on. Always power down the instrument before removing the hard disk drive.*

1. Verify that the instrument is turned off.
2. Remove the replaceable hard disk drive cartridge by depressing it to release the latch.
3. Pull on the replaceable hard disk drive cartridge to remove it from the chassis. Figures 1–17, 1–18, and 1–19 show the procedures for removing the hard disk drive for the benchtop controller and for the portable mainframe.

NOTE*. The TLA600 series logic analyzers do not have replaceable hard disk drives.*

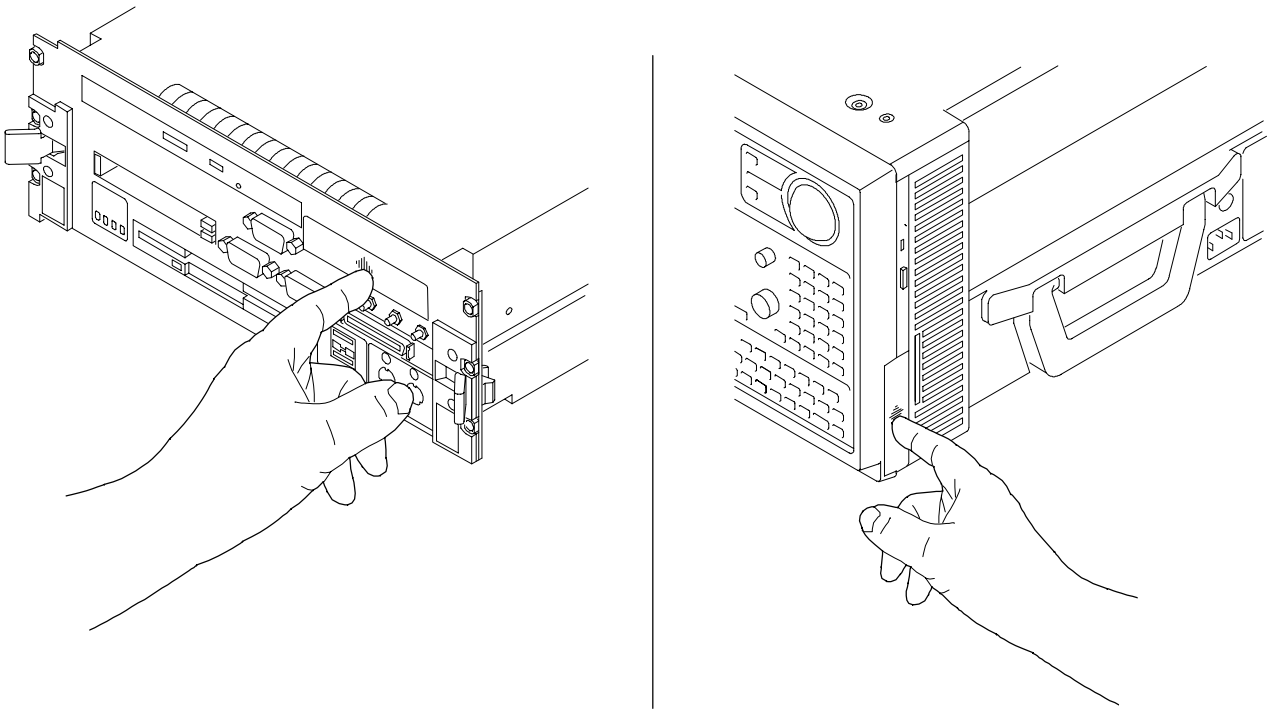


Figure 1-17: Depress the hard disk drive latch

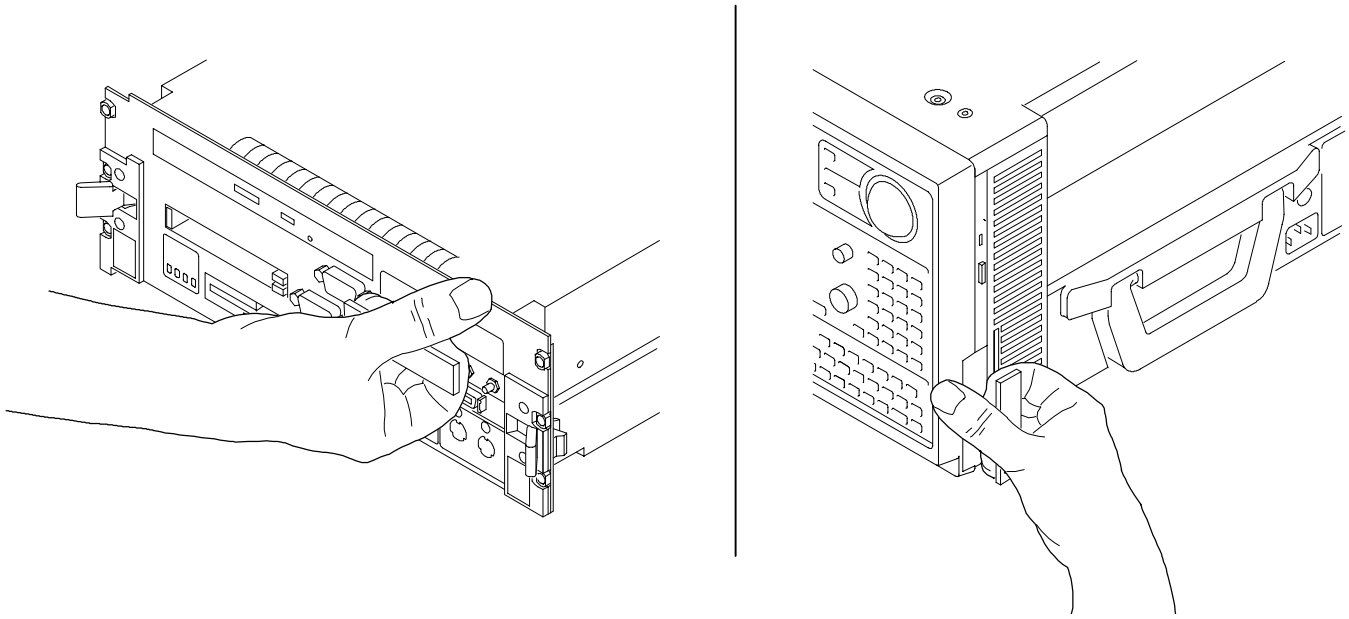


Figure 1-18: Unlatching the hard disk drive cartridge

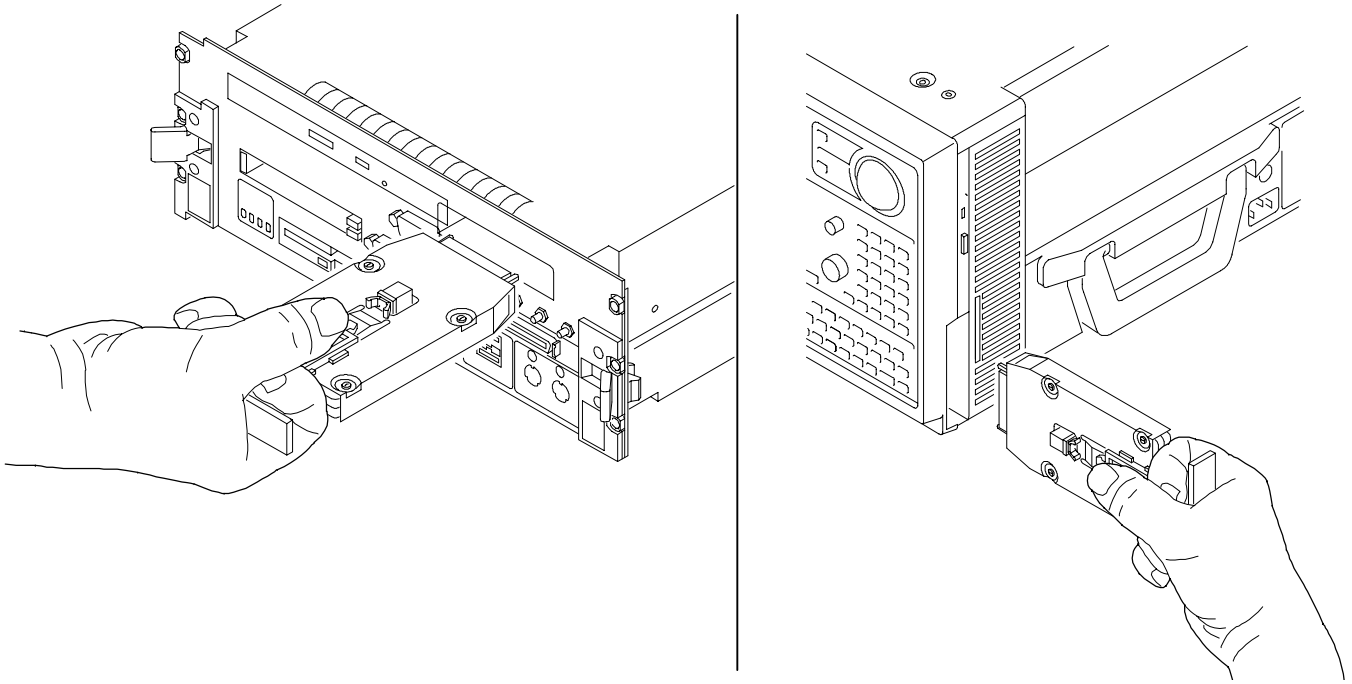


Figure 1-19: Removing the hard disk drive cartridge

Connecting Probes to the Target System

The logic analyzer connects to the target system through probes. The LA probes allow you to connect to the target system in several different ways as shown in the following illustrations. You can use the color-coded probe channels to map the hardware connections to the channel settings in the LA Setup window. Each LA probe group consists of eight channels that can be individually named in the LA Setup menu.

***NOTE**. Power off the target system and the logic analyzer before connecting the probes to the target system.*

Connect the probes to the logic analyzer by matching the color-coded label to the label on the LA module. Table 1–4 identifies the recommended probes for each logic analyzer series.

Table 1-4: Probe/Logic Analyzer cross reference

	TLA7Lx/Mx	TLA7Nx/Px/Qx	TLA600	TLA7Axx
General Purpose Probe	P6417/P6418	P6417/P6418	P6417/P6418	P6810
High Density Probe	P6434	P6434	P6434	P6860[1]
High Density Differential Probe	N/A	N/A	N/A	P6880[2]

1 **Differential clocks with single-ended data**

2 **Differential clocks with differential data**

General Purpose Connections

The P6417, P6418, and P6810 probes provide a means of connecting to the target system for most applications.

P6417 and P6418 17-Channel Probes. Figure 1–20 shows different ways to connect the P6417 and P6418 probes to the target system. To provide a secure connection to the LA module, you can optionally use the probe retainer bracket with the probe connector.

Note the location of the ground connections for the probe:

- The individual podlets have the ground (GND) engraved on the podlet.
- When you use the 8-channel leadsets, the ground lead is a single black connector. Make sure you connect the ground side of the 8-channel leadset to the ground side of the 8-channel podlet holder.

Refer to the *P6417 & P6418 Logic Analyzer Probe Instructions* for information on dimensions for the P6417 and P6418 probes.

P6810 34-Channel Probe. The P6810 probe is a 34-channel, general purpose logic analyzer probe that is used with the TLA7Axx Logic Analyzer series. Figure 1-21 shows how to connect the probe to the target system.

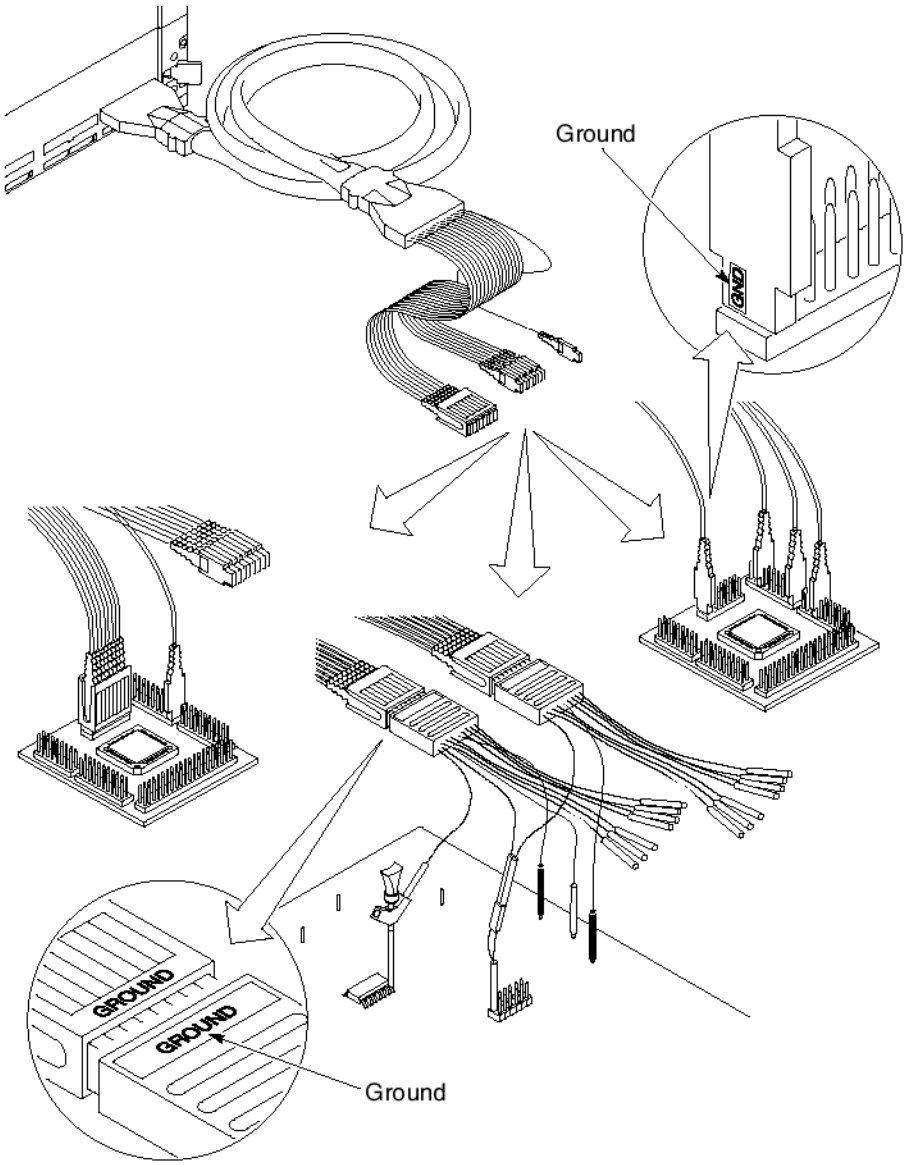
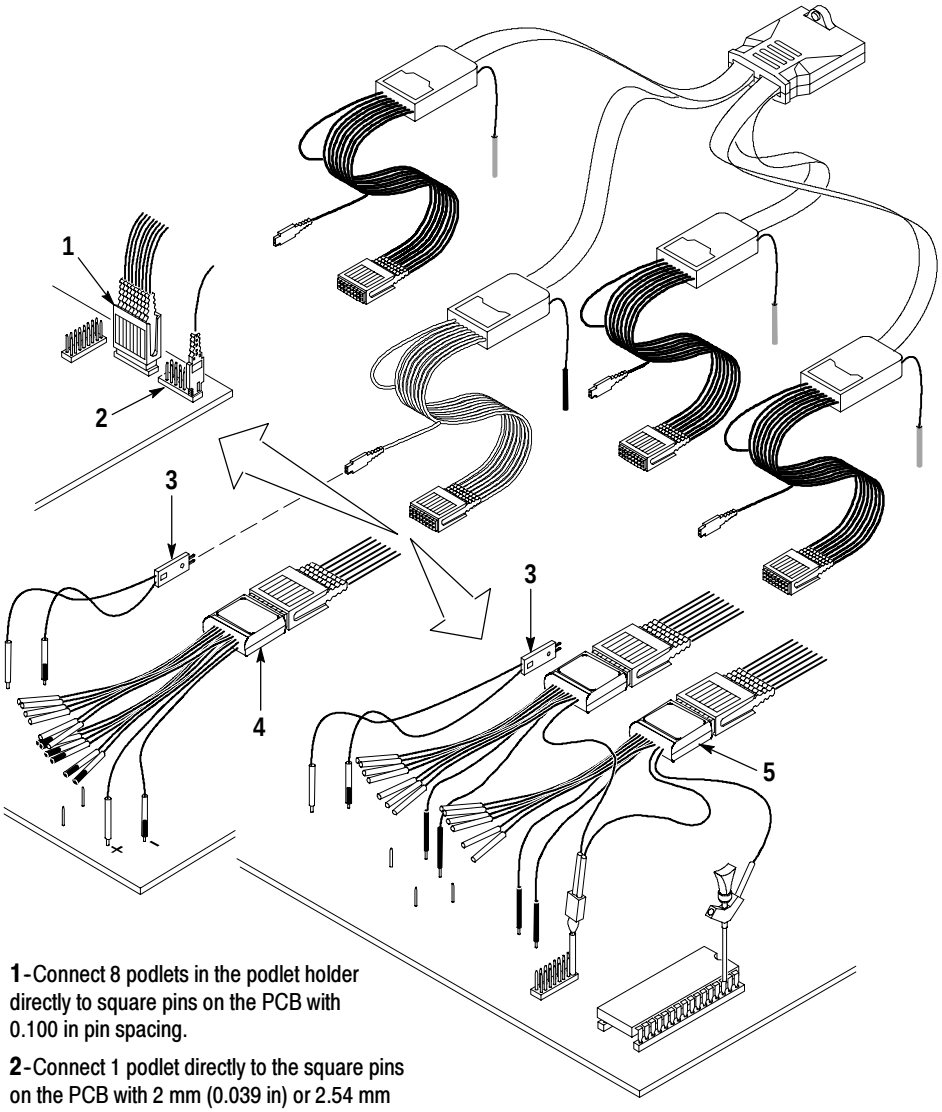


Figure 1-20: Connecting the 17-channel general purpose probe to the target system



1-Connect 8 podlets in the podlet holder directly to square pins on the PCB with 0.100 in pin spacing.

2-Connect 1 podlet directly to the square pins on the PCB with 2 mm (0.039 in) or 2.54 mm (0.100 in) pin spacing.

3-Connect 1 podlet with 1 channel leadset to the square pin on the PCB with 2 mm (0.039 in) or 2.54 mm (0.100 in) pin spacing. The negative lead (half-white/half-black housing that contains a damping resistor) is connected to ground in a single-ended application lead or the minus in a differential application.

4-Connect 8 podlets in the podlet holder with an 8 channel differential leadset to the square pins on the PCB with 2 mm (0.039 in) or 2.54 mm (0.100 in) pin spacing. The negative lead (half-white/half-black housing that contains a damping resistor) is connected to the minus in a differential application.

5-Connect 8 podlets in the podlet holder with an 8 channel single-ended leadset to the square pins on the PCB with 2 mm (0.039 in) or 2.54 mm (0.100 in) pin spacing. The negative lead (total black housing that contains no damping resistor; however, the leadset housing contains a damping resistor in ground path for each channel) is connected to ground in a single-ended application lead.

Figure 1-21: Connecting the 34-channel P6810 general purpose probe to the target system

High-Density Probe Connections

P6434 Mass Termination Probe. The P6434 Mass Termination Probe allows you to connect 34 LA channels to a microprocessor probe adapter or directly to the target system. To connect to the target system directly, you must include compatible Mictor connectors in your circuit board design.

Figure 1–22 shows two ways of connecting the LA module to a target system. For more instructions on this probe and instructions for connecting it to your target system, refer to the *P6434 Mass Termination Probe Instructions.*

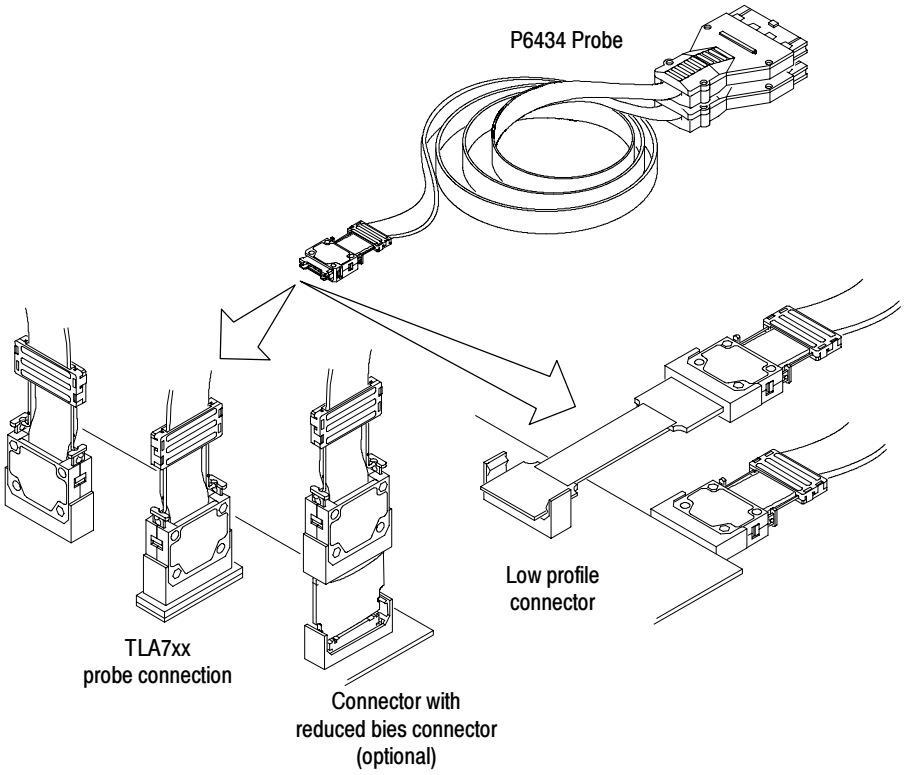


Figure 1-22: P6434 High-Density Probe connections

P6860 High-Density Probe. The P6860 probe is a 34-channel, high-density compression probe consisting of two independent probe heads of 17 channel connectors each (16 data and 1 clock/qual). This probe possesses differential clock and single-ended data input capabilities.

P6880 High-Density Differential Probe. The P6880 probe is a 34-channel, high-density differential compression probe consisting of four independent probe heads of 8/9 channels each. This probe also possesses differential clock and differential data input capabilities.

NOTE*. Compression probes provide a compression contact, which eliminates the need for a built-in connector.*

Figure 1–23 shows how to connect the compression probes to the Logic Analyzer and to the target system. For more information on the P6860 and P6880 probes and adapters, refer to the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction Manual.*

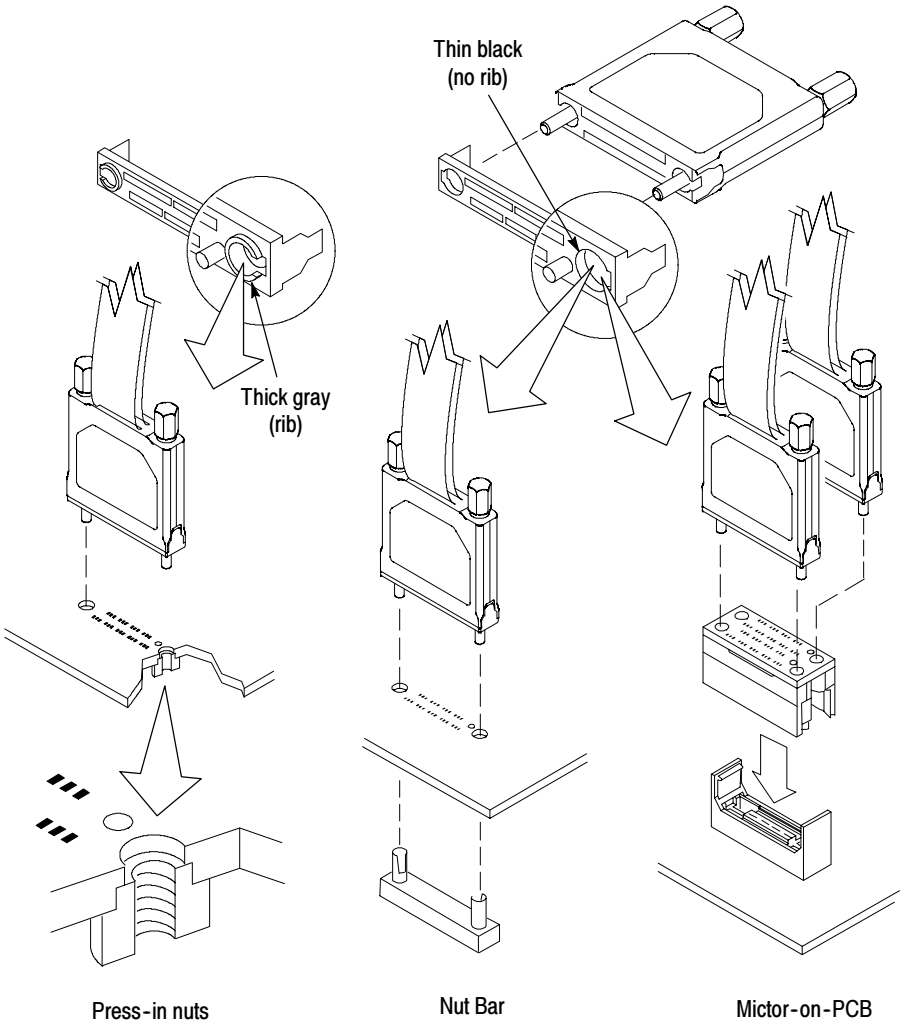


Figure 1-23: P6860 High-Density Probe and P6880 Differential Probe connections

***NOTE**. When connecting the P6860 or P6880 probe head to the target system, make sure that the alignment pin on the probe head is aligned with the hole on the test fixture. Tighten the probe head screws by alternating between them until they are finger tight (no more than 1 in-lbs of torque).*

Microprocessor Connections

All LA probes can be connected to microprocessor adapters. Refer to the documentation that came with your microprocessor disassembler package for details about connecting the probes to the microprocessor adapters and to the target system.

DSO Probe Connections

Refer to the user documentation that came with your DSO probes (P6243 and P6245 probes) for connecting and using the DSO probes.

Pattern Generator Probes

Refer to the TLA7PG2 *Pattern Generator Probe Instruction Manual* for more information on using the pattern generator probes with the pattern generator module.

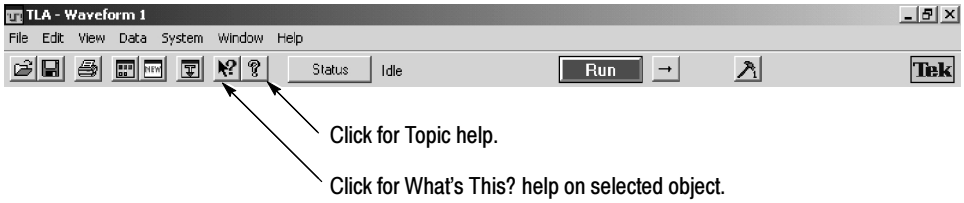
Additional Information

This section lists sources for more information. These sources are shipped with your logic analyzer.

Online Help

The online help gives detailed information about the logic analyzer and its modules. Look in the online help for details about user interface selections that are not described in this manual. The online help also has basic operating information for microprocessor support products.

To access online help, go to the Help menu or click the toolbar buttons shown:



Help topics tell you how to perform tasks and describe software features and selections shown on the screen. There are two types of help topics: overview topics and task topics.

Overview topics describe application features, such as the different application windows. Overview topics also describe concepts. Overview topics are available through the Help menu and through Help buttons in dialog boxes. From the Help menu, click Help Topics and locate the topic using the Contents or Index tab. The Help on Window selection in the Help menu provides overview help for the currently selected window.

Task topics provide procedure information about how to perform specific tasks. Task topics are available through the Help menu. From the Help menu, click Help Topics and locate the topic using the Contents or Index tab.

What's This? Help. What's This? help provides a short description of the control or screen feature selected. First click the What's This? button on the toolbar, and then click the item of interest. For further information about the item, go to the Topic help.

TPI Online Help. Select Help on TPI from the drop-down help menu for information on using the TLA Programmatic Interface. A printable version of the TPI online help is available on the instrument. Click Start > Programs > Tektronix Logic Analyzer > TLA Documentation > TPI Manual.

TLAScript Online Help. TLAScript is a script that works with TPI. Select Help from the menu bar within the TLAScript application. To start TLAScript, select Start > Programs > Tektronix Logic Analyzer > TLAScript.

Pattern Generator Online Help. Select Help on TLA7PG2 from the drop-down help menu for information on using the TLA Pattern Generator.

PPI Online Help. Select Help on the TLA7PG2 PPI from the drop-down help menu for information on using the TLA Pattern Generator. A printable version of the PPI online help is available on the instrument. Click Start > Programs > Tektronix Pattern Generator > Pattern Generator Documentation > PPI Manual.

To access the Logic Analyzer Release Notes, select Start > Programs > Tektronix Logic Analyzer > TLA Release Notes.

Microsoft Windows Online Help. Information about Microsoft Windows features is available through the Windows help system. Access Microsoft Windows help as you would with any Microsoft Windows application.

PV Adjust Online Help. Available only on the TLA7Axx modules, online help is available from the TLA7Axx PVAdjust program. To access the TLA7Axx PVAdjust program select Start > Programs > Tektronix Logic Analyzer > TLA7Axx PVAdjust. Click the Help button to access the online help.

Software

TLAVu and PatGenVu software applications provide you with the ability to view your TLA data offline on your own Microsoft Windows-based PC. Both TLAVu and PatGenVu are versions of the TLA software and Pattern Generator Software that contain online help content identical to the help provided in the respective applications.

Release Notes

The online Release Notes contain information about this release of the logic analyzer application and pattern generator application. Check the Release Notes for information such as software compatibility and software version differences from earlier releases.

To access the Logic Analyzer Release Notes, click Start > Programs > Tektronix Logic Analyzer > TLA Release Notes.

To access the Pattern Generator Release Notes, click Start > Programs > Tektronix Pattern Generator > Pattern Generator Release Notes.

Operating Basics

Functional Overview

This chapter is divided into the following sections:

- *Functional Overview.* Provides an overview of the front panel controls of the logic analyzer and the location of external connectors.
- *Approaching the Tektronix Logic Analyzer Windows.* Provides a high-level overview of the basic logic analyzer and DSO windows.
- *Approaching the Pattern Generator Application Windows.* Provides a high-level overview of the basic pattern generator windows.
- *Operating Basics.* Provides an overview of the logic analyzer operation.

Front Panel Controls

This section introduces you to the front panel controls of the TLA600 series logic analyzer and the portable mainframe. It provides a brief overview on how to use the front panel controls.

In addition to the front panel controls, you can also control the logic analyzer from an attached keyboard and mouse.

TLA600 Front Panel Controls

For the TLA61x and TLA62x you can use the front panel keys as an alternative to an external keyboard. Most keys and key combinations are available using the front panel. See Figure 2-1.

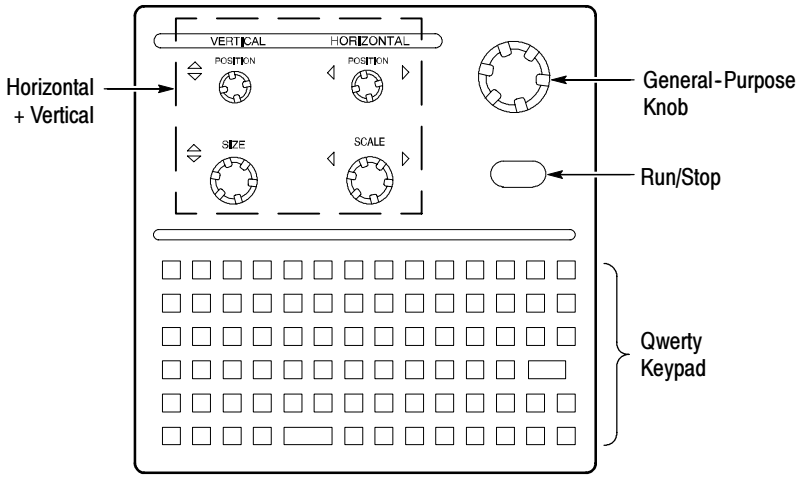


Figure 2-1: TLA61x/62x Logic analyzer front panel

For key combinations, it is not necessary to hold down more than one key at a time. For example, you can press the SHIFT key in the hexadecimal keypad, and then press a keypad key to accomplish a Shift+key combination. The same is true for other key combinations, such as CTRL and ALT keys.

Portable Mainframe Front Panel Controls

The portable mainframe has front-panel controls that operate the logic analyzer without an external mouse or keyboard.

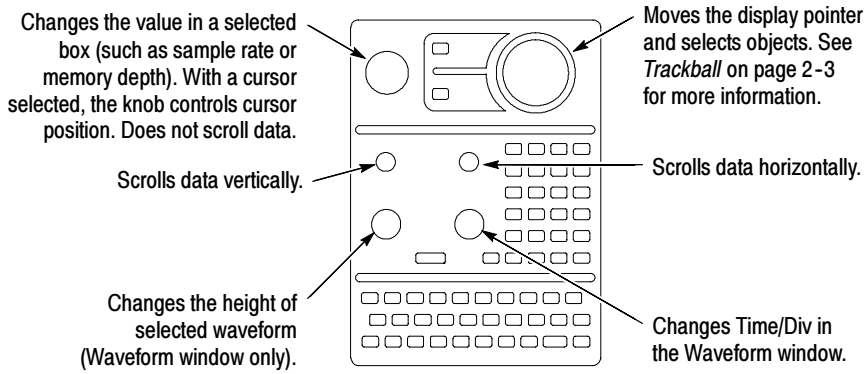


Figure 2-2: TLA715 Portable mainframe front panel

Keyboard. For the portable mainframe, you can use the front panel keys as an alternative to an external keyboard. Most keys and key combinations are available using the front panel.

For key combinations, it is not necessary to hold down more than one key at a time. For example, you can press the SHIFT key in the hexadecimal keypad, and then press a keypad key to accomplish a Shift+key combination. The same is true for other key combinations, such as CTRL and ALT keys.

GlidePoint Pad. The TLA714 Portable Mainframe has a GlidePoint pad as an alternative to the mouse. To move the pointer, slide your finger lightly over the surface of the pad. Tap the surface to simulate a click of the left mouse button, or use the control buttons to select the type of operation.

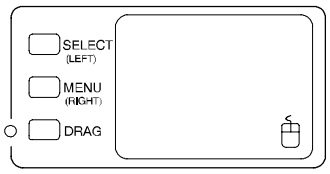


Figure 2-3: GlidePoint pad

Trackball. The TLA715 portable mainframe has a Trackball as an alternative to the mouse. To move the pointer, roll the trackball in the direction that you want the pointer to go. Press the Select button to simulate a click of the left mouse button, or use the control buttons to select the type of operation. Press the Menu button to simulate a click of the right mouse button.

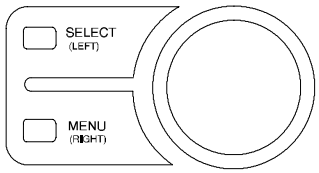


Figure 2-4: Trackball

TLA600 Series External Connectors

The external connectors on the rear panel of the TLA600 series logic analyzer are shown in Figure 2–5.

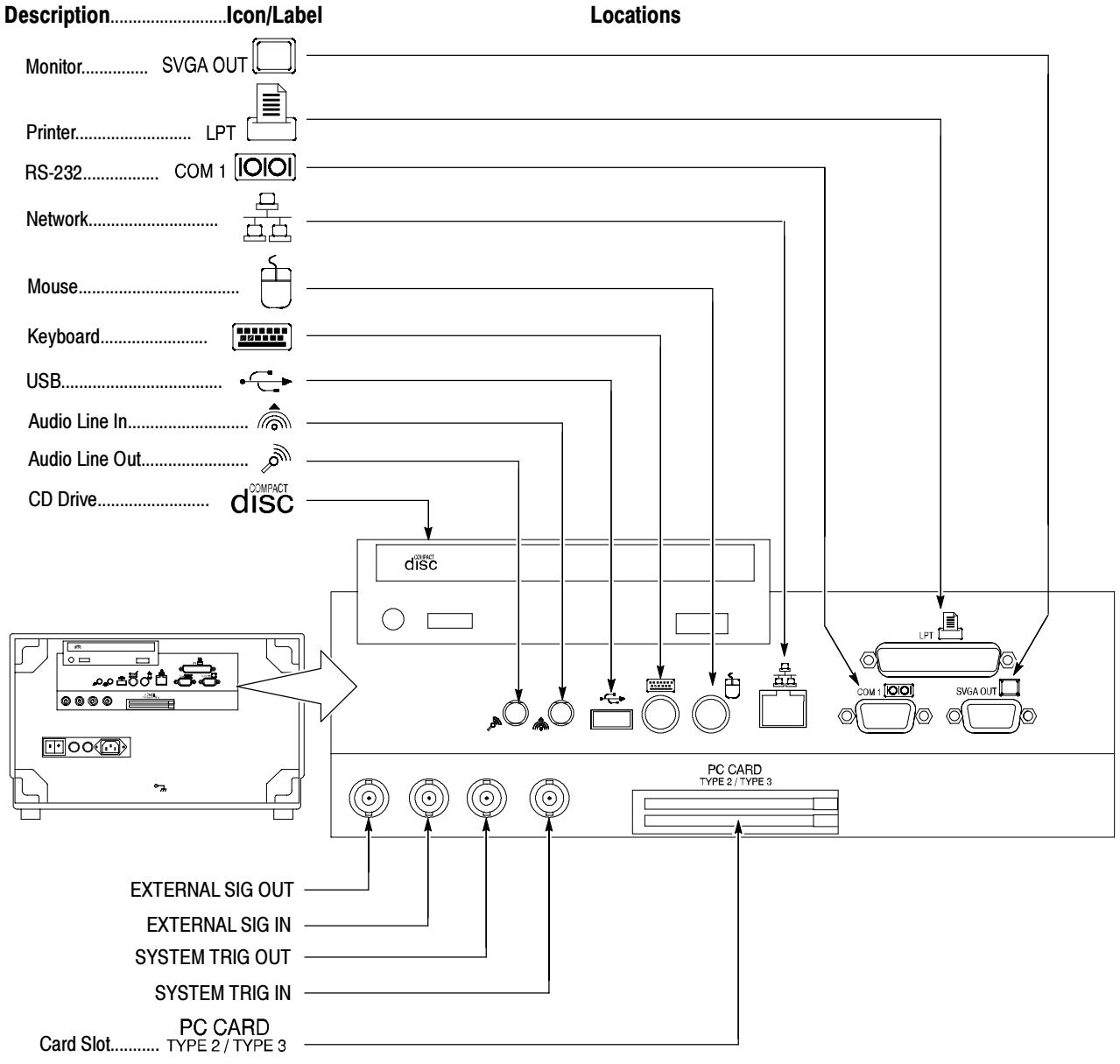


Figure 2- 5: TLA600 series external connectors

TLA600 Series Chassis Ground Connections

Figure 2–6 shows the chassis ground connection. Use the chassis ground connections to connect the grounds of the target system (system-under-test) to the logic analyzer to ensure a common ground connection between instruments.

WARNING. *To reduce the risk of an electrical shock, do not remove the safety ground screw from the logic analyzer. The safety ground screw must always be in place to ensure proper grounding of the power supply to the logic analyzer.*

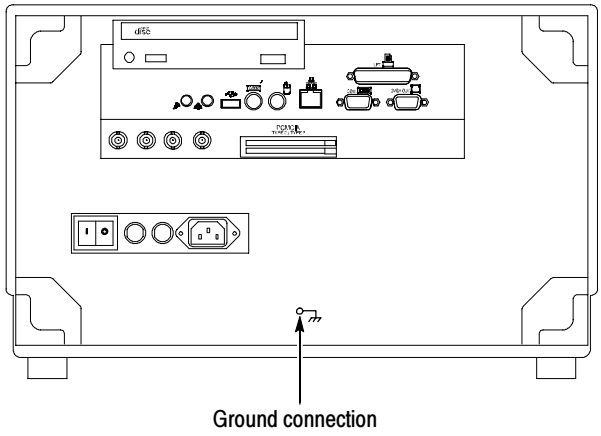


Figure 2-6: Location of ground connection

TLA700 Series External Connectors

The mainframe external connectors are shown in Figure 2–7. The following connections are available:

- System Trigger In and System Trigger Out, used to receive or send a trigger from/to an external source.
- External Signal In and External Signal Out, used to receive or send a signal from/to an external source.
- Accessory connections.

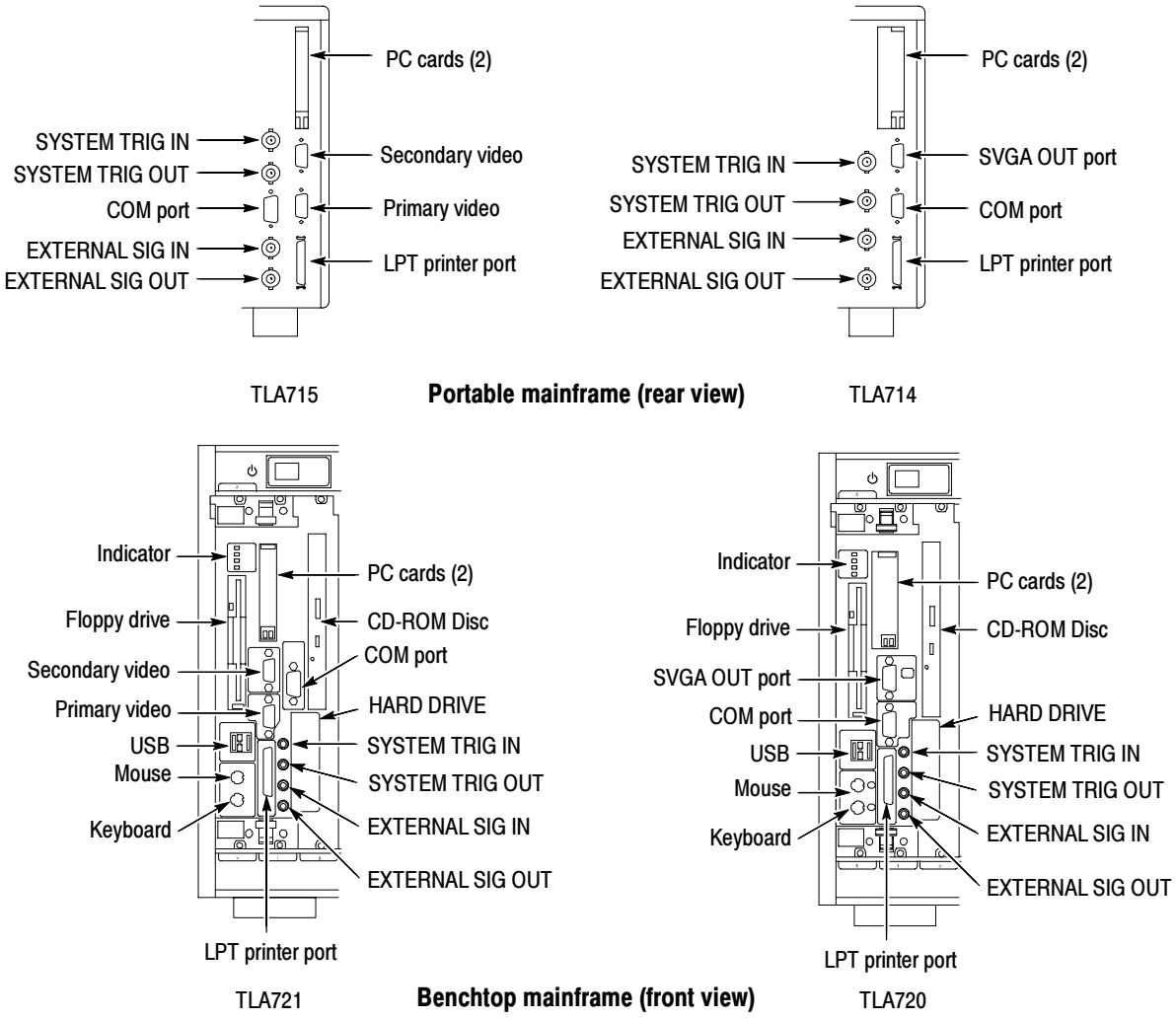


Figure 2-7: TLA700 series external connectors

TLA700 Series Chassis Ground Connections

Figure 2–8 shows chassis ground connections. Use the chassis ground connections to connect the grounds of one or more instruments to the mainframe to ensure a common ground connection between instruments.

WARNING. *To reduce the risk of an electrical shock, do not remove the safety ground screw from the benchtop mainframe. The safety ground screw must always be in place to ensure proper grounding of the power supply to the mainframe.*

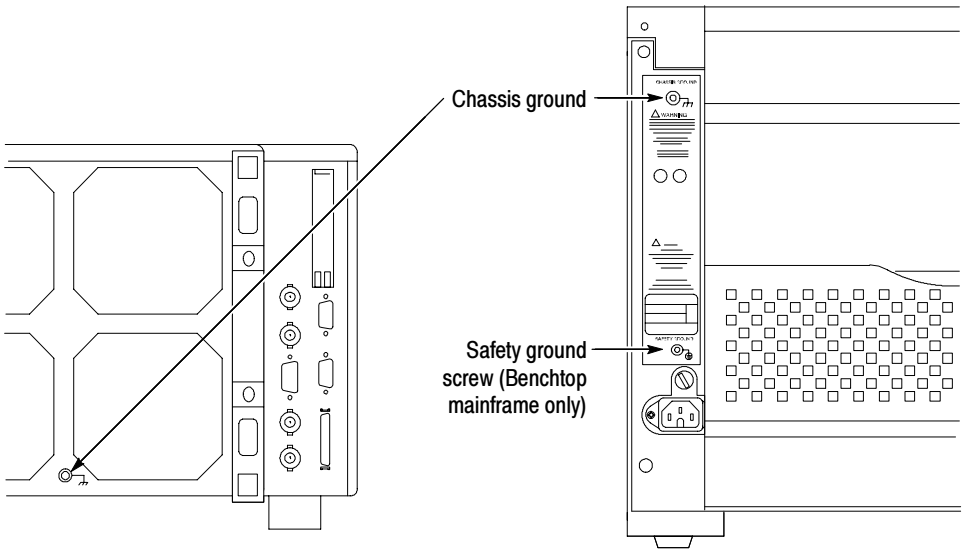


Figure 2-8: Location of ground connections

Approaching the TLA Application Windows

The Tektronix Logic Analyzer application interface consists of Setup and Data windows as shown in Figure 2–9.

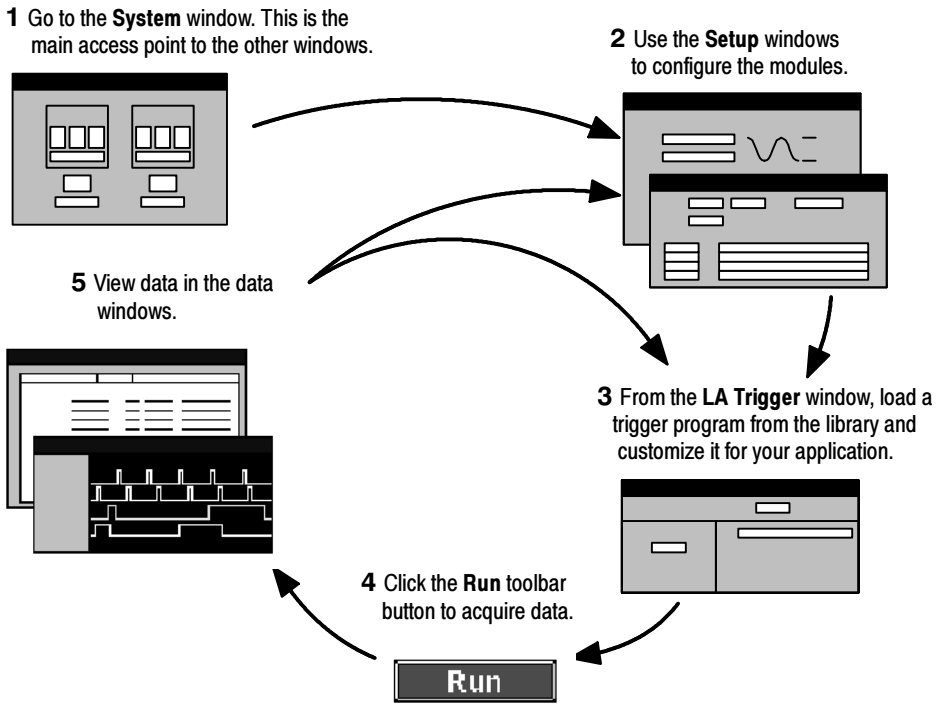


Figure 2-9: Window usage control flow

System Window

The System window is your point-of-entry into the logic analyzer and functions as the overall control center. The System window on a TLA600 series logic analyzer (Figure 2–10) is almost identical to the System window on the TLA700 series logic analyzer (Figure 2–11). The only difference between the two System windows is that the TLA700 series System window reflects the additional modules available with the TLA700 series.

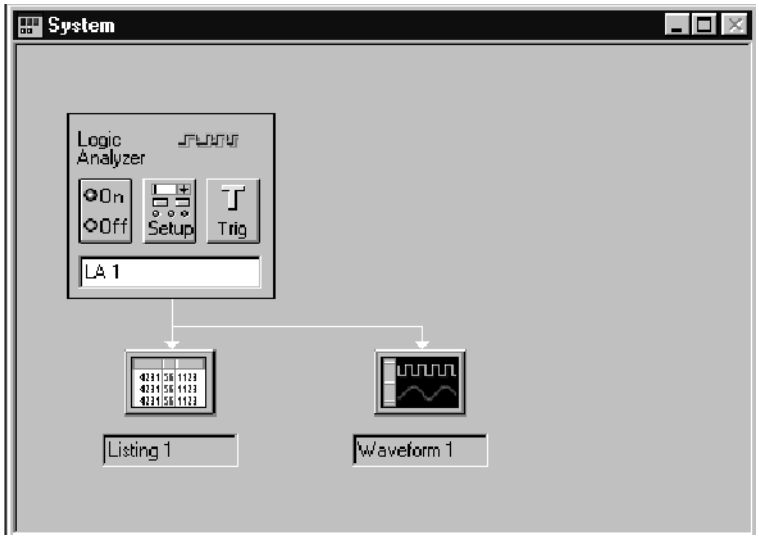


Figure 2- 10: System window on a TLA600 series

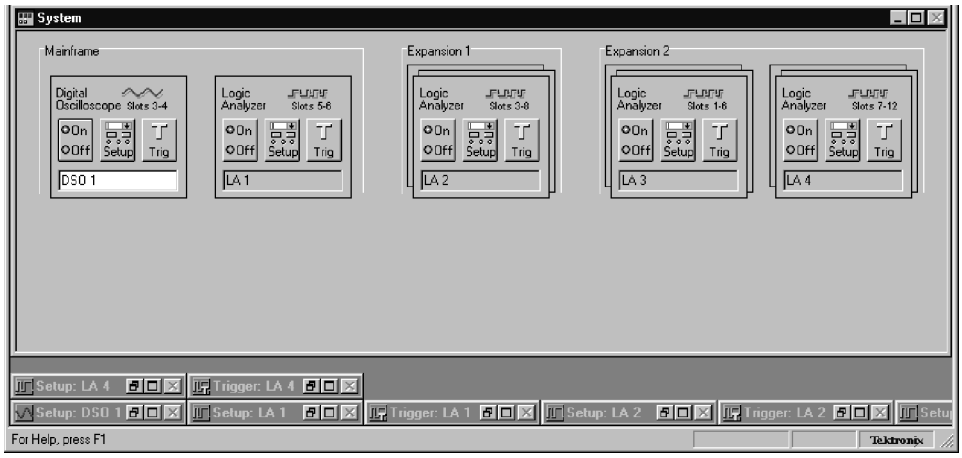


Figure 2- 11: System window on a TLA700 series

You can perform the following functions from the System window:

- Open module and data windows by clicking their icons. To select a module without opening its window, click inside the icon.
- Create new data windows through the New Data Window wizard. You can create Histogram windows for performance analysis operations and Source windows to track the execution of source code. You can also create additional Listing and Waveform windows.

- Use the System window for an overview of how the modules and data windows relate to one another. Relationships between modules (if any) are always shown; to view which modules are associated with a data window, you must select the module icon.
- View which modules provide data to each window by clicking the window name.
- Enable and disable modules by clicking their On/Off buttons.
- Save and load files containing setup, trigger, and data information using the File menu.
- Add an external oscilloscope connection or delete an existing external oscilloscope connection using the context menu.

Setup Windows

Before you acquire and display data, you must first configure the modules using the module Setup windows. Each module has its own Setup and Trigger window; each module is set up individually. Configure the Setup window before configuring the Trigger window because the Setup window settings affect the Trigger window selections. An example of a logic analyzer Setup window is shown in Figure 2–12.

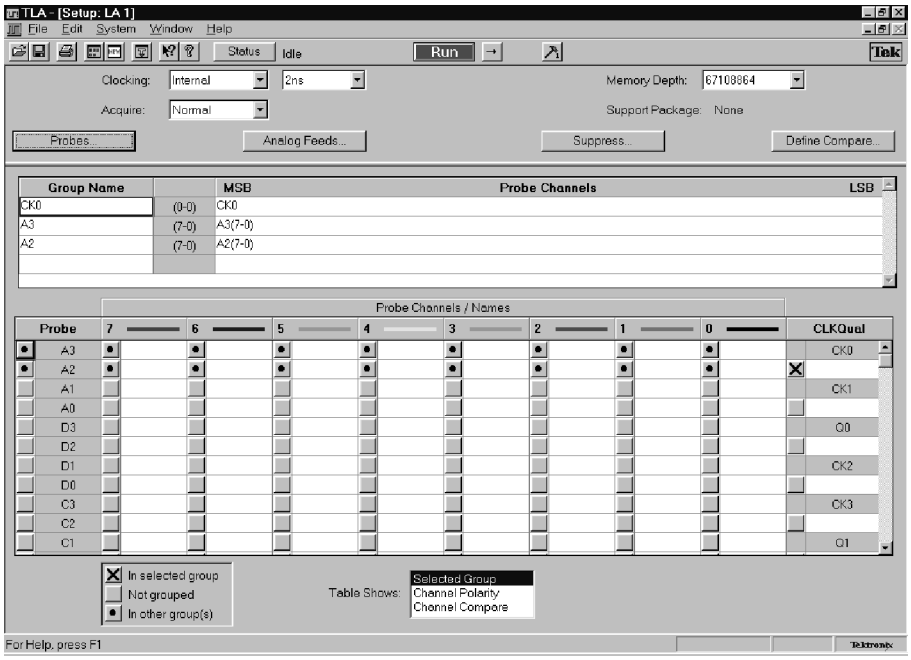


Figure 2-12: LA Setup window

Use the DSO Setup window to define the channel and horizontal setups for the DSO module. An example of a DSO Setup window is shown in Figure 2–13.

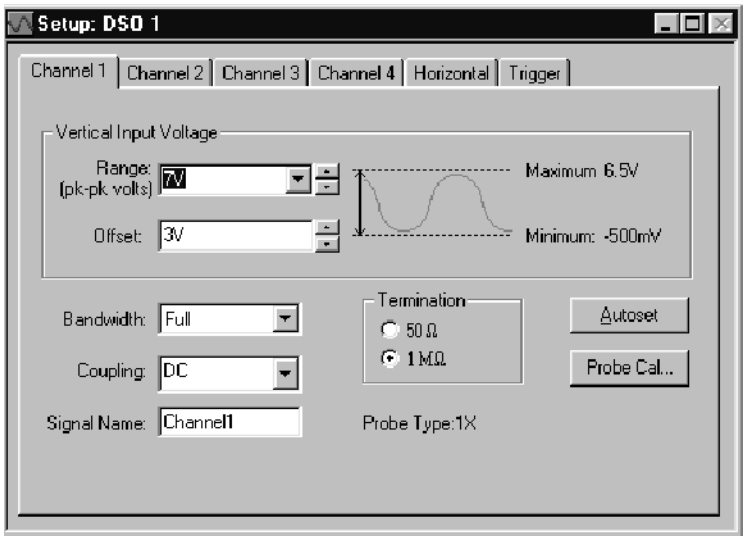


Figure 2- 13: DSO Setup window

Trigger Windows

Logic analyzer and DSO modules have their own Trigger windows. Use the Trigger window to define the conditions when the instrument acquires and stores data.

LA Trigger Window

This version of the TLA600/700 logic analyzers simplifies triggers by providing a list of trigger programs for you to either load or use as the basis for developing customized trigger programs that are specifically designed to your data requirements. The EasyTrigger tab lists all available predefined trigger programs and provides both a text description and graphical representation of each. The system responds by displaying a simplified version of the program's event conditions. The PowerTrigger tab shows the general structure of the trigger program and summarizes activity within individual program states.

You can also use the PowerTrigger tab to manually define simple or complex trigger programs one step at a time to determine how the logic analyzer finds the data you are interested in.

See Figure 2–14 for an example of the default LA Trigger window.

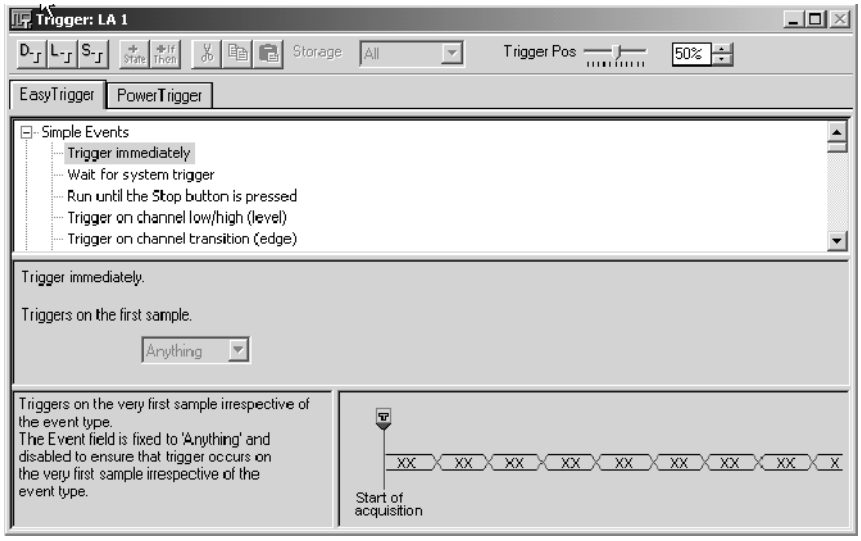


Figure 2-14: LA Trigger window

DSO Trigger Window

The DSO Trigger window lets you define how to trigger the DSO on analog and digital signals. See Figure 2–15.

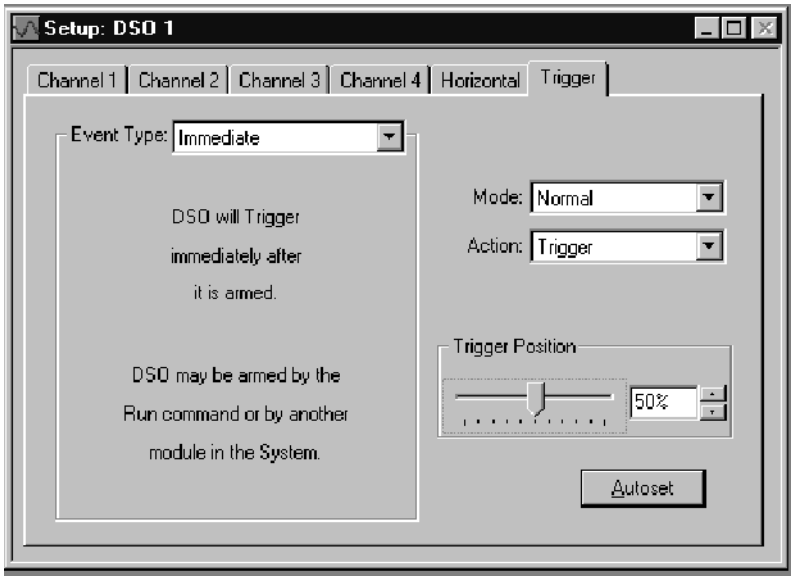


Figure 2-15: DSO Trigger window

Data Windows

You can use data windows to display and analyze acquired data from the logic analyzer or DSO modules. The most common data windows are the Listing windows and Waveform windows. These are the two default windows.

To display and evaluate complex logic analyzer data, you can create other types of data windows using the New Data Window wizard (such as the Histogram window and the Source window). For more information on the New Data Window Wizard, refer to *Creating a New Data Window* beginning on page 3-90 or the online help.

You can have as many data windows as you want to display different data or different views of the same data.

Listing Windows

Listing windows display logic analyzer data in lists or columns. The following list describes some of the tasks you can perform with Listing windows.

- Place user marks to flag specific data samples for evaluation.
- Use the scroll bars to move through the data or jump to a specific point in the data by clicking the Go To toolbar button and selecting a mark.
- Search for a data event by clicking the Define Search button in the toolbar.
- Add columns by clicking the Add Column toolbar button.
- Move columns by clicking on their labels to select them, and then dragging them to a new location.
- Split the window into two panes for viewing data that is off screen.
- Click and drag columns.
- Identify sample suppression.

Waveform Windows

Waveform windows display DSO or LA waveform data. The following list describes some of the tasks you can perform with Waveform windows.

- Perform automatic measurements on DSO analog waveforms.
- Use the cursors to take time or voltage measurements.
- Place user marks to flag specific data samples for evaluation.
- Overlay waveforms.

- Identify sample suppression.
- View collections of logic analyzer module waveforms as busforms.
- View the value of a logic analyzer module waveform group versus time using magnitude mode.
- Expand and contract busforms.
- Move waveforms by clicking their labels to select them and then dragging them to a new location.
- Split the window into two panes for viewing data that is off screen.
- Use the scroll bars to move through the data or jump to a specific point in the data by clicking the Go To toolbar button and selecting a mark.

Histogram Windows

Histogram windows display logic analyzer data as histograms. You use Histogram windows to evaluate the performance of software, which is also known as performance analysis. The following list describes some of the tasks you can perform with Histogram windows.

- Use the scroll bars to move through the data.
- Sort histogram data by ranges, counts, or percentages.
- Change the magnification of histogram bars to view the data in greater detail.
- Split the window into two panes for viewing data that is off screen.
- View various statistics on the acquired data.

Source Windows

Source windows display source data. You can track the execution of source code, based on the data displayed in a Listing window. The following list describes some of the tasks you can perform with Source windows.

- Step through source code statements.
- Turn source code line numbers on or off.
- Place user marks to flag specific data samples for evaluation.
- Use the scroll bars to move through the data, or jump to a specific point in the data by clicking the Go To toolbar button and selecting a mark.
- Search for source code statements by clicking the Define Search button in the toolbar.
- Determine whether there is any acquired data for the corresponding source file displayed in the Source window.

MagniVu Data

MagniVu data is the result of asynchronous digital oversampling acquisition. This data is automatically acquired whenever you perform an acquisition. This means that even if you specify synchronous acquisition, you can view the asynchronous data at any time without having to reacquire. MagniVu functionality is designed to acquire data at a high sample rate allowing you to see the timing of signals in much greater detail. This is useful when you are debugging hardware and needing higher resolution data samples for viewing events that change very quickly.

The logic analyzer modules have MagniVu data acquisition as a standard feature. MagniVu acquisition offers 500 ps high-resolution sampling rate on both TLA600 and TLA7Lx/Mx/Nx/Px/Qx modules simultaneous with either 100 MHz or 200 MHz maximum synchronous speed on all channels through the same probes. Both the MagniVu sample and storage rates are 2 GS/s. MagniVu memory depth is set to a fixed 2K.

MagniVu acquisition for TLA7Axx modules offers 125 ps high-resolution sampling rate with 120, 235, or 450 MHz maximum synchronous speed on all channels through the same probes. The MagniVu *sample* rate is 8 GS/s; while the MagniVu *storage* rate can be 8 GS/s, 4 GS/s, 2 GS/s or 1 GS/s. Setting a lower storage rate allows you to stretch MagniVu memory over a greater span of time, providing a lower resolution data sample from a greater time period. MagniVu memory depth is set to a fixed 16K.

The example in Figure 2–16 shows regular data and MagniVu data for the same channels. The MagniVu channels have the “Mag_” prefix associated with each channel and with group names. You can add MagniVu data with the Add Waveform toolbar button.

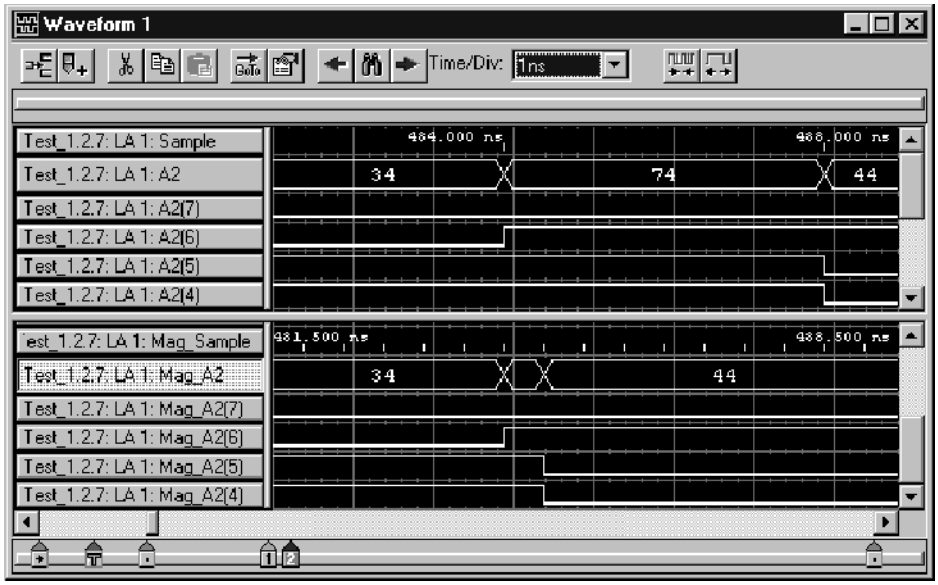


Figure 2- 16: Comparing regular and MagniVu data

Saving and Loading Setups and Data

Once you set up the logic analyzer to your satisfaction, you will probably want to save the setup for future use. You can save setup information as a saved system file or as a saved module file. You can also independently save LA module trigger information.

Saved system files contain setup and trigger information for each module as well as system level information (such as repetitive properties) and data windows for the logic analyzer. Saved module files contain setup and trigger information for only the specified module. In both cases, you have the option of saving acquired data with the files. Saved LA module trigger files contain trigger state information as well as information about the currently selected EasyTrigger program. If you do not use an EasyTrigger program as the basis for your modified trigger design, but instead use the PowerTrigger tab to develop your trigger program, only a TLA file with the state information is saved.

Execute Save and Load operations from the File menu. For module Save or Load operations, you must first go to the module Setup or Trigger window. Execute the trigger save operation by clicking the Save Trigger button from the Trigger window.

Save the setups and data in a folder where you can easily retrieve them. For example, you may want to save the data in the My Documents folder or within a folder of your own choosing. You should not save the data in a location that may be difficult to find or in a location (such as the Microsoft Windows System folder) that may cause problems with your operating system.

Avoid using file name extensions other than the default extensions supplied by the system. The logic analyzer may not recognize saved setups with nonstandard file name extensions.

Saved system and module files both contain trigger program information. When you load a trigger from the LA Trigger window, you can select a saved system or module file as the source. When you do so, the logic analyzer extracts only the trigger information from the file and loads it to the module.

Customizing the Display

You can customize your data windows. Using property sheets, you can control data window display parameters. Many screen elements, such as waveforms, columns, and marks, have their own property sheets. Figure 2–17 shows an example of a typical property sheet.

Open data window property sheets by clicking the Properties toolbar button on the data window. Open screen element property sheets by double-clicking the element or its label.

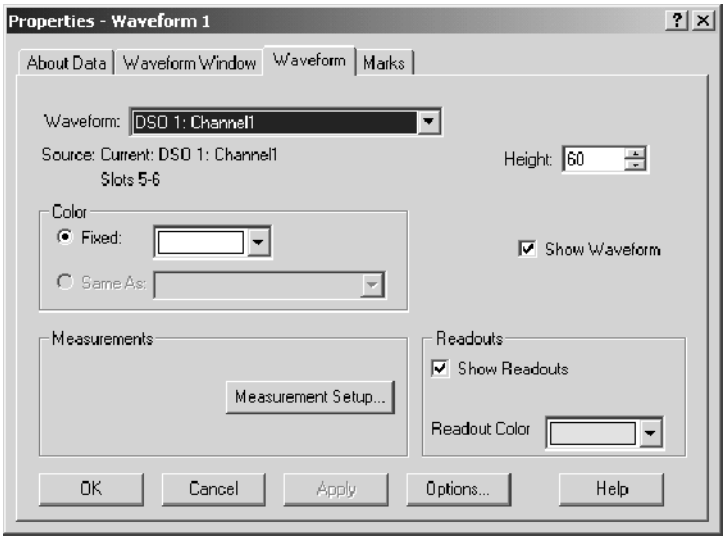


Figure 2- 17: Using a property sheet to customize the display

Programmatic Control

In addition to controlling the logic analyzer from the user interface, you can use the TLA Programmatic Interface (TPI) to control the logic analyzer from a separate program running on the logic analyzer or on a remote host. Information for using TPI is included as part of the TLA online help. A printable version (PDF file) of the TPI online help is available on the instrument. Click Start > Programs > Tektronix Logic Analyzer > TLA Documentation > TPI Manual.

Approaching the Pattern Generator Application Windows

The TLA pattern generator application is similar to the logic analyzer application. Typically you use the windows in the pattern generator application as shown in Figure 2–18.

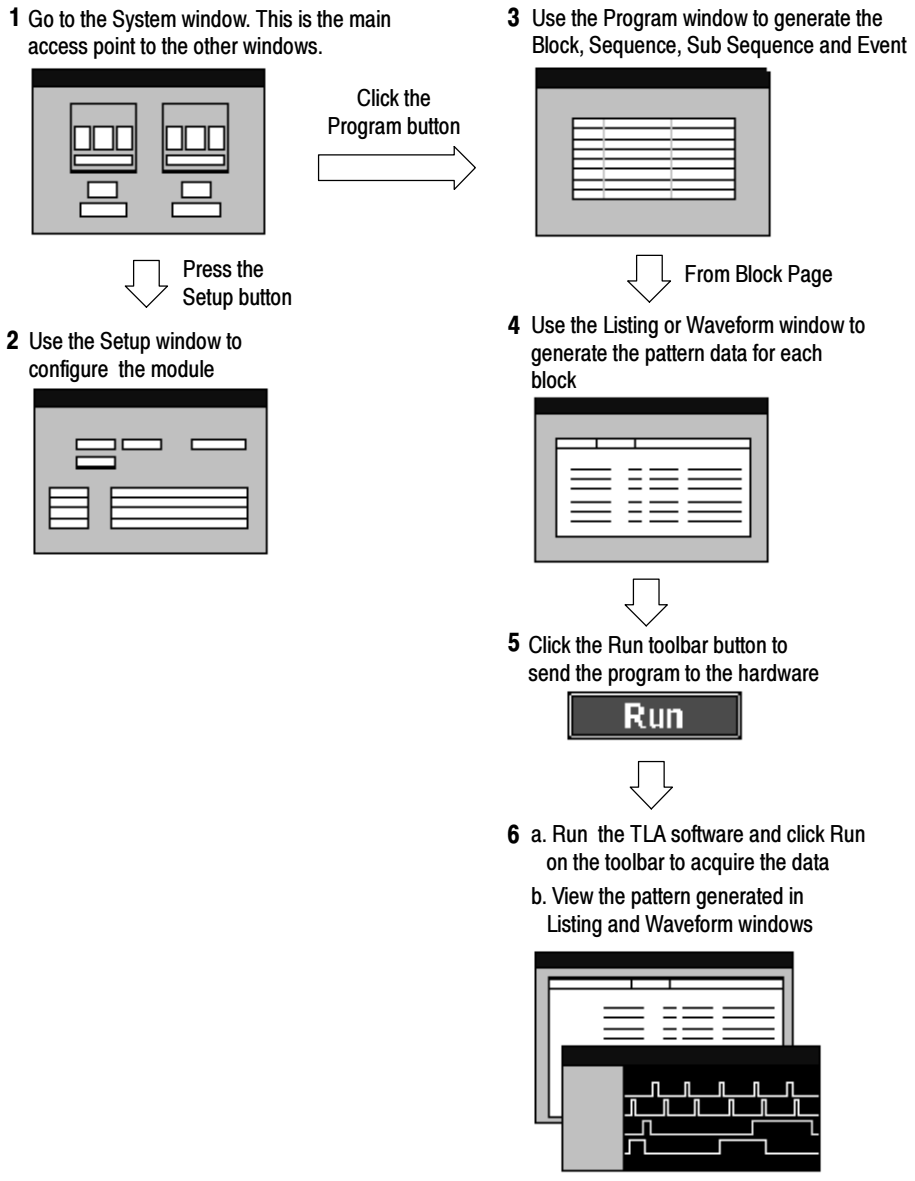


Figure 2-18: Window usage control flow

System Window

The pattern generator System window (see Figure 2–19) graphically represents the pattern generator configuration. The modules are placed in slot order by the application. This window functions as the main application window and provides a familiar starting point for Tektronix logic analyzer users.

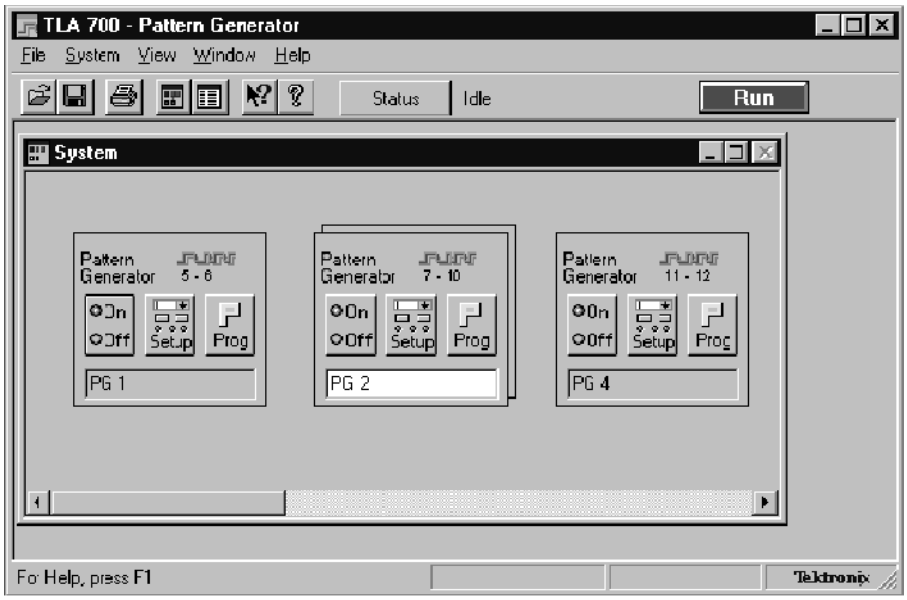


Figure 2- 19: System window

You can perform the following tasks in the System window:

- Enable and disable modules by clicking their On/Off buttons.
- Open Setup and Pattern windows by clicking the module icons. To select a module without opening its window, click inside the icon.
- Save and load files containing setup and pattern information from the File menu.

Setup Windows

Before you can generate data, you must first configure the modules using the module Setup windows. Each pattern generator module has its own set of Setup windows. Click the Setup icon to open the Module Setup window and then select the individual setup windows from tabs at the top of the windows.

Module Setup Tab

Use the Module Setup tab to set various parameters pertaining to the current pattern generator module such as clocking and the run modes. Figure 2–20 shows an example of the Module Setup tab.

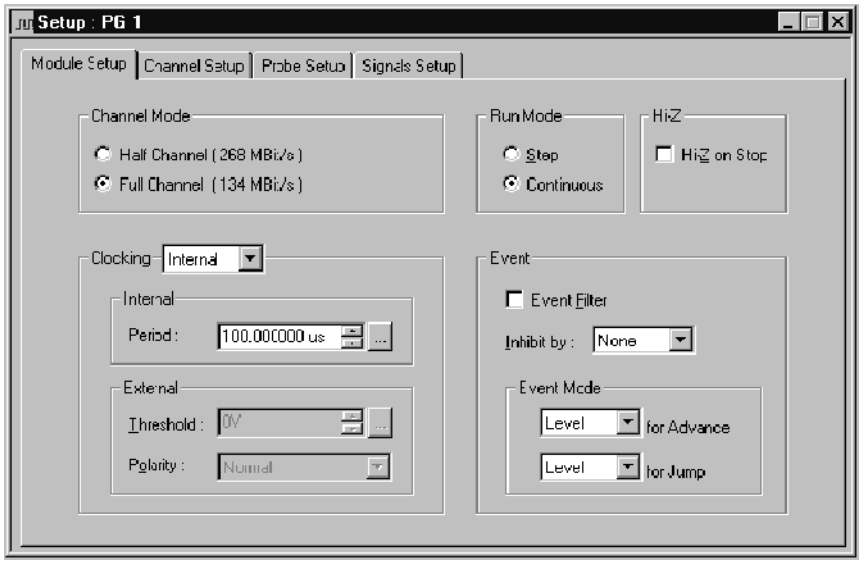


Figure 2-20: Module Setup tab

Channel Setup tab

Click the Channel Setup tab to define the individual channel setups. The Channel Setup tab is similar to the LA Setup window. It shows all of the probe and channel groupings. You can edit the groups as necessary to fit the needs of your application.

Probe Setup tab

Click the Probe Setup tab to specify probe details such as the output threshold voltage and inhibit information. The Probe Setup window shows the detailed settings of all probes connected to the pattern generator module.

Signal Setup tab

Click the Signal Setup tab to define the input and output signals. Use these signals together with the Program window settings to control the pattern generator program.

Program Window

Use the Program window to develop the pattern generator program. The Program window provides access to the Block tab, Sequence tab, Subsequence tab, and the Event tab. Use the Program windows to create the data vectors and the pattern generator program flow.

Block Tab

Use the Block tab to create blocks of data vectors. The Block tab lets you view all of the data blocks in a single window without having to view the individual data vectors. You can assign meaningful names to each data block and then use those data blocks in the Sequence tab to create the pattern generator program.

Use the pattern generator Listing and Waveform windows from the Block tab to create the data vectors that you want to send to the target system. Figure 2–21 shows an example of the Block tab.

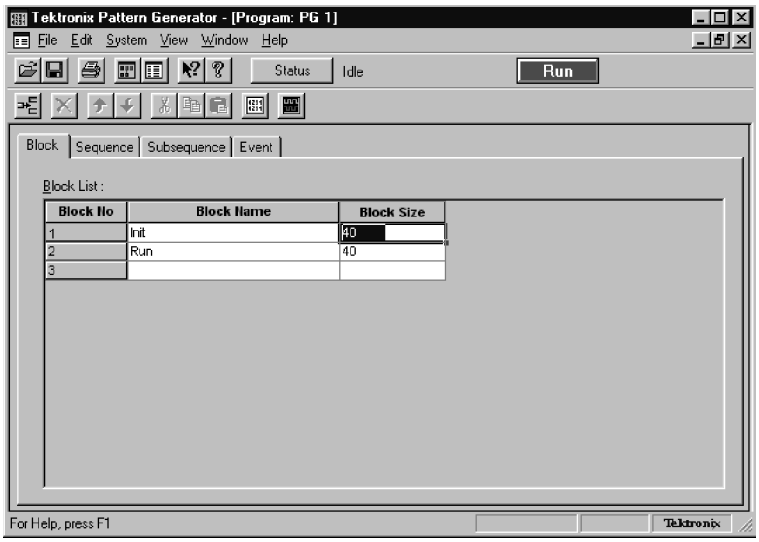


Figure 2-21: Block tab

Sequence Tab

Use the Sequence tab to provide a high-level view of the pattern generator program. Use the data blocks that you created in the Block tab together with subsequences, signals, and events to create the pattern generator program. Use labels with each sequence to help control the flow of the pattern generator program.

Subsequence Tab

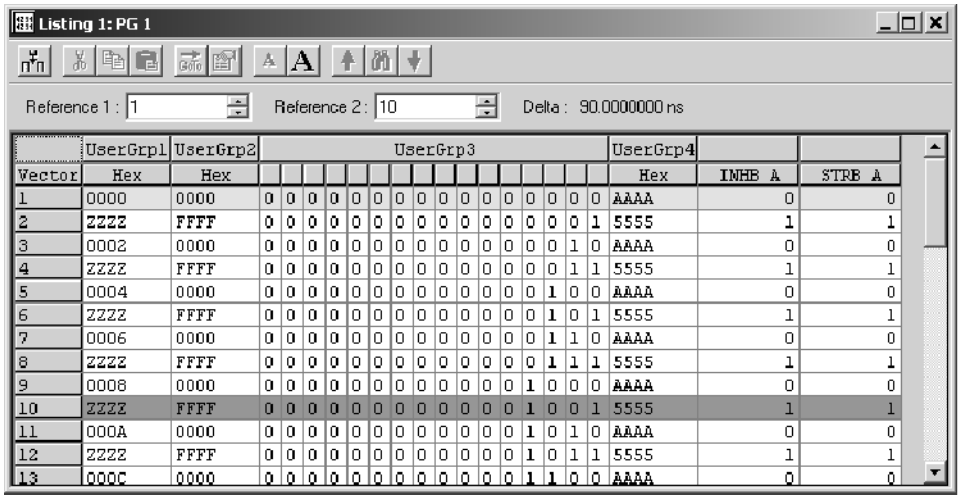
Use the Subsequence tab to create subsequences or macros that contain tasks that you may not want visible as part of the high-level sequence flow. You may want to create a subsequence that repeats a series of data blocks before returning control to the main program. You can use meaningful names with each subsequence.

Event Tab

Use the Event tab to define how to use external signals with the pattern generator program. You can logically AND and OR the probe event inputs to provide program control.

Listing Windows

Use the pattern generator Listing window to edit the vector data. You can open multiple listing windows to easily move selected data from one block to another by copying and pasting the vector data. You can define the radix to help you set up the vector data. For example, Figure 2–22 shows UserGrp3 with binary data as compared to the other user groups which show their data in Hexadecimal.



	UserGrp1	UserGrp2	UserGrp3																UserGrp4		
Vector	Hex	Hex																	Hex	INHB A	STRB A
1	0000	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AAAA	0	0
2	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	5555	1	1
3	0002	0000	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0		AAAA	0	0
4	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1		5555	1	1
5	0004	0000	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0		AAAA	0	0
6	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1		5555	1	1
7	0006	0000	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0		AAAA	0	0
8	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1		5555	1	1
9	0008	0000	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0		AAAA	0	0
10	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1		5555	1	1
11	000A	0000	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0		AAAA	0	0
12	ZZZZ	FFFF	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1		5555	1	1
13	000C	0000	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0		AAAA	0	0

Figure 2-22: Listing window

Waveform Window

Use the Patten Generator Waveform window to edit the vector data. This method may be useful when you want to see the timing relationship between the pattern generator channels. Figure 2–23 shows an example of a Waveform window.

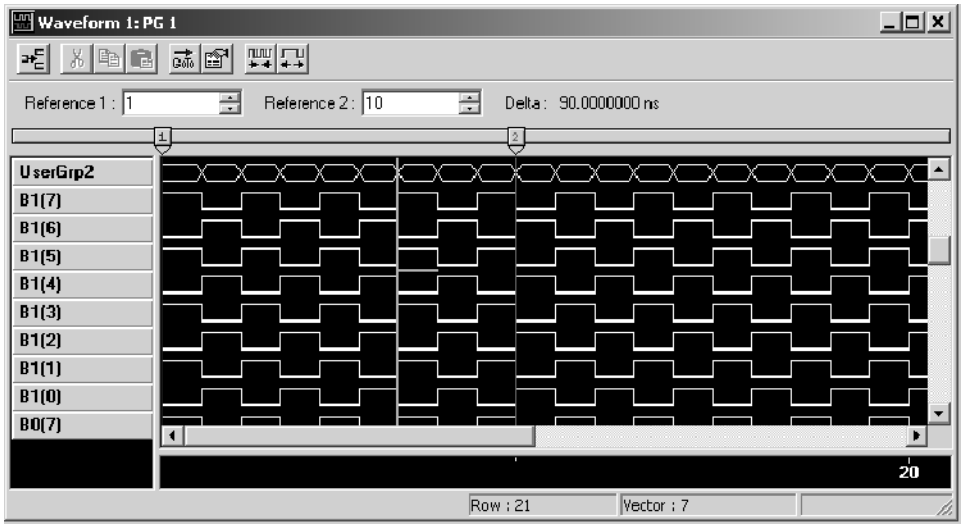


Figure 2-23: Waveform window

PG Run Properties Dialog Box

The Pattern Generator (PG) Run Properties dialog box selections determine if the logic analyzer Run button will start and stop the pattern generator (PG) modules. Access the dialog box by clicking PG Run Properties from the System menu under the TLA application See Figure 2–24.

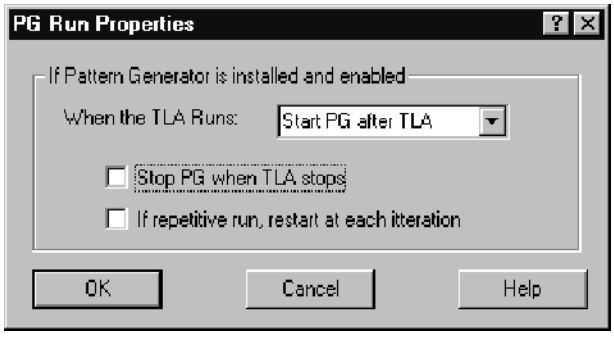


Figure 2-24: Pattern Generator Run Properties dialog box

Operating Basics

This section provides an overview of logic analyzer concepts and some of the features of the Tektronix Logic Analyzer.

To acquire and display signals from the target system, the logic analyzer must perform a complex series of actions. For the most part, these actions are transparent. However, it can be helpful to understand how the logic analyzer operates. This knowledge can influence how you approach a logic analysis problem.

Sampling and Digitizing a Signal

Acquisition is the process of sampling the input signal, digitizing it to convert it into digital data, and assembling it into a waveform record. The order and method of accomplishing these functions is different between the LA and DSO modules.

The LA module converts incoming data into ones and zeros using a comparator with a user-selectable threshold voltage. If the incoming signal is above the threshold voltage, it is converted to a one; if it is below the threshold voltage, it is converted to a zero. After digitizing the data, the LA module samples it at regular time intervals. The sampled and digitized points are stored in memory along with corresponding timing information. (See Figure 2–25.)

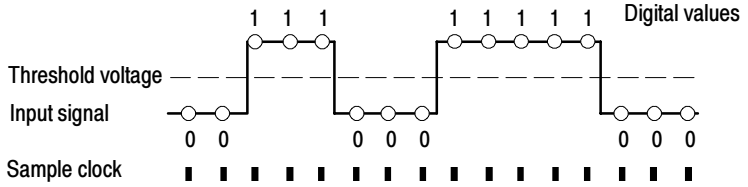


Figure 2-25: Acquiring a digital signal (LA module)

The DSO module samples the voltage level of the signal at regular intervals, and then converts the sampled analog data into 8-bit digital values (see Figure 2–26). The sampled and digitized points are stored in memory along with corresponding timing information.

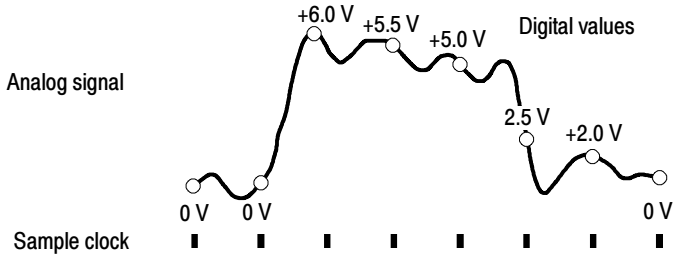


Figure 2-26: Acquiring an analog signal (DSO module)

LA Module Block Diagram

The LA module is the key element of the instrument. Functionally, the LA module can be divided into several blocks, as shown in Figure 2–27. Refer to the figure as you read about the functional blocks.

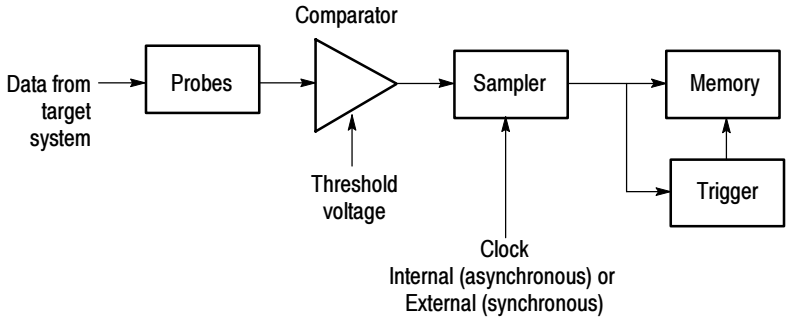


Figure 2-27: Block diagram of the LA module acquisition and storage

Clocking

Clocks control when data is sampled. The point at which you sample data has a great deal to do with the type and quality of data you acquire. For the LA module, there are two primary approaches to clocking, external (synchronous) clocking and internal (asynchronous) clocking. Generally you use external clocking for listing data and internal clocking for waveform data.

External (Synchronous) Clocking. This clocking mode is called an external or synchronous clock because the clock is external to the logic analyzer, and is synchronized to the target system. External clocking is the best choice when you are primarily interested in state aspects of the data.

The signal you chose as the external clock to the logic analyzer should be the signal that controls the activity of the other signals you want to observe. For example, to observe the output states of a counter chip, use the clock input to the counter chip to act as the external clock source to the logic analyzer. With this setup, each clock pulse to the counter chip can also be used to clock data from the counter output lines into the logic analyzer. As another example, to record the data being written to a latch, you could use the load signal to the latch as the external clock source to the logic analyzer.

Internal (Asynchronous) Clocking. Much activity can occur in the target system between system clock signals. Using the LA module's internal (asynchronous) clock, you can view all activity in the target system, not just the data available at the target system clock signal.

Internal clocking is the best choice when you are primarily interested in the timing aspects of the data. It is important to note, however, that the value of internal clocking is not limited to displaying waveforms. If you want a detailed picture of data activity both during and between state changes, use internal clocking. For example, internal clocking allows you to acquire and display glitch information in either the Waveform or Listing windows.

Acquiring Data

When you start an acquisition, the logic analyzer begins sampling data from the probes. Then, each time a sample clock occurs, data is sampled. Sampled data is sent to the trigger functional block and to the main memory.

Triggering and Storage Qualification

The trigger program looks at sampled data for specific events and then takes a specified action. The trigger program can look for events such as data values, data ranges, or signals from another module. You can also use internal counters to trigger when the counter reaches a specified value.

When the trigger condition is satisfied, the LA module enables a post trigger delay counter to allow the post trigger portion of the acquisition memory to fill before stopping acquisition. You can also indicate a prefill portion of acquisition memory that must be met before the trigger state machine can store post trigger data.

The trigger function block includes storage qualification that looks at sampled data. If the storage conditions are met, a storage qualifier signal enables sampled data to pass into the acquisition memory as qualified data. Any unqualified data samples are excluded.

Storing Data in Memory

The acquisition memory works like a circular buffer, storing every qualified data sample until the entire memory is full. After that, each new data sample overwrites the oldest existing sample. This process continues until the trigger event is found and the post trigger delay counter reaches the specified value (based on the trigger position selection), which stops acquisition. During acquisition, you can monitor the progress of the data storage process using the Status Monitor.

After storing the data you can display the acquired data in the Listing or Waveform data windows.

DSO Module Block Diagram

The DSO module adds analog analysis capability to the instrument. Functionally, the DSO module can be divided into several blocks, as shown in Figure 2–28. Refer to the figure as you read about the functional blocks.

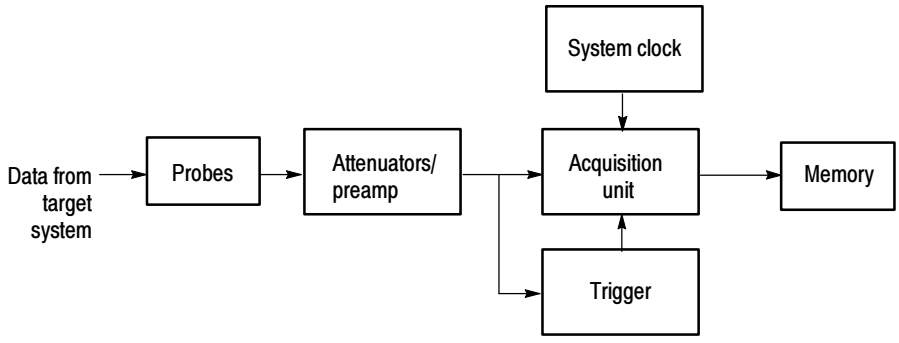


Figure 2-28: Block diagram of the DSO module acquisition and storage

Probes

A probe interface detects the attenuation factor of each probe. This information is used to set the vertical scale.

Acquiring Data

When you start an acquisition, the DSO module begins sampling data from the probes. Each time a sample clock occurs, data is sampled. Signals from the probes go to the attenuators/preamp functional block, which is responsible for input coupling, termination, bandwidth, offset, and full scale range. The DSO module always uses internal clocking.

From the attenuators/preamp, signals are sent to the acquisition unit and trigger functional blocks.

Acquisition Unit

The acquisition unit functional block samples the input signals and converts them to digital data.

Triggering

The DSO trigger looks at sampled data for a specific event. The trigger can look for various types of events, such as glitches, setup and hold violations, runt pulses, or signals from another module.

When the trigger event is found, the DSO module enables its post trigger delay counter to allow the post trigger portion of the acquisition memory to fill before stopping acquisition. When triggered, the DSO module performs its specified trigger action (for example, triggering all modules).

Storing Data in Memory

The acquisition memory works like a circular buffer, storing data samples until the entire memory is full. After that, each new data sample overwrites the oldest existing sample. This process continues until the trigger occurs and the post trigger delay counter reaches the specified value (based on the trigger position selection), which stops acquisition. During acquisition, you can monitor the progress of the data storage process using the Status Monitor.

After storing the data you can display the acquired data in the data windows. In the Waveform window, the data is shown as analog waveforms. In the Listing window, the data is shown as a series of voltage values.

Pattern Generator Module Block Diagram

The pattern generator module adds pattern generator capability to the logic analyzer. You can generate specific data patterns to a target system and then use the logic analyzer to evaluate the resultant data from the target system.

The pattern generator module functionality can be divided into blocks as shown in Figure 2–29. Refer to the figure as you read about the functional blocks.

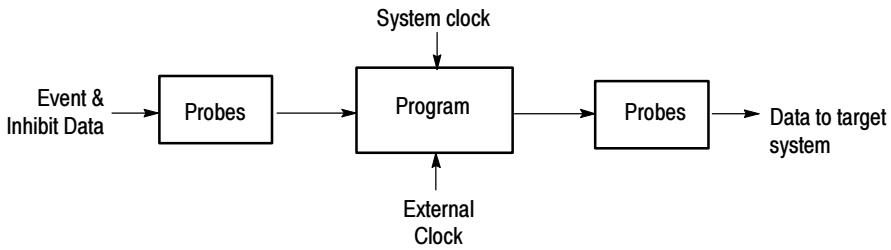


Figure 2-29: Block diagram of the pattern generator module

Probes

The probe interface serves two purposes: to detect event and inhibit information and to output data to a target system. In addition to sending pattern generator data to the target system, the probe also sends clock and strobe information.

You can connect up to four probes to a single module. Each probe supports either 8 or 16 channels.

Pattern Generator Program

The pattern generator program is the heart of the pattern generator module. You can create blocks of data vectors to work together to create complex pattern generator programs. The program uses external and internal events to determine specific actions such as loops and branches to other data blocks. The program can be controlled by an internally selected clock or by an external clock through a front-panel BNC connector.

Use the Sequence Definition page of the Program window to set up and define a sequence events that make up the pattern generator program. Each sequence line determines how the pattern generator will use blocks of data that you define in the Pattern Generator Listing or Waveform window. You can set up the program to wait for specific events or signals and then jump to a different sequence when an event is either true or false.

You can also set up the pattern generator to single step through programs and output a single set of vectors with each clock cycle. This is useful for trouble-shooting or debugging setups.

Logic Analyzer Physical Model

Physically, the logic analyzer is made up of two main parts: the modules and the mainframe. Figure 2–30 illustrates the relationship between the logic analyzer and its subparts.

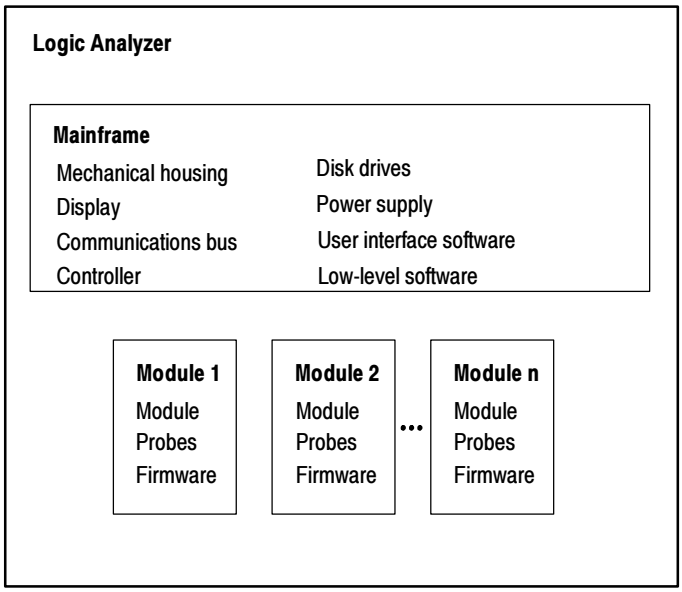


Figure 2-30: Logic analyzer physical model

Logic Analyzer Conceptual Model

Conceptually, the logic analyzer is made up of two main parts: the modules and the system. From the operational perspective, a module encompasses the setup, trigger, and data associated with the physical logic analyzer, DSO module installed in the logic analyzer, or the external oscilloscope that is physically connected to the logic analyzer. See Figure 2–31. The system refers to the setup and data for the whole logic analyzer, including all the modules.

Some actions occur at the module level, some at the system level. For example, you can save either module or system files. When you save a module, you save all the setup and trigger information for that module. (You also have the option of saving the data for that module.) When you save a system, you save all the setup information for the system, including data window display settings, and all the module information, as well.

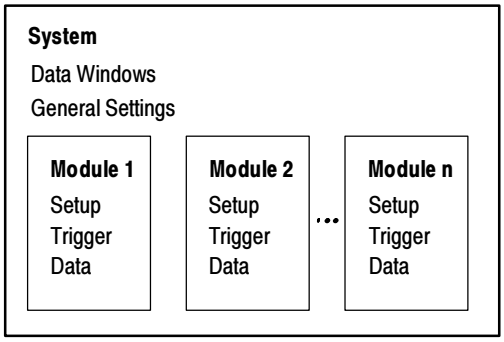


Figure 2- 31: Logic analyzer conceptual model

Intermodule Interactions and Time Correlation

Each module has its own setup, trigger, and clocking functions. (LA modules may include microprocessor support as part of their setup.) Each module also acquires and stores its own data.

When you start an acquisition, all modules start acquiring data together. (Exceptions are when one module has been programmed to arm another or when a module has been turned off.) Modules stop acquiring data individually, according to their trigger programming. You also have the option of setting the logic analyzer to operate in repetitive mode, in which the modules acquire data and update the data windows continually until you manually stop the acquisition.

Modules readily communicate with one another by means of their trigger programs. You can specify functions such as the following:

- Trigger all modules (system trigger)
- One module arms another
- Modules respond to events declared by another module (internal signals)

After the modules have captured and stored data, you can view the data in a Listing or Waveform window. All data is time-correlated in the display, regardless of its source. Due to the precise time stamp information stored with the data, and the tightly-integrated communications between modules, the logic analyzer interleaves data acquired from various sources. Because time stamp information is always stored with the data, you can also compare saved data and current data with no loss of accuracy.

MagniVu data is also time-correlated with regular data. Because MagniVu data is always present, you can easily compare a normal acquisition with the MagniVu counterpart.

Listing-Data Concepts

In many cases, you will use the logic analyzer to observe the data flow in the target system. The data recorded by the logic analyzer can be displayed in a listing format, as shown in Figure 2–32.

Listing data is a table of sequential operations performed by the target system. In the Listing window, each data sample is displayed sequentially. Because each data sample includes time stamp information, it is a straightforward process to display acquisitions from multiple data sources. Samples from all specified data sources are interleaved in chronological order. For clarity, each line in the table represents a single data sample from a single data source.

You control the presentation of the data by selecting the display radix of the columns. You can also make other format selections such as font size, color, and column width.

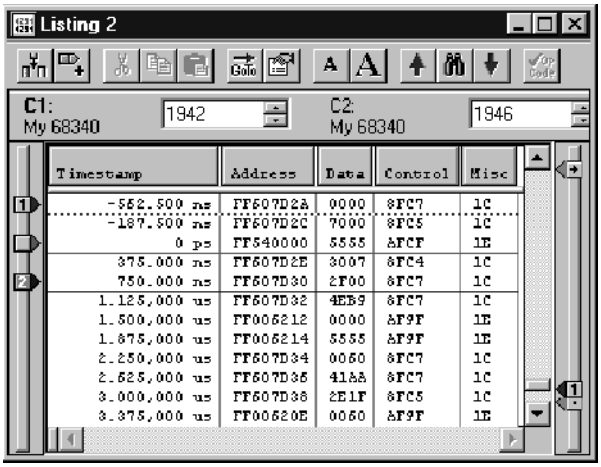


Figure 2-32: Listing data

You can include data acquired by the DSO module in the Listing window. The Listing window in Figure 2–33 shows DSO module Channel 1 data as discrete voltage levels. As with any module, the data samples from the DSO module are time-correlated with the other data and appear on separate lines.

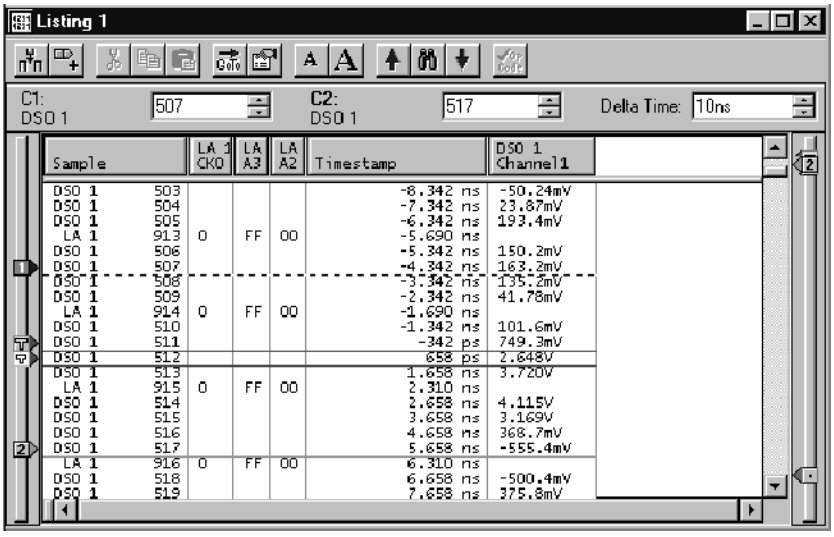


Figure 2- 33: Listing window with analog data

Microprocessor Support

For microprocessor applications, the acquired data can be disassembled back into the assembly language mnemonics used by a particular microprocessor. Figure 2–34 shows an example of the disassembled mnemonic display format. Microprocessor support usually requires a special input probe dedicated to a specific microprocessor.

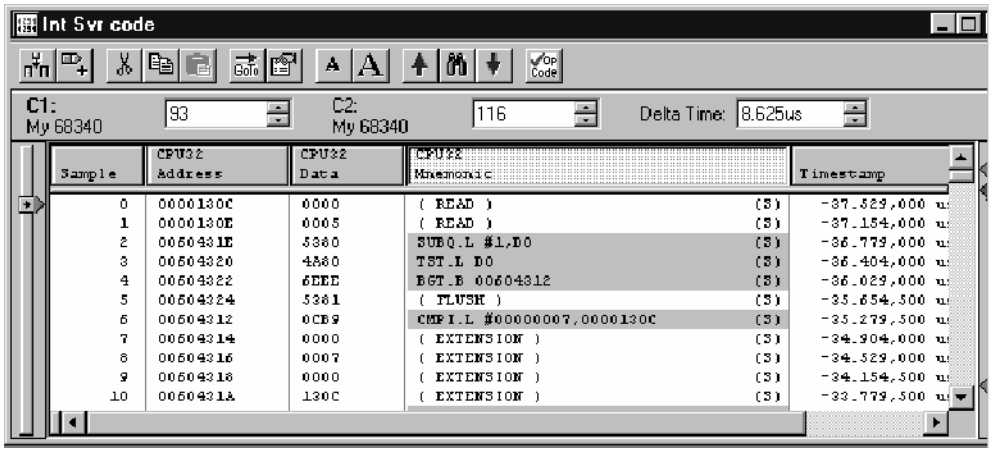


Figure 2- 34: Listing data using a microprocessor support package

The logic analyzer provides support for a wide variety of different microprocessors. Microprocessor support packages include the software, probe adapters, and documentation.

High-Level Language (Source Code) Support

You can correlate the high-level language (HLL) source code that you wrote with your code as it was executed on your target system and acquired by the logic analyzer. The correlation is based on symbolic information that is extracted from your object file or load module. You configure the logic analyzer to access your source files.

You can step through each executed source statement in the Source window and view the results in a correlated Listing window. You can also set user-defined marks as break points within the code and then trace the execution of the code between the marks. Figure 2–35 shows an example of viewing source code in a Source window, while Figure 2–36 on page 2–38 shows the actual acquired data in an associated Listing window.

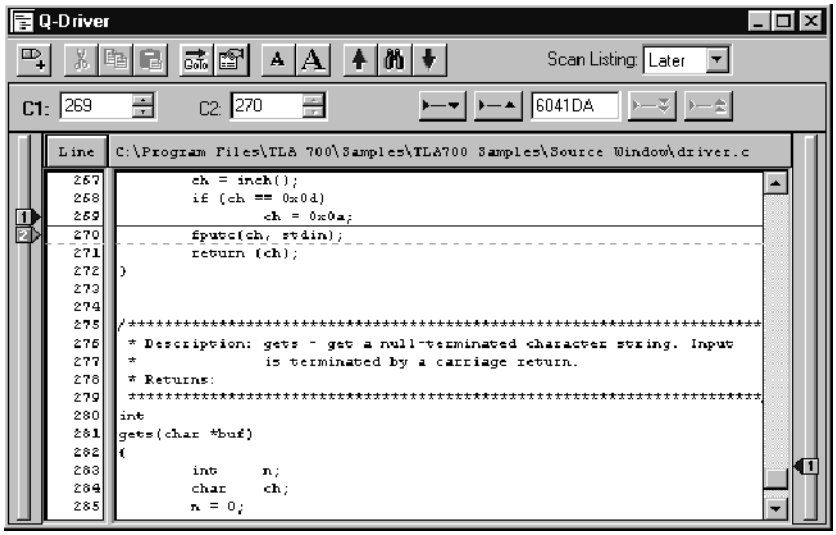


Figure 2-35: High-level source code

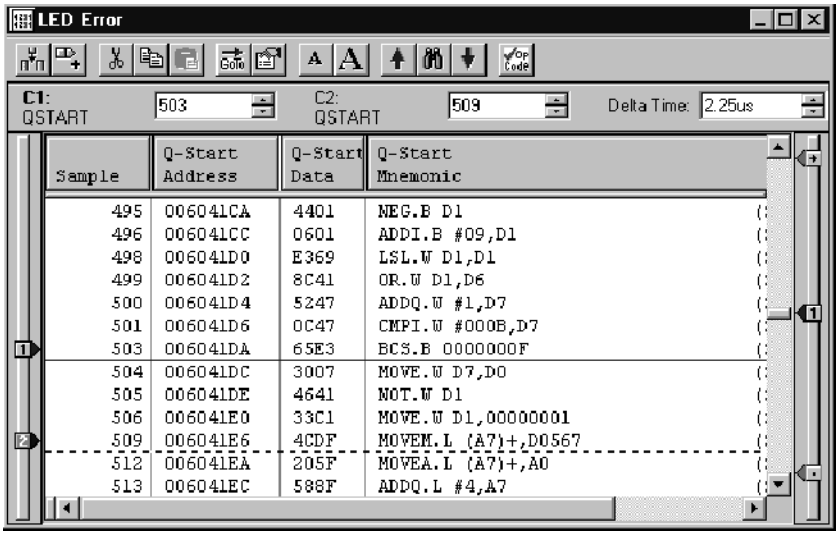


Figure 2- 36: Source code viewed as acquired data

The LA module supports a wide variety of object files including IEEE695, OMF51 OMF86, OMF286, OMF386, OMF166, COFF, Elf/Dwarf1 and Dwarf2, Elf/Stabs, and the TLA Symbol File (TSF) format (a text format). Refer to *Appendix B: TLA Symbol File Format*.

Waveform Data Concepts

You can use the logic analyzer to observe the timing relationships between signals by displaying the recorded signal activity as a series of waveforms in the Waveform window. Figure 2–37 shows waveform data from an LA module.

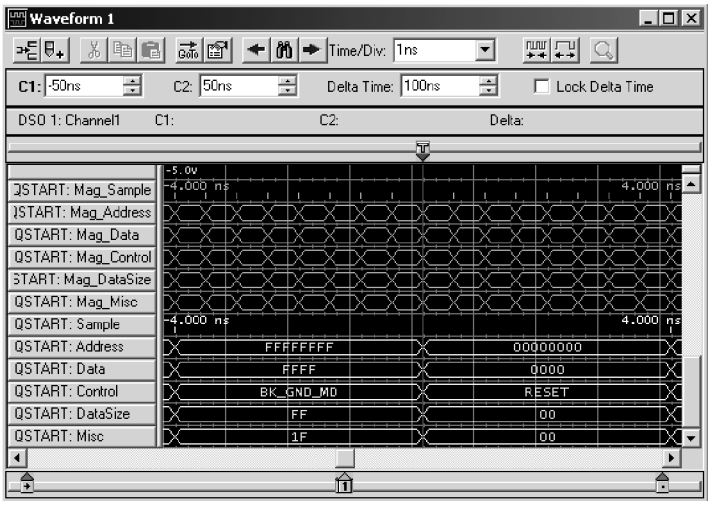


Figure 2-37: Waveform data

Each waveform is initially displayed in a separate track, but all waveforms are time-aligned horizontally and displayed in the same time per division. Again, the inclusion of time stamp information with the stored data samples makes it a straightforward process to display time-correlated acquisitions from multiple data sources.

You control the horizontal scale of the acquired data in the display. (You do not, however, change setup parameters by changing settings in the waveform display.) You can also make other format selections such as channel group radix, waveform color, and track height. To show when the logic analyzer sampled the data, you can add Sample using the Add Waveform tool bar button.

When viewing logic analyzer data, you can view the data as individual channels. You can also display the logic analyzer data in groups of channels known as busforms. Use the busforms to display when data changes with respect to clock or control signals. Another method of displaying logic analyzer data is to overlay waveform channels. Use overlay waveforms to visually compare two or more waveforms at the same time.

When you are interested in displaying the value of a group of channels over a period of time, you can use magnitude mode. For example, using magnitude mode, you can view the channels connected to a 16-bit digital counter. The magnitude waveform appears as a sawtooth waveform as the counter values increment from the minimum value (00) to the maximum value (FF).

LA Module Versus DSO Waveforms

A logic analyzer waveform appears to have zero-length rise and fall times. This is because the logic analyzer is recreating the waveform from the samples stored in its memory, which are either ones or zeros.

No electronic signal is perfectly digital in nature; there is always some analog component. Consider a fast-rising pulse with ringing on the front edge, or glitches that can occur in a noisy circuit. If you suspect problems caused by analog signal characteristics (such as signal voltages higher or lower than specified voltage levels, or slow transition times), use a DSO module to observe the voltage characteristics of the signal. Figure 2–38 shows where the DSO module captured a runt pulse that was below the logic analyzer's threshold.

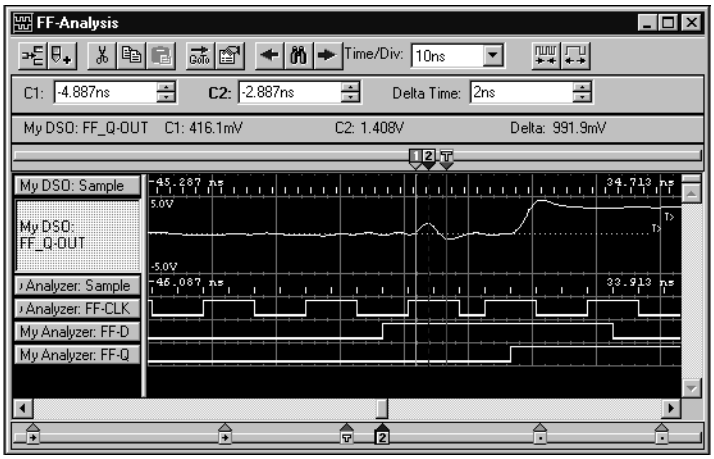


Figure 2-38: Using the DSO module to capture a runt pulse

Sampling Resolution

The accuracy of the waveform re-created from the sampled data depends on the sample clock rate used to record the incoming signals. This is due to the fact that the waveform re-created by the logic analyzer is based on the sampled signals stored in its memory. If the sample clock rate is too slow, the recorded data will produce an inaccurate display. Figure 2–39 shows how the sample clock rate can affect an LA waveform.

Insufficient DSO module sampling resolution can result in aliasing. For information about aliasing, see page 2–42.

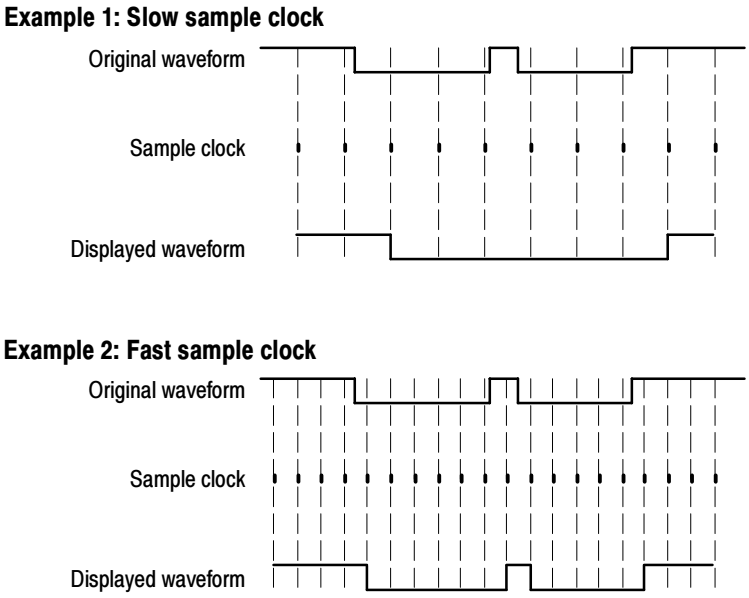


Figure 2-39: LA module sampling resolution

Signal Resolution and Signal Duration

There is an important trade-off between the resolution of the recorded signal and its duration in terms of elapsed time. Because the total number of samples that can be recorded by the logic analyzer is fixed by the depth of the logic analyzer's acquisition memory, increasing the sample clock rate provides better signal resolution at the expense of reducing the duration of the captured signal. That is, a faster sample clock rate will record a smaller portion of the signal, but with better resolution; or, you can trade channels or depth to maintain higher resolution.

It is important to remember that you have two additional tools for the TLA7Lx/Mx/Nx/Px/Qx modules and three additional tools for the TLA7Axx modules to offset the signal resolution/signal duration relationship:

- By using the MagniVu data feature available for all modules, you can view high-resolution data centered about the LA module trigger. This allows you to zoom in on the data of particular interest while still maintaining visibility of a more extended signal duration.
- By using Internal 2X Clocking mode available for all modules, you can trade one half the channels for twice the resolution and twice the memory depth. The 2X Clocking mode is only available with the main timing (not with the MagniVu data feature).
- By using Internal 4X Clocking mode available only for TLA7Axx modules, you can trade three-quarters of the channels for four times the speed and memory depth. The 4X Clocking mode is only available with the main timing (not with the MagniVu data feature).

Preventing Aliasing

Under certain conditions, an analog waveform can be aliased on screen. When a waveform aliases, it appears on screen with a frequency lower than the actual waveform being input or it appears unstable. Aliasing occurs because the instrument cannot sample the signal fast enough to construct an accurate waveform record. (See Figure 2–40.)

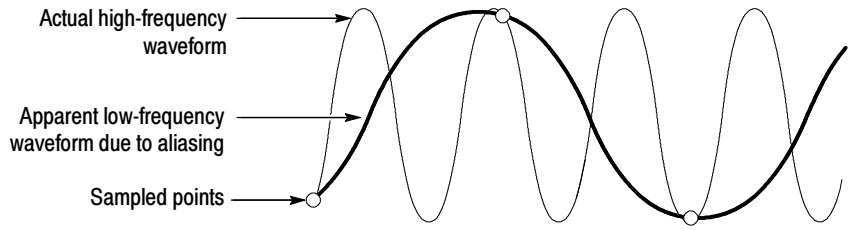


Figure 2- 40: Aliasing

To check for aliasing, increase the sampling rate (decrease the clock sample period) in the module Setup window. If the shape of the displayed waveform changes drastically or becomes stable at a faster clock sample period setting, your waveform was probably aliased.

Although the principles of sampling theory define a minimum sample rate of 2X, a good rule of thumb is to choose a sample clock rate five times faster than the speed of the fastest signal being measured. A faster sample clock rate results in a more accurate reconstructed waveform.

Displaying Waveforms

Waveforms are rarely displayed at an exact one sample point per pixel. Waveforms are usually displayed in a compressed or expanded format. As a general rule, waveforms are compressed when the time per pixel is greater than the time per sample clock. Waveforms are expanded when the time per pixel is less than the time per sample clock.

For compressed DSO waveforms, the display shows the lowest and highest point that occupy a given pixel column joined by a vertical line. For expanded waveforms, the display points between the actual sample points are calculated.

For expanded DSO waveforms, *Sin(x)/x interpolation* computes the display points between the actual values acquired.

High-Speed Timing

The LA module provides high-speed timing support through MagniVu data. The MagniVu data is stored in a separate memory that is parallel to the main memory. All data from the sampler goes directly to the MagniVu memory. The MagniVu memory also works like a circular buffer. Unlike the acquisition memory, the MagniVu memory does not qualify data storage through the trigger function block.

MagniVu data is continuously acquired on all channels at the fastest sample rate of 500 ps for TLA7Lx/Mx/Nx/Px/Qx modules and 125 ps for TLA7Axx modules. Like normal acquisition data, MagniVu data can be displayed in the Listing or Waveform data windows. For TLA7Lx/Mx/Nx/Px/Qx modules, the MagniVu data is centered on the LA module trigger in the data window. For TLA7Axx modules, the trigger position for MagniVu data is variable; you control the MagniVu trigger position by a set of controls in the advanced toolbar. See *MagniVu Data* on page 3–106 for additional information.

Detecting Violations

One of the logic analyzer's most useful features is its ability to detect and trigger on both signal glitches and setup and hold violations.

A glitch is a signal that makes a transition through the threshold voltage two or more times *between* successive acquisition samples. Because glitches are often signal transitions that occur intermittently, they can cause circuit malfunctions that are extremely difficult to diagnose.

Although you could try using a very fast sample clock rate to ensure that you never miss any glitches, a better solution is to use the glitch-detection feature. The logic analyzer can trigger on a glitch, either alone or in combination with other signal events. This capability is useful for catching intermittent glitches that might not occur very often or appear only when a particular operation is taking place.

You can capture noise spikes and pulse ringing using the glitch capture feature. Figures 2–41 and 2–42 show data captured by triggering on a glitch. In the Waveform window, a glitch captured by an LA module is indicated by a band of color. (See Figure 2–41. For clarity, an arrow identifies the glitch in the figure.)

A setup and hold violation is a data signal that transitions *within* the setup and hold time period. You can identify setup and hold violations by looking at each clock edge and reviewing all relevant data signals. However, it is more efficient and reliable to use Setup/Hold triggering to identify violations.

You must select the correct clocking mode to use either the glitch detection or the setup and hold violation features. Choose internal clocking to use glitch detection; choose external clocking, source synchronous clocking, or custom clocking to use setup and hold detection. For information on glitch storage, see Selecting the Acquisition Mode on page 3–17.

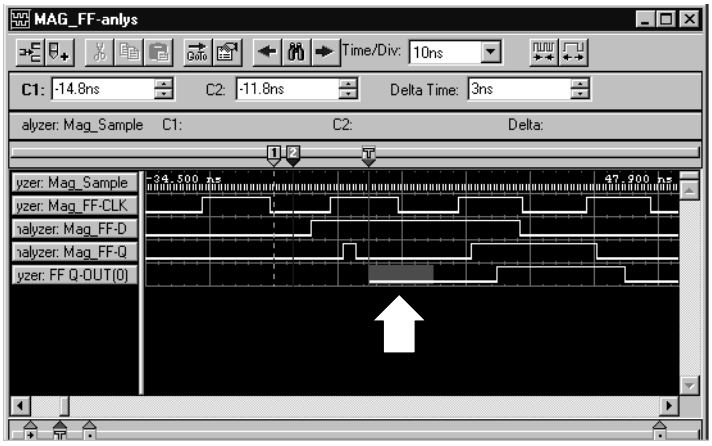


Figure 2- 41: LA module triggering on a glitch

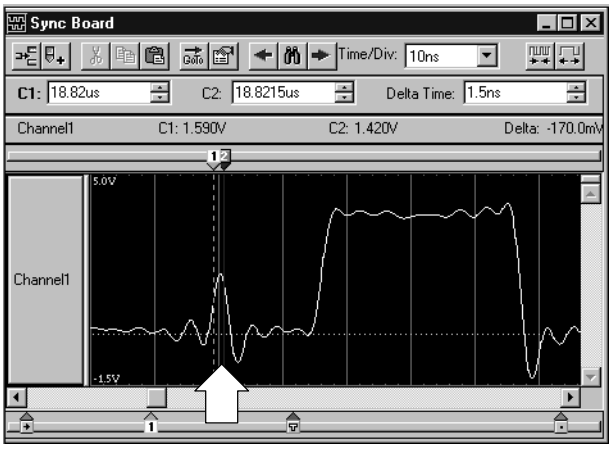


Figure 2- 42: DSO module triggering on a glitch

Performance Analysis Concepts

For performance analysis applications, you can use the Histogram window to view the performance of your software. The actual data is displayed as horizontal bars in a histogram.

You may want to use the Histogram window to see which one of your software routines is taking up most of the CPU time. Or, you can use the Histogram window to measure the amount of time used by a particular subroutine. You can use a symbol file to view each of the routines by name.

Figure 2–43 shows an example of the Histogram window where the StopLite routine is taking up most of the computer resources.

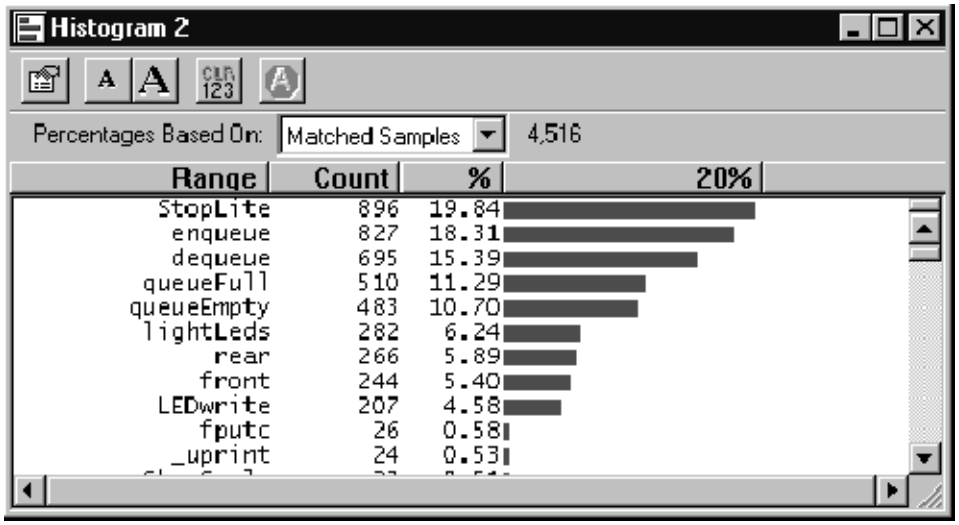


Figure 2-43: Viewing the performance of code with a Histogram window

Comparing Acquired Data Against Saved Data

You can use the LA module to compare acquired data against saved reference data. Use the LA Setup menu to define the data channels that you want to use during the compare operations. You can further define the number of samples that you want to compare as well as data alignment offset.

In the Listing and Waveform windows, you can use color to quickly identify the compared data. You can set up one color to show where the acquired data does not equal the reference data. You can use another color to show where the acquired data equals the reference data.

Figure 2–44 shows a Listing window during a memory compare operation. Notice that some of the data under the LA 2 A2 column appears in a different color, indicating that there were differences between the acquired data and the reference data.

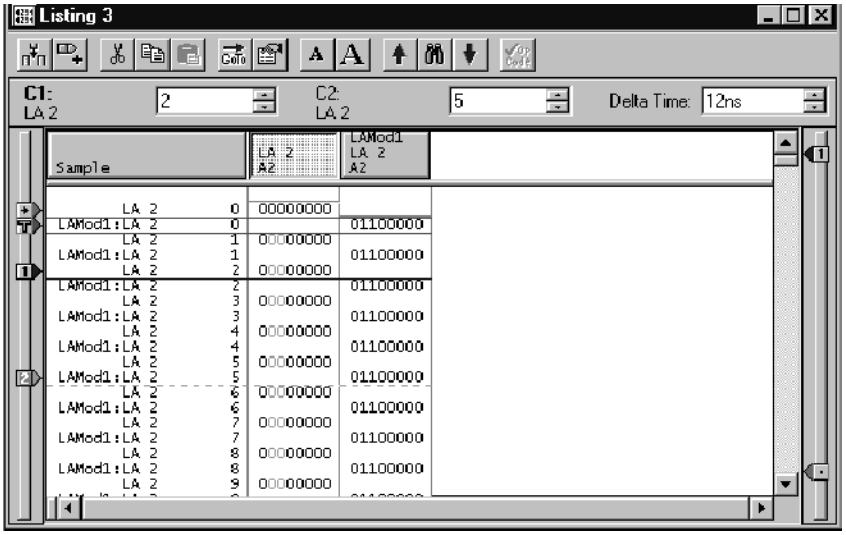


Figure 2- 44: Using color to show memory differences in a Listing window

Repetitive Acquisitions

Use the Repetitive acquisition features of the logic analyzer to automate repetitive and time-consuming tasks. For example, you can specify the number of times that you want the logic analyzer to acquire data. With each acquisition, you can save the data to a file for analysis. You can also set up the logic analyzer to open a file or execute a program when all of the acquisitions have been completed.

You can set up the LA module to acquire and compare the acquisition data to known reference data. The LA module can continue acquiring data until there is a mismatch between the acquisition data and the reference data.

Figure 2–45 shows an example of such a setup where the acquired data is exported to a file for each acquisition. When a data-mismatch occurs the logic analyzer stops acquiring data and exports the data to a file. The faulty data can now be analyzed by another application.

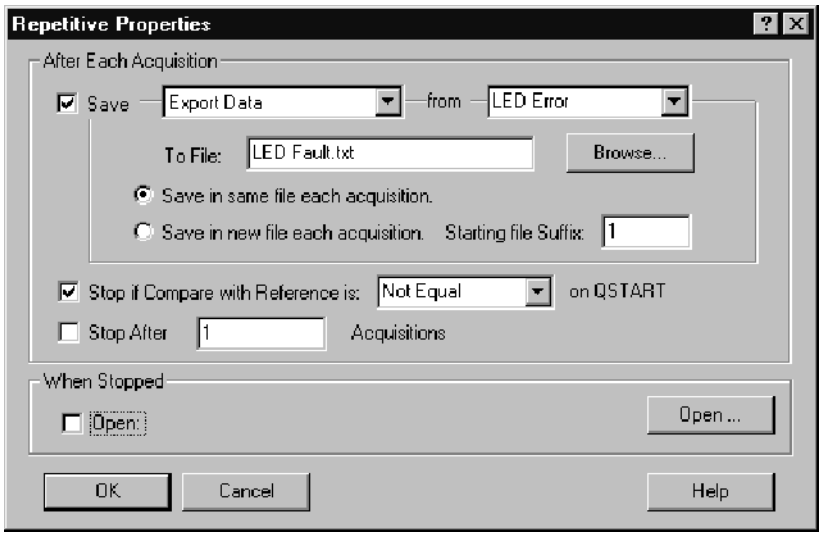


Figure 2-45: Defining repetitive setups

Symbol Support

Symbols simplify tasks, such as setting up triggers or identifying specific values within the data. When you program a trigger or view data, it is cumbersome to remember which numeric channel group values correspond to particular machine instructions or code modules. The logic analyzer makes this task more manageable by allowing you to assign symbolic names or mnemonics to group values.

For example, assign the symbol WRITE to the control bus event that causes the target system to write to a memory location. Then, if you want to trigger when a write cycle occurs, enter WRITE in the trigger program in place of the actual data value. You can also choose to have WRITE appear in the Listing window for quick identification of the instruction.

In Figure 2–46, the example shows a trigger program that uses the symbol BUS_ERROR as part of the trigger clause.

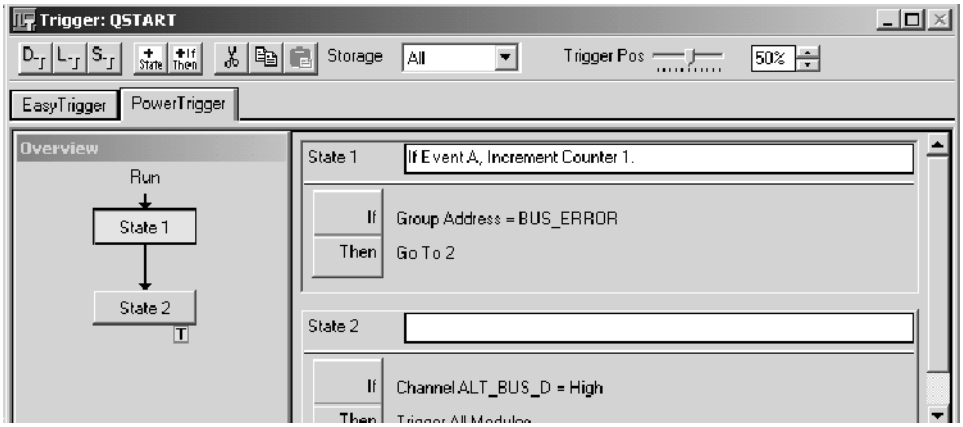


Figure 2- 46: Using symbols in a trigger program

You can use symbol files with a Source window and an associated Listing window to track the execution of source code. The symbol file provides the information to associate a line of source code to an address in a Listing window. When you move a cursor in one window, the symbol file provides the necessary information to move the cursor to the correct location in the other window.

Often, the application software will define symbols for you. For example, when you load a microprocessor support package, symbols are also loaded (typically, to the control group). These symbols represent data values that correspond to bus cycle types. Other software applications produce range symbol files which you can load (typically, these files are loaded to the address group).

Symbol Files

To use symbols, you must first load or create one or more symbol files that define the symbols. Symbol files contain symbol names and their associated data values. You can use symbol files created by another application, edit symbol files from other applications, or you can create your own symbol files using a text editor.

Each entry in a symbol file consists of an alphanumeric symbol name with its associated numeric value or range of values. After you create a symbol file, you can specify the symbol file for the appropriate channel group in the Waveform or Listing window, use symbolic names as a substitute for numeric values in the Trigger and data windows, and use symbols for tracing source code in a Source window.

Symbol files perform like look-up tables. For example, if the address of a printer I/O port is at address F734BC, you can define a symbol, printer-port, that corresponds to that value. Then, in the Trigger window, you can specify the symbol name as an event in the trigger program and cause the module to trigger when printer-port (F734BC) appears on the address bus. You can also specify the symbolic display radix for the address channel group and the symbol name printer-port will show in the Listing window every time F734BC appears on the address bus.

Symbol Types. Two main types of symbol files are possible: pattern symbol files and range symbol files. Range symbols can be further divided into three different categories: functions, variables, and source code (source). Table 2–1 shows the different types of symbols and the windows where they are commonly used.

Table 2-1: Using symbols in logic analyzer windows

Window	Pattern symbols	Range symbols		
		Functions	Variables	Source code
Listing	Yes	Yes	Yes	Yes
Waveform	Yes	Yes	Yes	Yes
Histogram	No	Yes	Yes	No
Source	No	No	No	Yes
LA Trigger	Yes	Yes	Yes	Yes

Pattern Symbols. Pattern symbols consist of data patterns up to 32 bits. Each bit in a pattern symbol can be 0, 1, or X (don't care). Pattern symbols are used when a group of signals define a logical state. For example, a microprocessor has a set of pins that indicates the type of bus cycle in progress. A memory read cycle is indicated when the RD~ and MREQ~ pins are 0 (logic low) and the BUSAK~ and M1~ pins are 1 (logic high). You can define a pattern symbol name called mem-read that corresponds to bit pattern 1100 and thereby mark all memory read

bus cycles in the Listing window. For other bus cycles the logic state of these pins is also important and you can define different bit patterns for each cycle type.

Figure 2–47 shows pattern symbols used in a Waveform window.

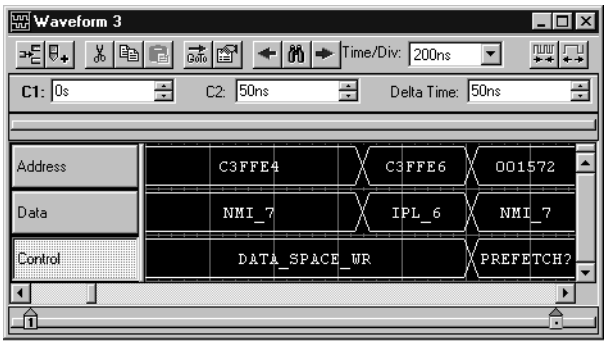


Figure 2-47: Waveforms using pattern symbols

Range Symbols. Range symbols define a range of 32-bit addresses represented by a contiguous set of integers, marked by specific lower and upper bounds. The different types of range symbols are discussed in detail under *TLA Symbol File Format* beginning on page B–1.

When defining a range symbol file, do not overlap ranges of values. If ranges overlap, they may not be recognized. For example, if SYM1 covers the range 1000–3FFF, and SYM2 covers 2000–2FFF, then the values in range 2000–2FFF may be recognized as either SYM1 or SYM2, and the values in the range 3000–3FFF may not be recognized as SYM1 at all.

The range symbols shown in Figure 2–48 define subroutine boundaries.

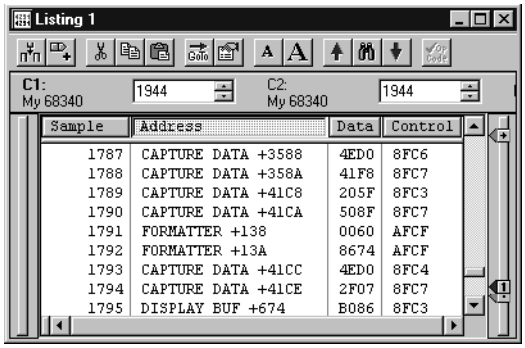


Figure 2-48: Listing data using range symbols

Symbols Dialog Box

Use the Symbols dialog box to provide an overview of all currently loaded symbol files (see Figure 2–49). You can display information about all symbol files currently used by the logic analyzer.

The following status information is available for each currently loaded symbol file:

- The last time the file was loaded into the logic analyzer application software. It also includes error and warning messages associated with the last load.
- When the file was last modified. The logic analyzer also displays a message if the file may need to be reloaded (such as when the file is modified after it was first loaded).
- The format of the loaded file.
- If the file can be unloaded or if the file is currently in use. Symbol files can only be unloaded if no data windows or setups are using them.

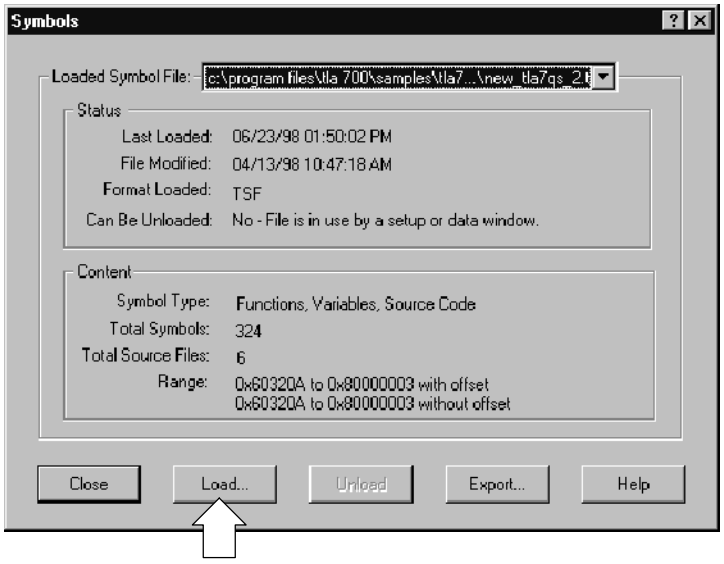


Figure 2-49: Symbols dialog box

The following information is displayed in the Symbols dialog box:

- Whether the file is a pattern symbol file or a range symbol file. If the file is a range file, this field also lists the types of symbols loaded.
- The number of symbols loaded from the file. Symbol files can have an unlimited number of symbols. The number of symbols is limited by the amount of memory. When you load a symbol file, the symbols are placed in memory. Because symbol files consume memory, you should unload unused symbol files to keep memory available for your main application.
- The number of source files referenced by source code symbols loaded from the file.
- The minimum and maximum address values and offset information.

Click the Load button (see Figure 2–49) to open the Select Symbol File dialog box and load a new symbol file. You can browse the file system for the symbol file. If the symbol file is a range file, you can click the Options button in the Select Symbol File dialog box to open the Load Symbols Options dialog box.

Click the Export button to save the current file as a TSF-format symbol file. You can view the exported symbol file with applications such as Wordpad. Edit the symbol file by saving it under a new name and using a text editor. Save the edited file in text format. You can then load the edited symbol file.

Load Symbol Options Dialog Box

Use the Load Symbols Options dialog box (see Figure 2–50) to specify options for range symbol files before loading them into the system.

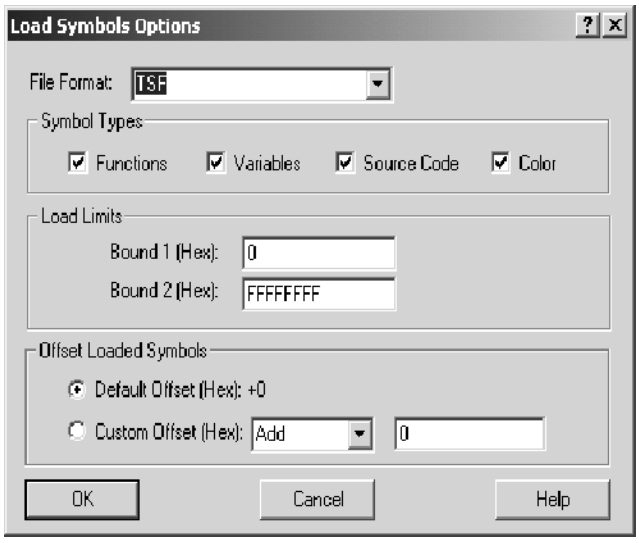


Figure 2- 50: Load Symbol Options dialog box

Select one or more of the symbols types to load. If you want to use the symbol file with the Source window, you should click the Source Code check box.

You can enter a decimal number for the maximum number of symbols to load. The maximum number of symbols that you can load is limited only by the amount of memory available. The file loads symbols until the specified maximum number of symbols is reached. Additional symbols are ignored, even if they fall within the Bound 1 and Bound 2 range limits.

The Bound 1 and Bound 2 fields define the range of symbol addresses that will be loaded. You can enter any hexadecimal values from 0 through FFFFFFFF. Symbols with values outside of these limits are ignored and will not be loaded.

NOTE. *If the lower bound of the range symbol is within the Bound 1 and Bound 2 limits and the higher bound is not, the entire symbol will be valid. However, if the higher bound is within the Bound 1 and Bound 2 limits and the lower bound is not, the entire symbol will be ignored.*

Select either Default Offset or Custom Offset to apply an offset to the symbol values. If you select Default Offset, the default offset is read from the source file and applied to each symbol in the file as it is loaded. If you select Custom Offset, you can add or subtract the specified offset value to each symbol in the file as it is loaded. You can choose any 32-bit hexadecimal value from 0 to FFFFFFFF.

When you enter bound values, enter the values without an offset value. If your application adds an offset, you must subtract the offset value before you enter the bound values.

Reference

Setup

This section describes how to set up the logic analyzer (LA), DSO modules, and pattern generator modules.

For further details, particularly about selections available to you in windows and dialog boxes, please refer to the online help.

Starting From the System Window

The System window gives an overview of the logic analyzer configuration, arming, and triggering relationships. The System window also indicates whether LA modules are merged and whether an external oscilloscope has been set up. See Figure 3-1.

A black arrow from one module to another indicates that one module is set up to arm another. Figure 3-1 shows the merged LA module arming the DSO module.

A module that is programmed to cause a system trigger has an indicator symbol on the right edge of the module graphic.

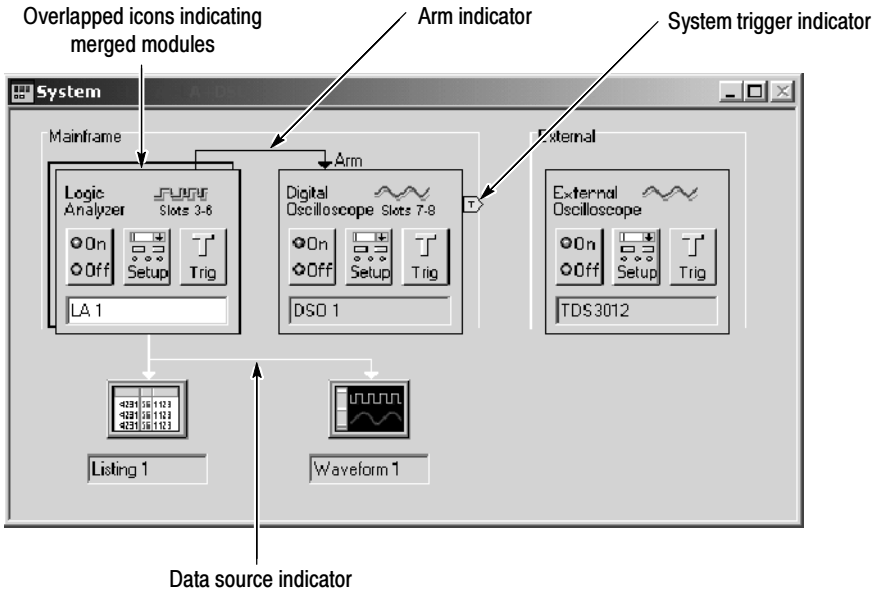


Figure 3-1: System window

Opening Other Windows from the System Window

You can use the System window as a quick navigation tool.

- To open a module Setup, Trigger, or Program window from the System window, click the Setup or Trigger button in the module icon.
- To open a data window from the System window, click the data window button. See Figure 3–2.

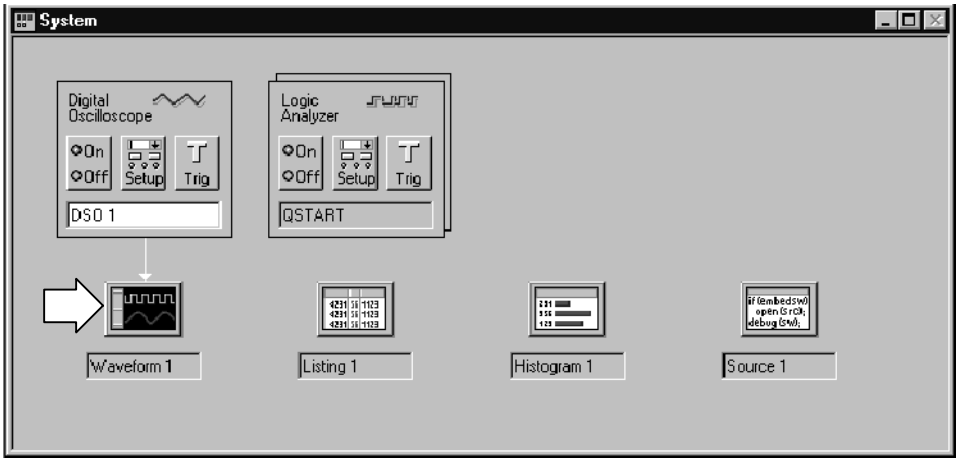


Figure 3-2: Opening a Waveform window from the System window

Disabling Modules

If you are not using a module, you can disable it by clicking the module On/Off button. When you disable a module, make sure that no other trigger programs depend on that module output.

Renaming Windows

You can rename the windows by selecting the current window labels and overtyping. Names must be unique and are limited to the space available.

Identifying Modules

If you are unsure which physical module is represented by an icon, double-click the icon to open its System Properties tab. This property tab lists information about the module, including the mainframe slot numbers in which it is installed. (Slot numbers are indicated on the mainframe.)

Setting Up the LA Module

The primary function of the Setup window (see Figure 3–3) is to configure the LA module for compatibility with the target system. This is where you specify channel groups, set thresholds, and select the sample clock rate. Additional selections configure the LA module for best compatibility with the type of data you want to acquire.

Before you acquire and display data, you must first set up the LA module using the LA Setup and Trigger windows. Together, these windows determine the data to be acquired.

Each module has its own Setup window and Trigger window, and each is set up individually. You should configure the Setup window before the Trigger window, because some of the Setup window settings affect Trigger window selections.

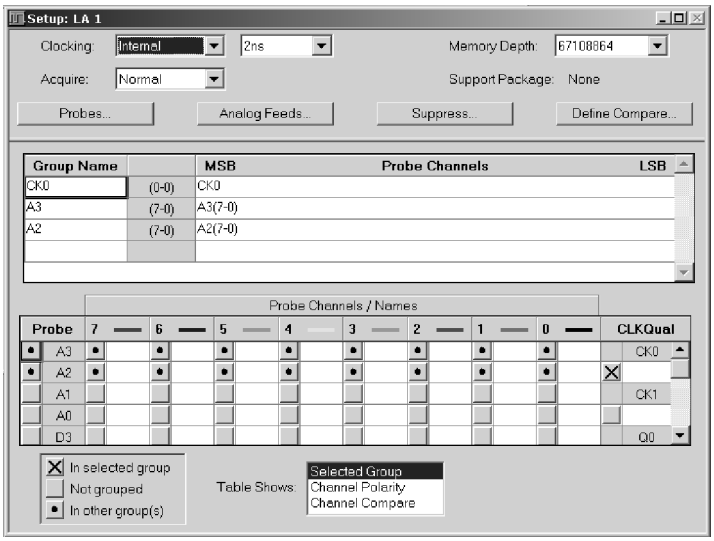


Figure 3-3: LA module Setup window

***NOTE**. If you intend to use merged modules, turn to page 3–73 for information before you proceed with the setup procedure.*

Microprocessor Support Setup

If you intend to use a microprocessor support package, load it before completing the entries in the Setup window. The microprocessor support package configures the Setup window for you.

To load a microprocessor support package, from the File menu, click Load Support Package, select the support package you want to load, and then click Load.

After loading the microprocessor support package, the LA Setup window shows the channel definitions, channel groups, and clocking requirements for the microprocessor support package. Figure 3–4 shows an example of the LA Setup window after loading the QSTART support package.

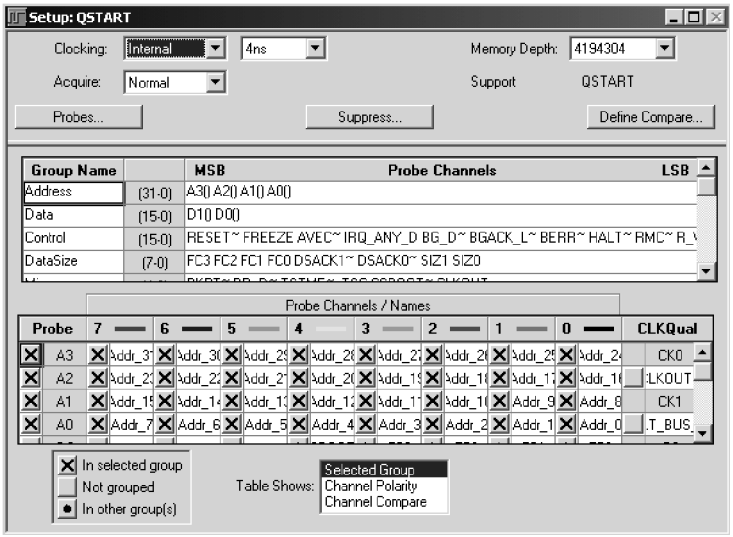


Figure 3-4: Setup window with the QSTART support package

For information about microprocessor support packages, refer to the online help and to the instruction manual that came with your microprocessor support package.

Performance Analysis Setups

If you intend to do performance analysis with your LA module, you may want to load a microprocessor support package that contains the predefined channel setups and clocking setups. You can also define the channel and clocking setups in the Setup window if you are not using a microprocessor support package.

Sample Suppression

You can use sample suppression to suppress or hide samples in the display windows. This can help you focus on the data that you want to see. When you suppress data samples, the suppressed samples are still in the acquisition memory; you can turn the sample suppression off to view all the data.

Click the Suppress button in the upper portion of the Setup window to display the Sample Suppression dialog box (see Figure 3–5). Select one of the options to define the data suppression. You can select a similar dialog box by right-clicking in one of the display windows.

For more information on data suppression, refer to the online help.

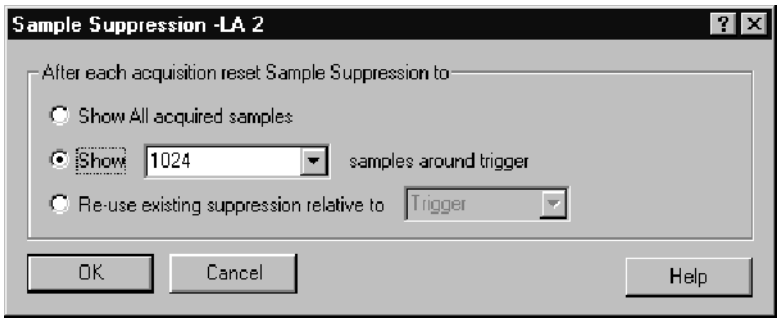


Figure 3-5: Sample Suppression dialog box

Data Compare

Data Compare allows you to compare the current acquisition data of an LA module to a known reference data. You can quickly view data differences and similarities in a Listing or Waveform window using user-defined colors.

Selecting Channels for the Memory Compare. Choose the channels that you want to compare in the LA Setup window by selecting Channel Compare in the Table Shows box (see Figure 3–6). You can then compare all data channels, specific channel groups, or individual channels by selecting the appropriate channels in the Probe Channels/Names table.

After selecting the channels that you want to compare, click the Define Compare button in the upper right of the Setup window to define the compare actions.

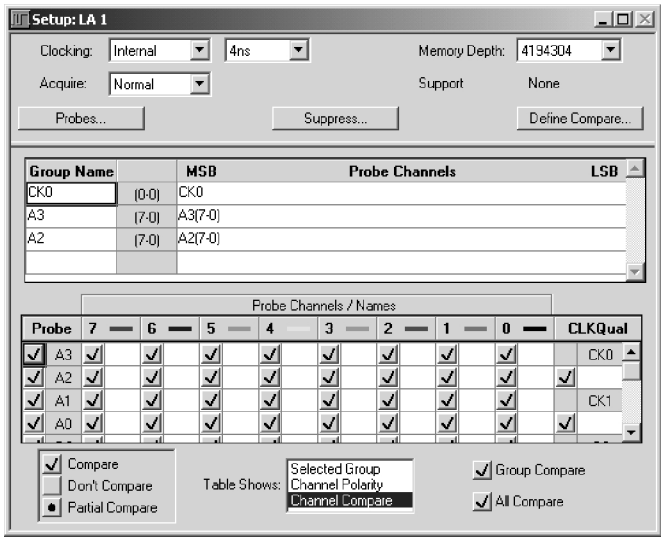


Figure 3-6: Selecting channels for memory compare

Defining Memory Compare Parameters. To enable the Define Compare dialog box controls, select the Enable Data Compare check box as shown in Figure 3–7. Select the reference data source in the list box; if the data source that you are interested in does not appear in the list, click Add Data Source to browse for the data source in the file system.

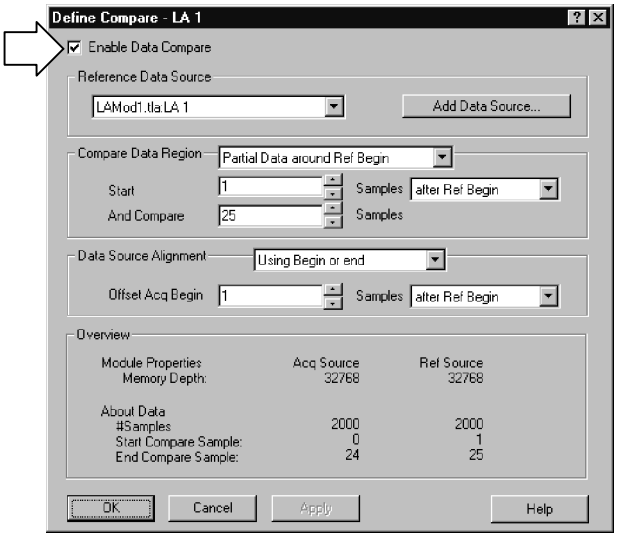


Figure 3-7: Enabling data compare

After you select the data source, define the amount of data that you want to compare against. You can compare all data or a portion of the data by filling in the appropriate information. You can also define the alignment of the data by filling in the appropriate information. A summary of your setup displays at the bottom of the dialog.

***NOTE**. After defining the compare setup, remember to select Show Compare in the Listing Window or Waveform Window property page.*

Guidelines for Memory Compare. There are a few guidelines that you should be aware of when using memory compare:

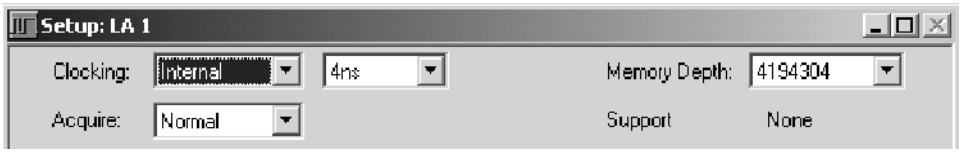
- You must select the Enable Data Compare check box in the Compare Definition dialog box (see Figure 3–7).
- Acquisition modules and reference modules must be the same width.
- Specify the color of compare data in the Listing Window or Waveform Window property sheet, or use the default colors.
- You can search for data differences or data equalities.
- You can use memory compare with repetitive acquisitions.
- You can compare only the main logic analyzer data; you cannot compare glitch data, disassembler group data, or MagniVu data.

***NOTE**. Although you cannot compare disassembler group data directly, you can compare the raw data (before it is disassembled) by using the channel groups as defined in the Setup window. To view these channel groups in a Listing window, use the Add Column toolbar button to add the channel group to the window.*

Clocking

Use Clocking to specify the clock(s) used to sample data. You have several clocking choices, depending on the module you are using; Internal, Internal 2X, and External are available for all module types. If you are using a TLA7Axx module, you can also choose Internal 4X, External 2X, External 2X Double Data Rate (DDR), External 4X, and Source Sync clocking. Custom clocking is also available, regardless of your module type, if a microprocessor support package has been loaded. Your clocking choice determines further clocking selections.

Internal Clocking. Internal (asynchronous) clocking uses the LA module internal clock to determine when to sample data. Typically, internal clocking is used for timing analysis (waveform data).



When you choose Internal clocking, the only additional selection is the clock rate in the next field.

Because the internal clock signal is asynchronous to the target system, be careful to select a sample period that is considerably faster than the data rate of your target system.

For more information on Internal clocking, refer to the online help.

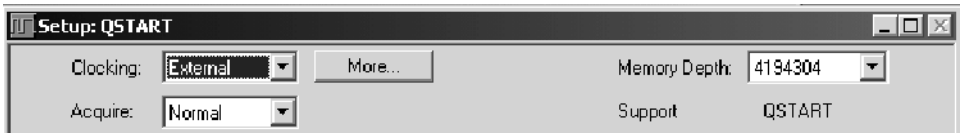
Internal 2X Clocking. When you use Internal 2X clocking mode, you trade half the input channels for twice the sampling speed and acquisition depth. You can use Internal 2X clocking mode with triggering and in both Listing and Waveform windows.

If you are using a TLA7Lx/Mx/Nx/Px/Qx module, Internal 2X clocking provides a sample rate of 2 ns; using a TLA7Axx module, Internal 2X clocking provides a sample rate of 1 ns.

Internal 4X Clocking. Available only for TLA7Axx modules, Internal 4X clocking mode allows you to trade three quarters of the input channels for four times the sampling speed and four times the acquisition depth. Available only in TLA7Axx modules, Internal 4X clocking provides a sample rate of 500 ps.

External Clocking. External (synchronous) clocking synchronizes data sampling with the clock of the target system so you can be more selective about the data you sample. This type of clocking is best for state analysis (listing data).

When you select External clocking, you have the option of further selections to define the sample clock. To do so, you create clocking definitions in the Clocking dialog box. Clocking definitions qualify when data is sampled. The definitions consist of a Boolean combination of events, linking clock and qualifier lines. Data is sampled and stored in memory only when the clock definition is true.



For more information on External clocking, refer to the online help.

Advanced Clocking. Advanced clocking is available only if you select External clocking. Use advanced clocking to set up multiple-phase clocking, probe demultiplexing, and other clocking features. Multiple-phase clocking specifies two different sample clock equations and assigns an equation to separate probe groups in order to clock in sample data. You can also sample data from different channel groups at different points in time, relative to the sample clock through a variable setup and hold window.

For more information on advanced clocking, refer to the online help.

External 2X Clocking. Available only in TLA7Axx modules, External 2X clocking allows you to acquire listing data at twice the normal maximum sample frequency of the logic analyzer. However, this increased speed and acquisition depth come at the expense of half the acquisition input channels. When you use External 2X clocking, you acquire data using a clock rate of up to 800 MHz from the test system. The maximum data rate in 2X clocking mode is 800 MB/s.

You can access advanced 2X clocking functionality by clicking the More button. The 2X Clocking dialog box allows you to select the active clock edge and to align data, in relation to the specified clock edge, for each channel group. The Setup/Hold window graphic illustrates your clock edge and data alignment settings.

External 2X DDR Clocking. Available only on TLA7Axx modules, External 2X Double Data Rate (DDR) clocking allows you to acquire data on both the rising and falling clock edges at clock rates up to the normal maximum sample frequency of the logic analyzer. In this mode, half the logic analyzer input channels are traded for twice the data rate and twice the acquisition depth. When you use External 2X DDR clocking, you acquire data using a clock rate of up to 450 MHz from the target system. The maximum data rate in External 2X DDR clocking mode is 900 MB/s.

You can access External 2X DDR advanced clocking functionality by selecting a clocking type of External 2X and then clicking the More button. Note that you must specify a clock edge of Both. The 2X Clocking dialog box also allows you to align the data, in relation to the specified clock edge, for each channel group. The Setup/Hold window graphic illustrates your clock edge(s) and data alignment settings.

External 4X Clocking. Available only in TLA7Axx modules, External 4X clocking acquisitions allow data to be acquired and displayed at approximately three to four times the normal maximum sample frequency of the logic analyzer. In this mode, three quarters of the logic analyzer input channels are traded for three to four times the speed and four times the acquisition depth. The reason that the External 4X clocking mode data rate does not always increase by four times above the base synchronous rate of the logic analyzer is that the Setup/Hold window requirements of the logic analyzer may come into play. Setup and hold requirements on the acquisition data can limit the acquisition rate to a lesser value than if it were constrained by the maximum clock speed alone. When you use External 4X clocking, you acquire data using a clock rate of up to 625 MHz from the test system. The maximum data rate in 4X clocking is 1.25 GB/s.

External 4X clocking mode is a double data rate (DDR) clocking mode, which means that the two acquisition samples are taken per clock cycle. This means that the data rate of the acquisition is double the rate of the clock signal that is driving it.

You can access advanced 4X clocking functionality by clicking the More button. The 4X Clocking dialog box allows you to select the active clock edge and to align data, in relation to the specified clock edge, for each channel group. Each channel group may be assigned a second edge delay to skew the second data capture in relation to the first. The Setup/Hold window graphic illustrates your clock edge and data alignment settings.

Source Synchronous Clocking. Available only in TLA7Axx modules, Source Synchronous clocking sends a strobe signal with the data signal. The data is then synchronized with the strobe signal instead of the clock signal. The sending device is responsible for synchronizing the data with the strobe signal; the receiving device is responsible for latching the data inside of itself and for resynchronizing the data with the clocking state machine (CSM) heartbeat clock. This type of clocking is best used for state analysis when you want to see the data signal in relation to the CSM heartbeat clock.

You can access advanced source synchronous clocking functionality by clicking the More button. The Source Synchronous Clocking dialog box allows you to specify edge detectors, define clock groups, create clocking equations, demultiplex data, and set up advanced clocking parameters. Once you have set all clocking parameters, you can click the Validate button to check that no source synchronous click setting conflicts exist.

Figure 3–8 shows a typical DDR SDRAM read data transfer, illustrating how the source synchronous clocking feature can be used to acquire data from a Double Data Rate (DDR) SDRAM memory bus.

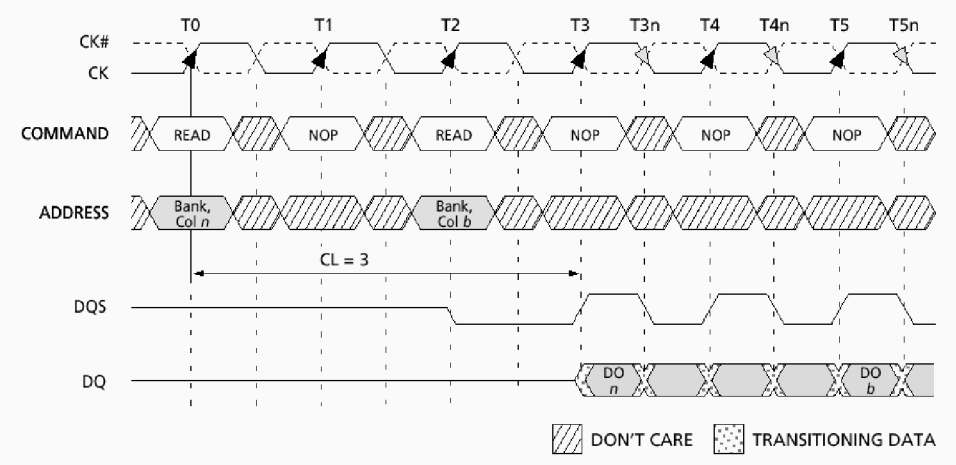


Figure 3-8: Typical DDR SDRAM consecutive READ bursts

Tables 3–1 and 3–2 show the channel assignments and group definitions, respectively, for the SDRAM signals contained in Figure 3–8.

Table 3-1: Channel assignments

SDRAM signal	Logic Analyzer channel
DQS	CK1
CK	CK0
CAS#	CK3
WE#	CK2
CS#	C2(3)
RAS#	C2(2)

Table 3-2: Group definitions

	Group name	Channels
	CLK	CK
Control	CMD_R	CS#, RAS#, CAS#, WE#
Control	CMD_W	CS#, RAS#, CAS#, WE#
Address	ADD_R	E3(7-0), E2(7-5)
Address	ADD_W	E1(7-0), E0(7-5)

As indicated in Figure 3–8, DQS is used as the strobe and the data is edge aligned with the strobe. For the read cycle, the setup/hold window must be set to sample the data after the strobe edge occurs (rising and falling edge). In the example, the CAS latency is three clock cycles, so the pipeline delays for the common clock signals need to be adjusted to three in order to put all the information on the same clock sample.

The signals that comprise the COMMAND group are CS#, RAS#, CAS# and WE#. A truth table for these signals is shown in Figure 3–9. To simplify the example, two of the four signals are used as qualifiers to enable the read data to be captured at the correct time. CAS# is assigned as QUAL2 and WE# is assigned as QUAL3. Because only two qualifiers are used, a few AUTO REFRESH, SELF REFRESH or LOAD MODE REGISTER cycles may be in the acquisition data.

TRUTH TABLE 1 – COMMANDS
(Note: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	9
NO OPERATION (NOP)	L	H	H	H	X	9
ACTIVE (Select bank and activate row)	L	L	H	H	Bank/Row	3
READ (Select bank and column, and start READ burst)	L	H	L	H	Bank/Col	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	Bank/Col	4
BURST TERMINATE	L	H	H	L	X	8
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	Code	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	6, 7
LOAD MODE REGISTER	L	L	L	L	Op-Code	2

Figure 3-9: Truth Table for the COMMAND group

A typical DDR SDRAM write data transfer is shown in Figure 3–10. The DQS signal is again used as the data strobe, but this time the data is center-aligned with the strobe. For the write cycle, the setup/hold window must be set to sample the data centered around the strobe edge (rising and falling edge). The same set of COMMAND group signals are used to determine the write cycle (see Figure 3–9). The qualifier assignments are the same for capturing the write data.

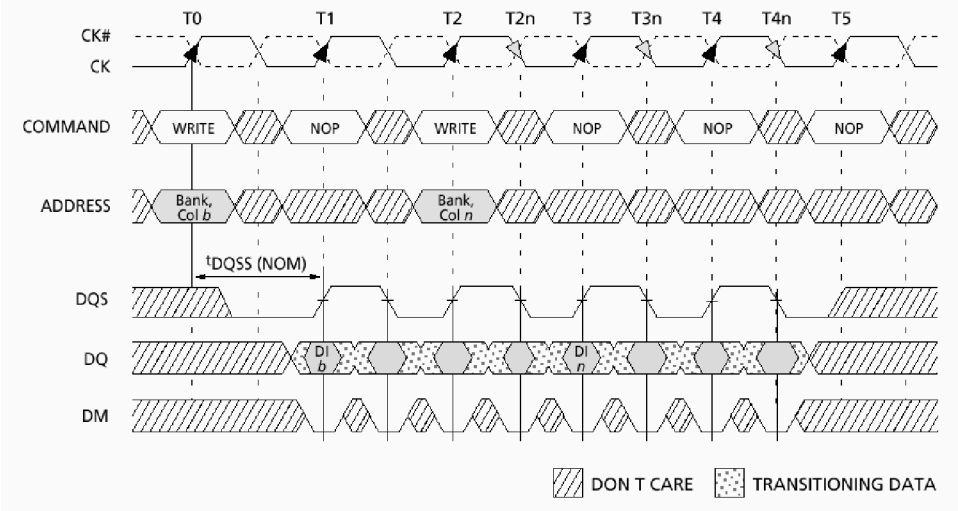


Figure 3-10: Typical DDR SDRAM consecutive WRITE to WRITE

In order to capture the DDR read and write data, use the Source Sync clocking capability of the TLA7Axx module. To begin, set up the Edge Detectors tab. As indicated in this tab, Edge Detector 0 is the CSM Heartbeat Clock, which means that Edge Detector 0 is the master clock that clocks the Clocking State Machine and the Clock Group Complete sections. You have a total of four Edge Detectors, each with four clocks (rising and falling edge) from which to choose. Assign the rising edge of the DDR SDRAM clock to Edge Detector 0, CK0 rising edge. For Edge Detector 1, assign the DQS signal to Edge Detector 1, CK1 rising and falling edge. Figure 3–11 shows the edge detect assignments.

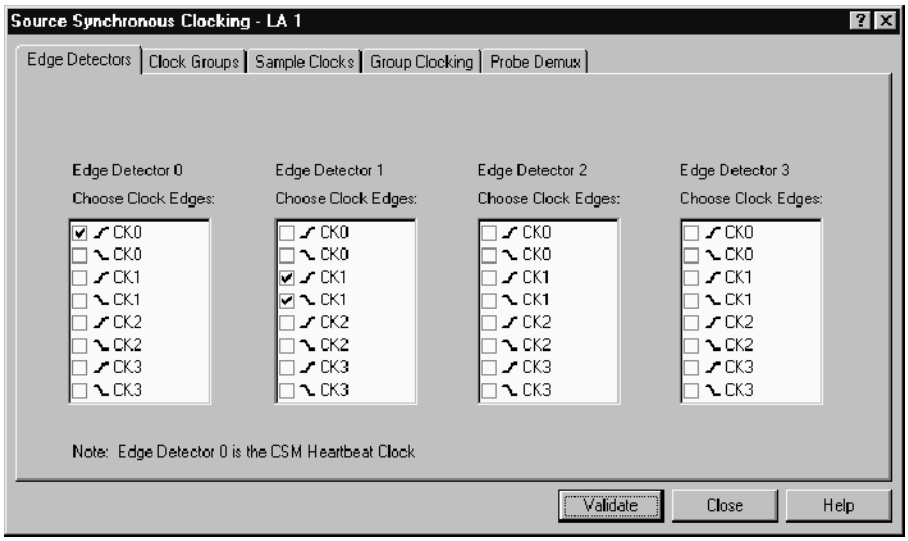


Figure 3-11: Edge Detector assignments

The Clock Groups tab has three Clock Groups from which to choose, each with four Edge Detectors. Clock Group 0 and Edge Detectors 0 and 1 are used for the example application. The DDR SDRAM clock and the DQS strobe comprise Clock Group 0. Figure 3–12 shows the clock groups selection.

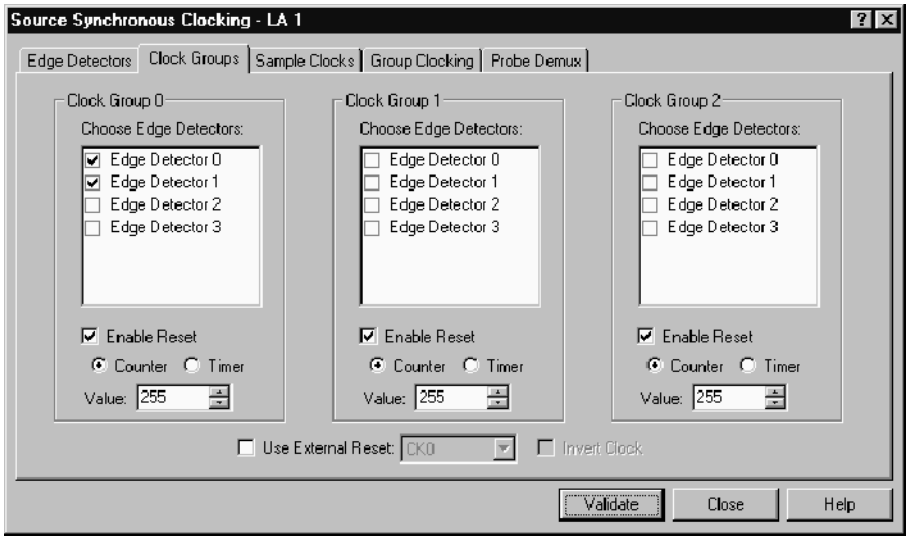


Figure 3-12: Clock Groups selection

To sample the read and write data at the correct time, use the Sample Clocks tab. Figure 3–13 shows the Sample Clock equation. The first equation is to properly sample the read data, the second equation is to properly sample the write data. These equations qualify the data so that the read and write transactions on the DDR SDRAM bus are sampled. The Sample Clocks tab supports up to four sample clocks. Each sample clock can have up to four OR'd Clock Groups, with each Clock Group containing up to three AND'd qualifiers.

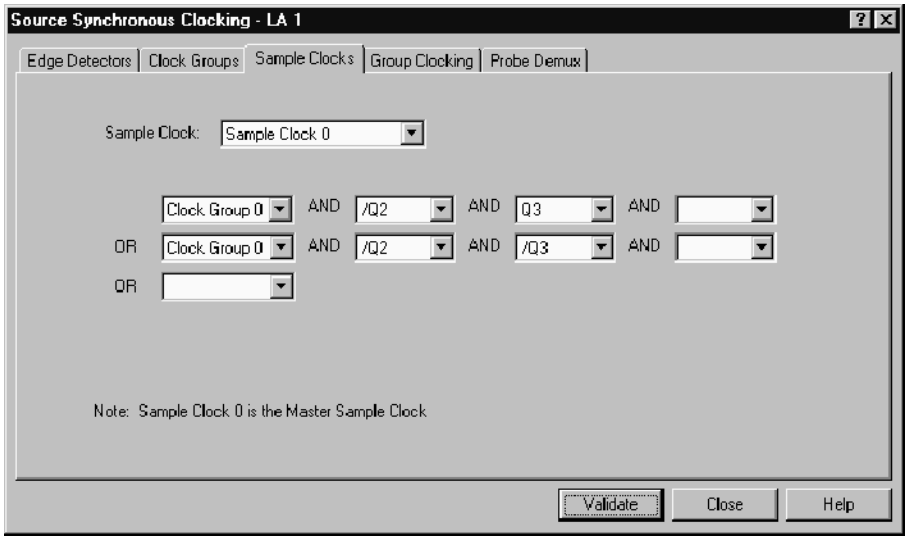


Figure 3-13: Sample Clocks equations

The Group Clocking tab is where you input the Edge Detector, Setup/Hold Window, Clock Group, Pipeline Delay and Sample Clock for all of the groups. Figure 3–14 shows the selections made in the sample application to properly capture both the read and write data on the DDR SDRAM bus.

To properly capture and align the common clock groups for both read and write, two COMMAND and two ADDRESS groups are set up. Remember, the read cycle has a CAS latency of three, so these two groups must be delayed three clock cycles to line up with the read data. For the write cycle, there is a delay of only one clock cycle. To be able to sample the same data at two different time clock pipeline delays, it is necessary to set up the groups as demultiplexed pairs. The setup/hold time relative to the common clock for these groups is always center-aligned.

For the DATA, you must have different setup/hold sample times. For the read cycle, the data is edge-aligned with the strobe; for the write cycle, the data is center-aligned with the strobe. DATA also has to be setup as a demultiplexed pair. Figure 3–14 shows the programming to capture the read and write DDR SDRAM data.

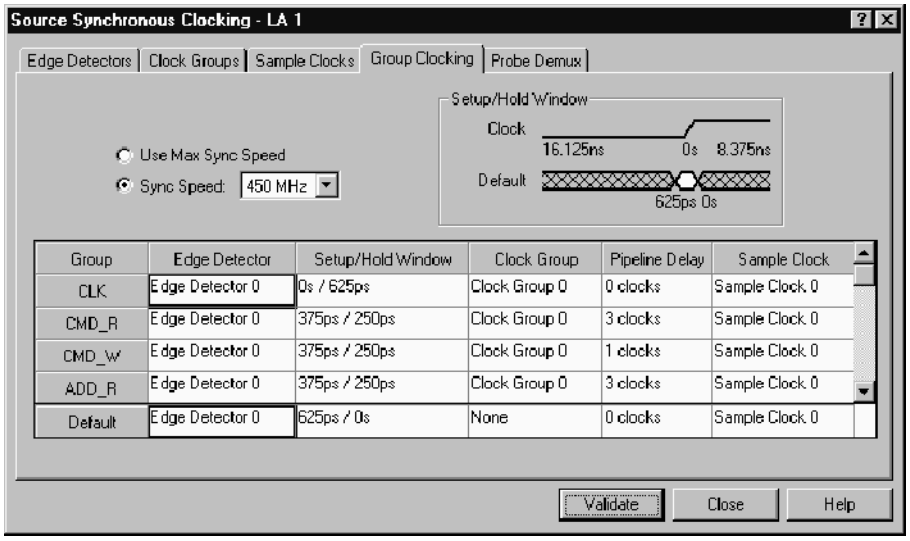


Figure 3-14: Group Clocking programming

Use the Probe Demux tab to select which groups of channels are to be demultiplexed. You have the choice of a two-way or four-way demultiplex. In addition, you have the option to select all channels or clear all channels. Figure 3–15 shows which channel groups are selected for a two-way demultiplex.

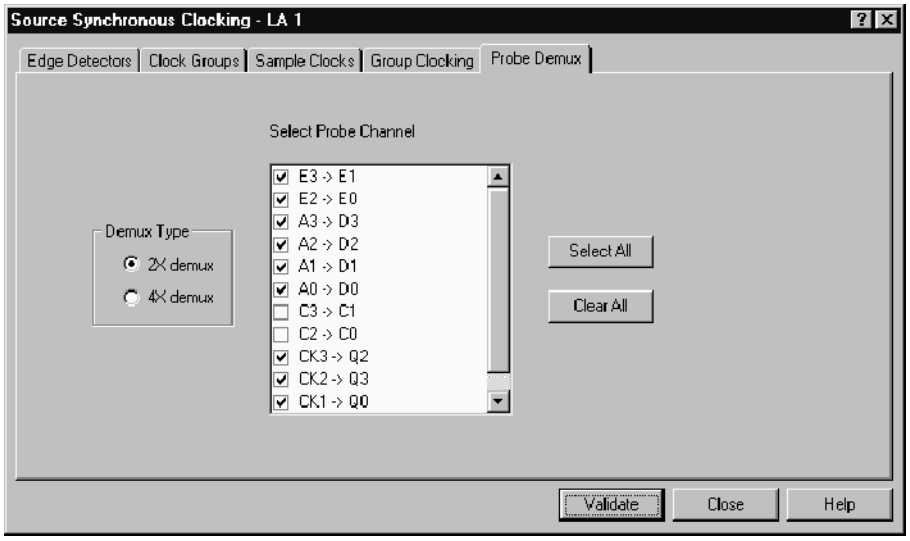


Figure 3-15: Probe Demux channel selections

The preceeding source synchronous clocking application example is intended to familiarize you with this clocking capability. In addition, you should consider the following functional clarifications:

- The source synchronous clocking hardware in the TLA7Axx is designed to wait for Clock Group Complete (CGC) signal before it clocks the CSM. If the data strobe straddles the master clock, meaning that one edge occurs before the master clock and one edge occurs after the master clock, then that sample will be clocked in on the next edge of the master clock.
- You must verify that the strobe edge is not time aligned with the master clock, because this will cause the CGC signal to shift from one master clock cycle to the next. This will cause the data sample presentation to dither back and forth.
- The separation of edges on the same signal is limited to no less than 2.2 ns (450 MHz).
- The frequency of the strobes must be equal to or less than the frequency of the master clock or the input data pipeline will overflow.

For more details on Source Synchronous Clocking, refer to the online help.

Custom Clocking. Custom clocking is used only with microprocessor support packages. Custom clocking enables and disables a variety of microprocessor-specific clock cycle types (such as DMA cycles). For more information, see the instructions that came with your microprocessor support package.

Selecting the Acquisition Mode

Use Acquire to select the acquisition mode, which determines the type of data to select and store. You can store channel data only, glitch data, setup and hold violation data, or blocks of data around requested samples.

Normal Mode. Normal mode stores only the requested channel data.

Glitch Storage Mode (Internal Clocking Mode Only). Glitch mode captures glitch data and regular data for each data channel. You must select internal clocking for Glitch mode to be available. Glitch storage is independent of glitch events. Therefore, you can trigger on a glitch even when you are not storing glitches.

Glitch mode limits memory depth to half of the maximum depth and limits the sample period to 10 ns or greater for TLA7Lx/Mx/Nx/Px/Qx modules and 4ns for TLA7Axx modules. However, there is no trade-off in channels, which avoids changing probe connections.

Setup/Hold Violation Storage Mode (External, Source Synchronous, and Custom Clocking Mode Only). Setup/Hold mode captures setup and hold violations for each channel. You must select External or Source Sync clocking for Setup/Hold mode to be available.

Setup/Hold mode limits memory depth to half of the maximum depth and limits the maximum synchronous speed to half its normal maximum value.

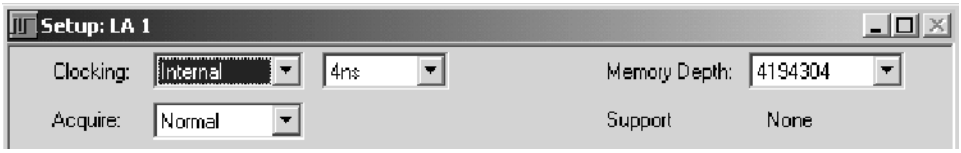
Blocks Mode. Blocks mode stores a block of approximately 60 samples around each qualified sample. In Blocks mode, only channel data is stored. If you store blocks, they will override other forms of data qualification. All samples in the block are always stored. Block size is fixed in the hardware and cannot be changed.

Setting Memory Depth

Use Memory Depth to specify the total number of samples acquired by the LA module. If you do not require full memory depth, select a lesser value because you will have less data to search to find the data of interest.

For a given memory depth there is a tradeoff between the clock sample rate and data record length. (A faster sample rate provides a shorter time window, but with higher resolution.)

***NOTE**. If you select Glitch or Setup/Hold mode, the maximum memory depth is limited to one half the normal value.*



Grouping Channels

Use channel grouping to organize the LA probe channels to match the configuration of the target system. Depending on your application, match the channel groups to the address and data buses, or other channels of interest. Then name the channel groups for easy identification.

Any number of groups can be created. Each group can contain any combination of module channels; the application does not restrict you from repeating channels from various groups.

When using group range events (range recognizers), the probe groups and probe channels must be used in hardware order. That is, probes must be used from the most-significant probe group to the least-significant probe group, based on the following order:

C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0

The probe channels must be used from the most-significant channel to the least-significant probe channel, based on the following order:

7 6 5 4 3 2 1 0

In Internal 2X Clocking and External 2X Clocking mode, half of the probe channels are designated as the demux destination, indicating that they are unavailable as a source (see Figure 3–16).

***NOTE**. If a microprocessor support package is loaded, do not change or delete the default channel groups. Doing so can cause an inaccurate analysis. However, you can still add and delete new channel groups.*

If you are using a TLA7Axx module, both Internal and External 4X Clocking modes designate three-quarters of the probe channels as the demux destination to indicate they are unavailable as a source. In Source Synchronous and External Clocking mode, the source channel availability depends on whether you have set up probe channel demultiplexing.

For more details on Source Synchronous clocking, refer to the online help.

If a microprocessor support package is loaded, the channel groups are defined for you.

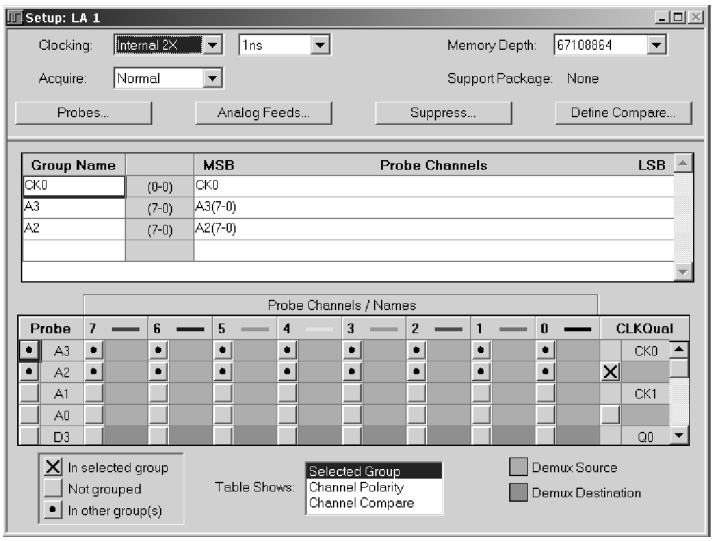


Figure 3- 16: Source and destination probe channels in Internal 2X Clocking mode

Channel Group Name. Each channel group must have a name. Use the default name or enter another name. There is no limit to the number of groups. Channel groups defined in the channel grouping table are used in other displays and setup controls. The order of the groups in this table determine the order of presentation in other windows.

For each group name, list all the probe channels that make up the group. The group names are listed in the left column of the table. The individual probe channels that make up each group are listed in the right column of the table. The center column of the table lists the number of channels in a group (where a zero refers to bit 0). For example in Figure 3–17, the Address group is made up of 32 channels, with channel 31 as the most-significant bit (A3-7) and channel 0 as the least-significant bit (A0-0).

Probe Channels/Names Table. Use the Probe Channels/Names Table to enter names for individual channels, add and remove channels from a group, or change polarity of individual channels.

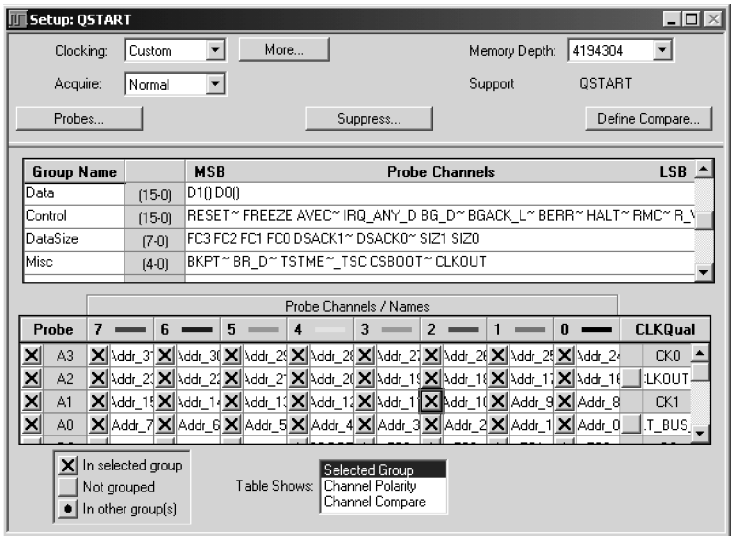


Figure 3-17: Channel grouping table in the Setup window

Analog Multiplexing

Available only in TLA7Axx modules, analog multiplexing allows you to observe multiple digital data signals on a DSO using multiple analog channel outputs. You can assign data signals in one of two ways: You can either select an *individual* channel and assign it to an analog output, or a *group* of channels and then select the analog outputs to which you want them assigned. Setting up analog multiplexing involves specifying signal routing between the LA module and the DSO module or external oscilloscope.

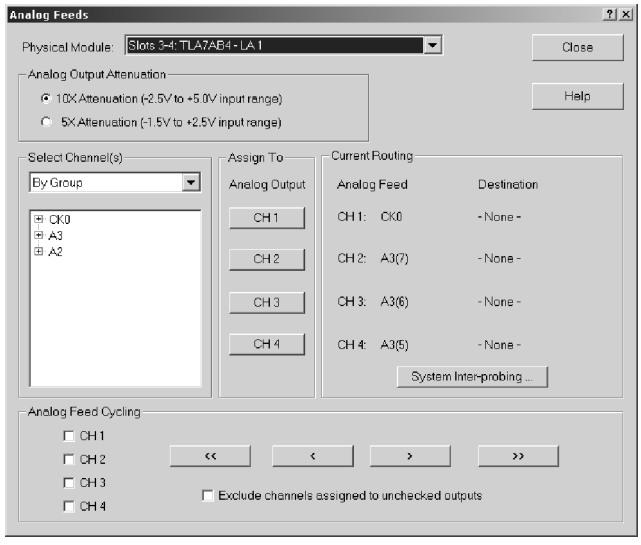


Figure 3-18: Analog Feeds dialog box

The Analog Feeds dialog box controls which digital data signals (via the probed channels on which they reside) are assigned to each analog output. In addition, you can specify an attenuation level, based on the amplitude of the signals being assigned. You can also choose the manner in which digital channels are displayed: by group, probe, or name.

Selecting individual channels.

After you have chosen a digital channel to output, you can assign it to an analog output channel by clicking a channel button under Assign To. You can confirm that the digital signal was correctly routed by reviewing the analog feed assignment information under Current Routing.

Selecting groups of channels.

When you select multiple digital channels to output, you can assign them to one or more analog output channels by selecting the check boxes associated with the target channels. If you are interested in more digital channels than you have analog outputs, use the Analog Feed Cycling buttons to cycle the selected digital channels through the selected analog outputs. You can additionally direct the system to exclude channels assigned to unchecked outputs from being re-assigned, which guarantees that channel assignments to unselected outputs are preserved. To do so, select the check box labeled Exclude channels assigned to unchecked outputs.

***NOTE**. The system only reassigns digital channels when the assigned digital channel is a member of the channels that you specified for output in Selected Channel(s) and the analog output channel to which the digital channel is assigned is not selected.*

If one or more of the selected digital channels are already assigned to an analog output, those channels are highlighted in yellow under Select Channel(s). As you feed digital channels to the selected analog output channel(s), this highlighting changes to reflect current channel routing.

The Current Routing group box displays read-only details about the assignment of individual data signals to analog outputs and the oscilloscope input ports to which they are physically connected. It additionally provides a System Inter-probing button that you can click to reassign oscilloscope destination of data signals.

***NOTE**. The Analog Feeds dialog box retains the channel assignment settings for each TLA7Axx module represented in the System window. When using Analog Feed Cycling functionality, you can assign channels using one of the control buttons, then close the Analog Feeds dialog box. Later, when you reopen the dialog box, you can resume assigning digital channels to analog outputs. However, if you change either the setup of groups or any channel names, channel assignment settings will return to defaults the next time the Analog Feeds dialog box is opened.*

Because the TLA application cannot sense probe physical connect/disconnects, it is unable to manage logic analyzer or oscilloscope mapping automatically. Therefore, you must use the System Inter-probing dialog box to manually specify which connectors between the logic analyzer and oscilloscope are fitted with probe connections.

***NOTE**. Only TLA7Axx modules, DSO modules, and external oscilloscopes can be displayed in the System Inter-probing dialog box.*

When an inter-probing connection is created, the system changes the oscilloscope signal name to reflect the logic analyzer channel that is feeding it. The signal name is visible in both the DSO Setup channel tabs and the waveform element label. The system also automatically adjusts the time alignment dialog to incorporate whatever signal path delay is determined for the oscilloscope individual signal. The delay is a single time value, based on both the cable length and the particular path of the logic analyzer channel feed.

Signal routing from the logic analyzer.

You can specify the logic analyzer channel through which probe data is sent to the currently selected oscilloscope channel using the Route from LA dialog box. To display this dialog box, select Route from LA from the context menu associated with a selected oscilloscope channel waveform.

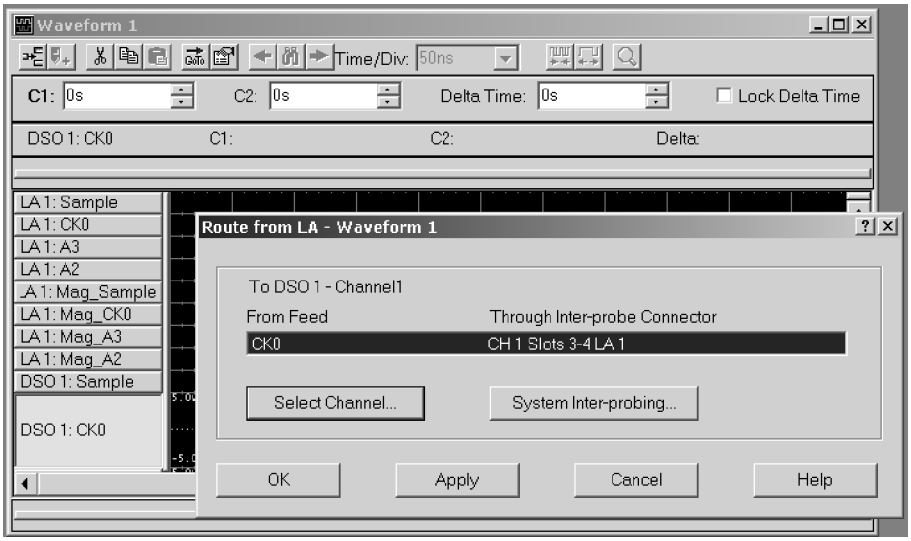


Figure 3- 19: Route from LA dialog box

The Route from LA dialog box displays the currently defined inter-probing connection and its feed for the oscilloscope channel. This item cannot be selected and is displayed for information purposes only. If no inter-probing connection is defined for the oscilloscope channel, the field is empty.

Click the System Inter-probing button to change the contents of the scroll list by adding or changing the connection to the logic analyzer.

Click the Select Channel button to select a new logic analyzer channel to feed the inter-probe connection to the oscilloscope channel. This button is made available when an inter-probe connection is defined.

Signal routing to the oscilloscope.

You can specify the inter-probe connector and DSO channel through which to route probe data from the specified logic analyzer channel using the Route to DSO dialog box. To display the Route to DSO dialog box, select Route to DSO from the context menu associated with a selected LA channel waveform. The Route to DSO context menu item is enabled only if the selected waveform is a TLA7Axx channel.

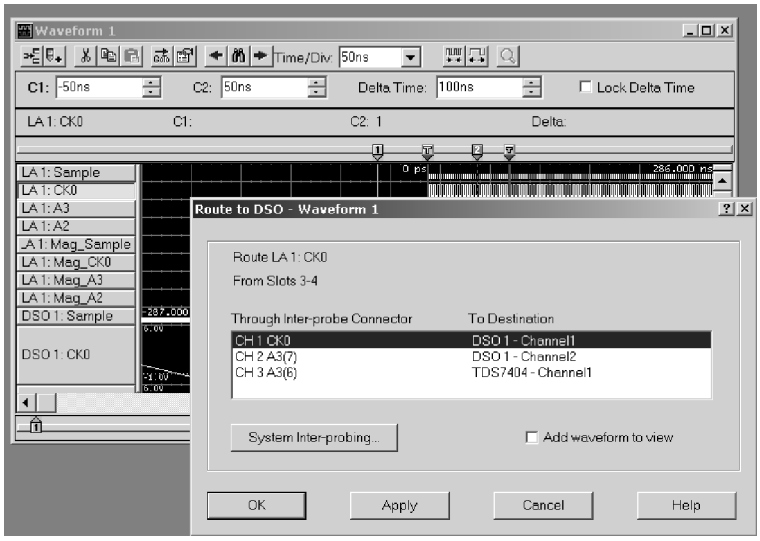


Figure 3-20: Route to DSO dialog box

The Route to DSO dialog box provides a list of oscilloscope channels that have inter-probe connections defined to the logic analyzer. If no inter-probe connections are defined, the list is empty. If the oscilloscope list contains the desired LA channel, then that list item is selected by default. Select an oscilloscope channel and click OK to feed the logic analyzer channel to the inter-probe connection attached to the oscilloscope channel.

The check box named Add new waveform to view is not selected by default because the waveform view typically already contains waveforms for the oscilloscope of interest. Selecting this check box and clicking OK will add a waveform of the selected oscilloscope destination to the view.

Click the System Inter-probing button to change the destination list contents by adding or deleting the connections for the logic analyzer.

Activity Indicators

Use the Activity tab located in the Probe Properties dialog box (click the Probes button located in the LA Setup window) to show the real-time signal activity at the LA module probe tip without having to acquire data. The activity symbols indicate whether the signals at the probe tip are high, low, or changing. See Figure 3-21.

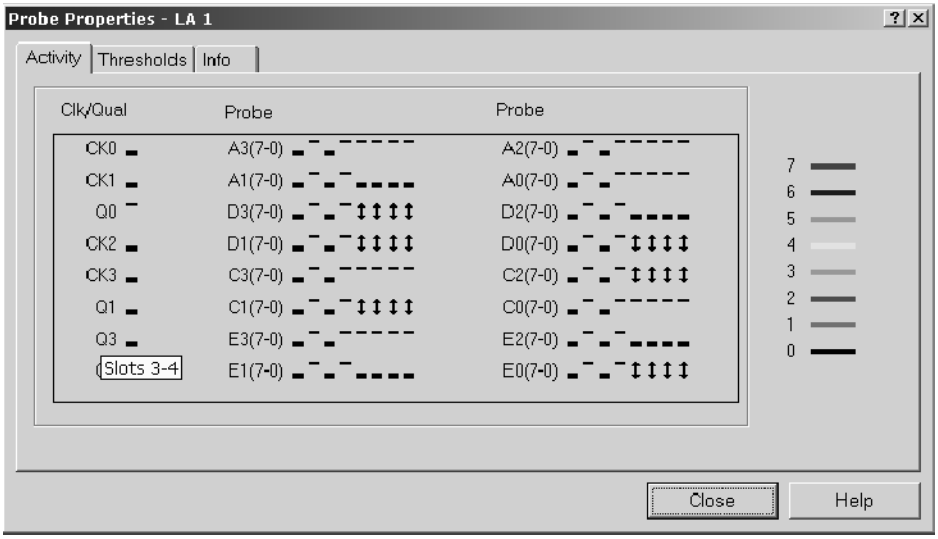


Figure 3-21: Activity Indicators dialog box

If the activity indicators show no activity, the problem could be that there is no signal voltage, the voltage threshold level is incorrect, or the channel lead is not connected. If all the channels associated with a probe are inactive, check the probe connections to the LA module.

You can leave the Probe Properties dialog box open while you set up other windows. This dialog box is useful for verifying that clocks are active in external clocking and for troubleshooting complex clock setups.

Setting Probe Thresholds

Use the Thresholds tab located in the Probe Properties dialog box to set the input threshold voltage settings for probe channels, clocks, and qualifiers of the LA module. Changes are immediately executed, even during acquisition.
Figure 3–22 shows the Thresholds tab within the Probe Properties dialog box.

***NOTE**. You can display a second Probe Properties dialog box to view real-time signal activity while modifying input threshold voltages. To do so, click the Probes button again and then click the Activity tab.*

Initially, the Thresholds tab contains values that are set in the Preset tab of the Options dialog box.

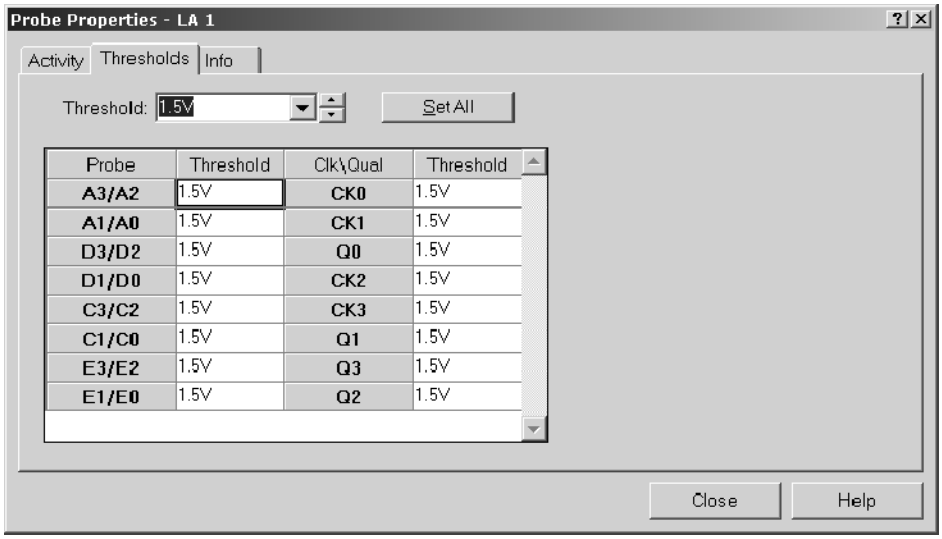


Figure 3-22: Probe Thresholds dialog box

Probe Info List

Use the Info tab located in the Probe Properties dialog box to view a listing of the probes connected to the logic analyzer and the set of channels coming through each probe. This tab is intended for informational purposes only. See Figure 3–23.

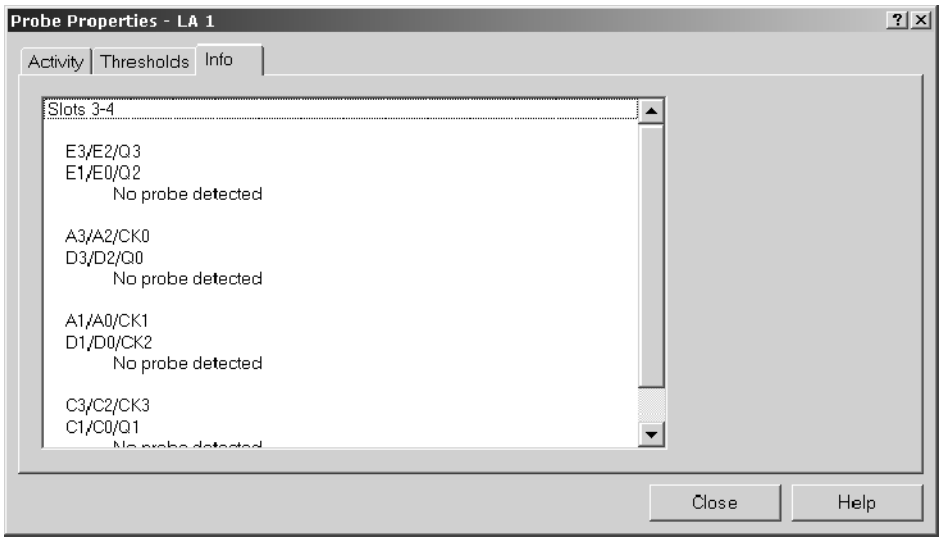


Figure 3-23: Probe Info dialog box

Setting Up the Trigger Program

Use the LA Trigger window (see Figure 3–25) to construct a trigger program. You also use the Trigger window to select how and when to store data.

It is important to configure the LA module Setup window before you work in the Trigger window, because some of the Setup window settings affect Trigger window selections.

A trigger program is a series of events and actions that define when to trigger and store data. The trigger program filters acquired data to find a specific data event, or series of data events. The trigger program can accept information from other modules or send signals external to the logic analyzer.

Trigger programs range from simple to extremely complex. They are the key to logic analyzer operation of acquiring the desired data in acquisition memory and to displaying the data for viewing.

There are two methods of setting up logic analyzer trigger programs. You can either select a preexisting EasyTrigger program or develop a trigger program using functionality available from the PowerTrigger tab.

EasyTrigger programs are designed to help you quickly start acquiring and displaying data. The EasyTrigger tab contains a list of predefined trigger programs that contain simplified event conditions. You can modify EasyTrigger program event conditions, and then rename and save the program to a specified file for later reuse.

For information about using an EasyTrigger program, refer to the online help.

You can switch between the EasyTrigger tab (to modify the trigger program or select another one) and the PowerTrigger tab (to view or modify state and clause details of the trigger program you selected) as many times as needed to acquire the desired data in acquisition memory.

CAUTION. *When you edit trigger programs from the PowerTrigger tab, you must save your changes before returning to the EasyTrigger tab. Otherwise, your changes will be lost.*

As you become more comfortable with trigger programming, you can use the PowerTrigger tab to both view and modify the predefined EasyTrigger programs, resulting in an increasingly complex trigger program designs. You can also create new trigger programs, using the PowerTrigger tab, instead of modifying predefined EasyTrigger programs.

Figures 3–24 and 3–25 show the Trigger window displaying both the EasyTrigger and PowerTrigger tab contents.

NOTE*. You can specify which trigger tab displays, by default, when you start the TLA application. From the System menu, click Options, and then click the Defaults tab. Click the Trigger Window Style field and then select the desired trigger tab from the list box.*

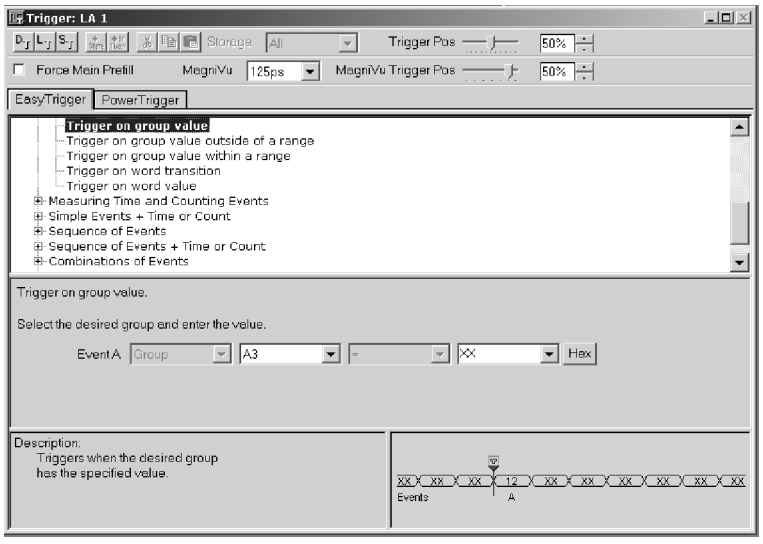


Figure 3-24: Sample EasyTrigger program

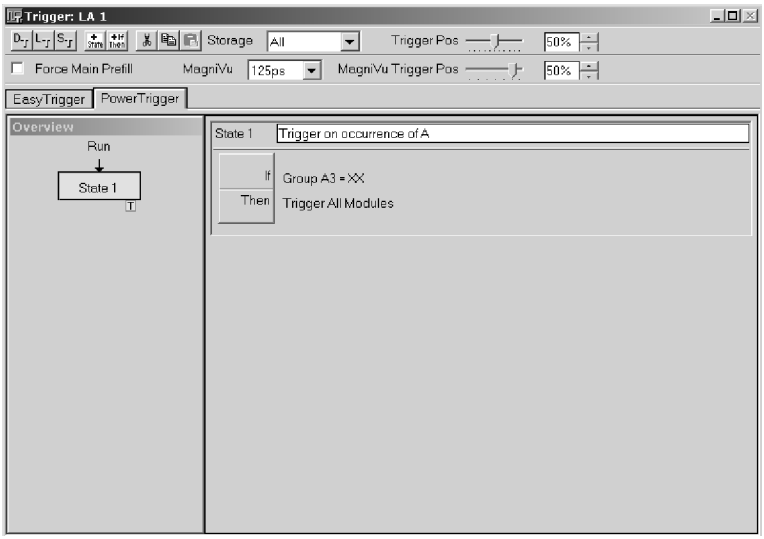


Figure 3- 25: Sample PowerTrigger program

Trigger Program Structure

A Trigger program consists of one or more states (up to 16). Only one state is active at a time.

Each state is made up of one or more clauses. If you use no more than four trigger event resources in a state, you can have up to four clauses per state. If you have less than four trigger event resources in a state, you can define up to 16 clauses per state. However, when you use a snapshot recognizer as an event in your clause definition, your use of clauses per state is restricted. If you use a snapshot recognizer and no more than one additional event, you can have up to eight clauses and one counter or timer per state. If you use a snapshot recognizer and two or more additional events, you can have up to two clauses and one counter or timer per state.

Clauses are made up of two parts: an If statement, which defines the data event of interest, and a Then statement, which specifies the action taken when the If statement is true. You can define up to eight events per If statement and up to eight trigger actions per Then statement.

During each sample clock cycle, all clauses within the active state simultaneously evaluate each data sample. Clauses are evaluated from top (State #1, IF-Then Clause #1) to bottom. When one of the clauses goes true (the event defined in the If statement occurs), then the logic analyzer performs the action(s) specified in the Then statement. There are several actions to choose from, including triggering the system and transferring control of the trigger program to another state.

***NOTE**. The clauses within a given state are hierarchical and are evaluated in real-time from top down. If multiple clauses are true in the same clock cycle, the earliest clause in the state that is evaluated as true will have its action(s) execute; all other clauses will be ignored.*

Add clause statements that are unconditionally true at the bottom of your If/Then list. Otherwise, no other If/Then clauses will be evaluated.

Complete details of a trigger program's structure are only available from the PowerTrigger tab, allowing you to either view details hidden in the EasyTrigger tab view, or change the composition of the states and clauses. The trigger program structure that displays from the EasyTrigger tab is predefined, and is based on the trigger program that you select. Using a predefined trigger structure allows you to begin using triggers without having to initially specify all of the available program implementation details.

EasyTrigger Properties

The EasyTrigger tab displays a list of simplified logic analyzer trigger programs, program controls, and both a description and graphic example of the selected trigger program. The trigger list is categorized by trigger program function and is simplified to hide many of the program implementation details, allowing you to focus on acquiring and displaying data. Once you have identified the EasyTrigger program that best fits your triggering needs, click the trigger program to display the underlying program controls. These controls are a simplified representation of the selected trigger program that allows you to select events and set event, timer, and counter values.

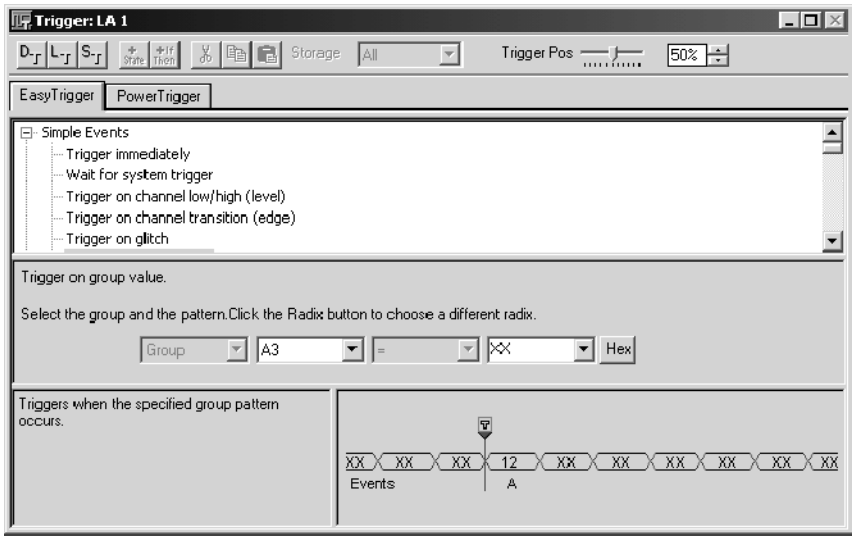


Figure 3-26: EasyTrigger tab structure

EasyTrigger Programs. One advantage of a logic analyzer is that you can create sophisticated trigger programs so that you can carefully qualify and store only the relevant data. This process is simplified by using predefined EasyTrigger programs.

The programs in the EasyTrigger program list can be used as they are designed or as a framework upon which to build more complex programs. With this in mind, the trigger programs should be viewed as a starting point to your program development, or as programming examples.

EasyTrigger programs are designed to accept data across predefined channels using a specific clocking mode. Therefore, you must specify the required channel grouping and clocking mode, using the LA Setup window, before using these trigger programs.

The EasyTrigger programs are listed below. In the trigger program descriptions, the following symbols are used:

Symbol	Meaning
A, B, C	Replaces events
Range A	A range value
N	A count (counter)
T	A time

If you choose to modify a trigger program to more closely fit your data requirements, select a trigger program that is close to what you require, and then use the functionality contained in the PowerTrigger tab to alter the program as necessary. Once you have customized the trigger, you can save it in a trigger folder that you create. You can later retrieve the saved trigger program alone or with the related saved module or system information. For information on loading trigger programs, refer to the online help.

Table 3–3 lists the programs in the EasyTrigger list and a brief description of each trigger program.

Table 3-3: EasyTrigger program list

File name	Description
Simple Events	
Trigger immediately	Triggers on the very first sample irrespective of the event type.
Wait for system trigger	The LA module is triggered when some other module sends a system trigger or the 'Run/Stop' button is pressed.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Run until the Stop button is pressed	Acquires samples until 'Run/Stop' button is pressed.
Trigger on channel low/high (level)	Triggers when the desired channel satisfies the specified condition.
Trigger on channel transition (edge)	Triggers if the desired channel satisfies the transition condition. You may choose 'Low' for falling edge or 'High' for rising edge or 'High or Low' for any edge.
Trigger on current sample using snapshot	When the specified word is matched in Event A, take a snapshot of all data lines. Trigger when a sample is found that matches the defined snapshot data in Event B.
Trigger on 2X clocking group match	Triggers when the 2X demux source group or the corresponding 2X demux destination group matches the specified value.
Trigger on 2X clocking channel match	Triggers when the 2X demux source channel or the corresponding 2X demux destination channel matches the specified value.
Trigger on 4X clocking group match	Triggers when the 4X demux source group or any of the three corresponding 4X demux destination groups match the specified value.
Trigger on 4X clocking channel match	Triggers when the 4X demux source channel or any of the three corresponding 4X demux destination channels match the specified value.
Trigger on glitch	Triggers when a glitch occurs in any of the selected groups. Glitches can be stored in Internal Clocking mode. Glitch storage is not available in Internal 2X mode, although glitch detection is possible.
Trigger on group setup/hold violation	Triggers when a setup or hold violation occurs in any of the selected groups. Instances of setup and hold fault can be acquired in External or Custom clocking. The sum of the setup and hold times must be equal to or greater than 1 ns.
Trigger on group transition	Triggers when the value of the selected group changes.
Trigger on group value	Trigger when the desired group has the specified value.
Trigger on group value outside of a range	Triggers when the group value is outside the specified range. For proper functioning of this program, probe groups and probe channels must be in hardware order.
Trigger on group value within a range	Triggers when the value of the desired group is within the specified range. For proper functioning of this program, probe groups and probe channels must be in hardware order.
Trigger on word transition	Triggers when transition occurs on any of the selected groups that have been specified in the Define Transition dialog box.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Trigger on word value	Triggers when sample matches the word definition in the Define Word dialog box.
Measuring Time and Counting Events	
Accumulate the number of occurrences of A	Accumulates the occurrences of Event A. Press the Run/Stop button to stop accumulating the count. Look for accumulated count (Counter 1) in the application Status Monitor.
Accumulate the time between A and B	Accumulate the total time between Event A and Event B. Press the Run/Stop button to stop accumulating the time. Look for the accumulated time (Timer 1) in the application Status Monitor.
Accumulate the time within a range	Accumulates the time during which the group value stays within the specified range. Press the Run/Stop button to stop accumulating the time. Look for the accumulated time (Timer 1) in the application Status Monitor.
Count occurrences of A between B and C	Count the occurrences of Event A between Event B and Event C and triggers on Event C. Look for the count value (Counter 1) in the application Status Monitor.
Measuring pulse width	Measures the pulse width of the desired channel and triggers. This program measures both On time and Off time of the desired channel. Timer 1 gives the On time value and Timer 2 gives the Off time value. Look for the Timer values in the application Status Monitor.
Measure the time between A and B	Measures the time between Event A and Event B and triggers on Event B. Look for the Timer value (Timer 1) in the application Status Monitor.
Measure the time between A and B, reset on C	Measures the time between Event A and Event B only if Event C does not occur between Event A and Event B. Look for time value (Timer 1) in application Status Monitor.
Measure the time within a range	Measure the time for which the selected group has its value within the specified range and triggers when the group value goes out of the specified range. Look for the time value (Timer 1) in application Status Monitor.
Profile range matches for time T	Increments counter on each match within range. Decrements counter on each match outside of range. Triggers when specified time has elapsed. If the counter is positive, then more values within the range have occurred. If the counter is negative, then values outside the range have occurred. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Trigger after acquiring for a specified time	Trigger after acquiring the samples for a specified time. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger after acquiring N samples	Trigger after acquiring N samples.
Trigger after filling pre-trigger acquisition memory	Triggers after filling pre-trigger acquisition memory. Note: Please ensure that the number of pre-trigger samples entered is <= number of pre-trigger samples as determined by trigger position in the tool bar. For example, if the memory depth in the Setup window is set to 512 and if the trigger position in the Trigger window is set to 50%, then the entered number of pre-triggered samples should be <= (50% of 512 = 256).
Trigger on stack overflow or underflow	Triggers if the number of function entries exceeds the max allowable value, or if the number of exits exceeds the number of entries. Note: This program requires the use of two counters to keep track of the upper and lower stack limits.
Simple Events + Time or Count	
Trigger on event absent for $>$ time T	Triggers if Event A is absent for a duration longer than the specified time.
Trigger on event absent for $\leq$ time T	Triggers if Event A is absent for any duration within the specified time.
Trigger on event present for $>$ time T	Triggers if the event is present for greater than the specified time.
Trigger on event present for $\leq$ time T	Triggers if Event A is present for any duration within the specified time.
Trigger on pulse width $>$ specified time	Triggers when the selected channel has pulse width greater than the specified time.
Trigger on pulse width $\leq$ specified time	Triggers when the selected channel has pulse width less than or equal to specified time.
Trigger on the Nth occurrence of edge	Triggers on the Nth occurrence of rising edge or falling edge of the desired channel.
Trigger on the Nth occurrence of group value	Triggers on the Nth occurrence of group value.
Trigger on the Nth occurrence of word value	Triggers on the Nth occurrence of word value.
Sequence of Events	
Trigger on A followed by B	Trigger on Event B, if Event B follows Event A eventually.
Trigger on A followed by B, reset on C	Trigger on Event B, if Event C does not occur between Event A and Event B.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Trigger on A followed immediately by B	Triggers on Event B, if Event B occurs immediately after Event A.
Trigger on B not occurring between A and C	Triggers on Event C, if Event B does not occur between Event A and Event C.
Trigger on the Nth consecutive occurrence of A	Triggers on the Nth consecutive occurrence of Event A. If anything occurs in between the consecutive occurrences of Event A, then program resets the counter and waits for Event A again.
Trigger on the Nth occurrence of A	Triggers on the Nth occurrence of Event A.
Trigger on the Nth transition of channel	Triggers on the Nth transition of the desired channel.
Trigger on violation of sequence A B C D	Triggers when Events A, B, C, and D do not occur sequentially.
Trigger on a glitch between A and B	Triggers on Event B, if glitch occurs between Event A and Event B. Glitches can only be stored in Internal Clocking mode. Glitch storage is not available in Internal 2X mode, though glitch detection is possible. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger on a sequence of edges	This example program checks a sequence of only three edges (rising or falling). Modify the PowerTrigger program to include checks for more edges.
Trigger on 16th edge transition	Triggers on the 16th transition of any of the selected groups that are specified in the Define Transition dialog box. This program demonstrates that up to 16 edge transition detectors can be specified and used.
Sequence of Events + Time or Count	
Trigger on A followed by B after N samples	Triggers on Event B, if there are at least N samples between Events A and B.
Trigger when A followed by B within N samples	Triggers on Event B, if Event B follows Event A within N samples.
Trigger on A followed by glitch within time T	Triggers if a glitch occurs within the specified time after Event A. Glitches can be stored in Internal Clocking mode. Glitch storage is not available in Internal 2X mode, though glitch detection is possible. This program is not designed to work with Timer or Counter event types for user selectable events. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger on A not followed by B within N samples	Triggers on the Nth sample following event A, if Event B does not follow Event A within N samples. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger on the Nth channel transition within time T	Triggers on the Nth transition of the desired channel if it occurs within the specified time. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Trigger on the Nth sample after A	Triggers on the Nth Sample following Event A. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger time T after A	Triggers after acquiring the samples for the specified time after the Event A. This program is not designed to work with Timer or Counter event types for user selectable events. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger main and trigger MagniVu on A	Upon recognition of Event A, the module will trigger and fill both main and MagniVu acquisition buffers. Counter and timer events should not be used. Main trigger position is set to 100% and Force Main Prefill is checked to capture the maximum number of samples after the main trigger. MagniVu trigger position is set to 0% to capture the maximum number of samples after MagniVu trigger.
Trigger main followed by trigger MagniVu within time T	Upon recognition of Event A, the module will trigger and start a timer. When the specified time has elapsed, MagniVu will trigger. Counter and timer events should not be selected. Main trigger position is set to 100% and Force Main Prefill is checked to capture the maximum number of samples after main trigger. MagniVu trigger position is set to 0% to capture the maximum number of samples after MagniVu trigger.
Trigger main followed by trigger MagniVu on event sequence	Upon recognition of Event A, the module will proceed to look for Event B. The module will trigger when Event B is detected and then proceed to look for Event C. When Event C is detected, MagniVu will trigger. Counter and timer events should not be selected. Main trigger position is set to 100% and Force Main Prefill is checked to capture the maximum number of samples after main trigger. MagniVu trigger position is set to 0% to capture the maximum number of samples after MagniVu trigger.
Trigger when A not followed by B within time T	Triggers if Event B does not follow Event A within the specific amount of time. This program is not designed to work with Timer or Counter event types for user selectable events. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger when A occurs <= N times between B and C	Triggers on Event C, if Event A occurs up to N times between Events B and C.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Trigger when A occurs <= N times between B and a time T after B	Triggers if Event A occurs up to N times in the duration between Event B and the specified time following B. This program is not designed to work with Timer or Counter event types for user selectable events. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger when A occurs N times between B and C	Triggers on Event C if Event A occurs N times between Event B and Event C. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger when A occurs N times between B and Time T after B	Triggers if Event A occurs N times between Event B and the specified time after Event B. This program is not designed to work with Timer or Counter event types for user selectable events. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger when A to B is > time T	Triggers on Event B if Event B follows Event A after a specific amount of time. This program is not designed to work with Timer or Counter event types for user selectable events. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger when A to B is <= time T	Triggers on Event B, if Event B follows Event A within a specific amount of time. This program is not designed to work with Timer or Counter event types for user selectable events. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger when the system-under-test hangs	The program checks for changes in channel value for the specified time. If channel value remains unchanged for the specified time, then the program triggers. Samples leading to SUT hang are stored. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.
Trigger when two edges are too close together	Triggers if any two edges of the desired channel are separated by less than or equal to specified time. The minimum time value that can be measured between two edges is one clock period in case of External and Custom clocking and the module timing resolution in case of Internal clocking.
Trigger when two edges are too far apart	Triggers if any two edges of the desired channel are separated by time greater than the specified time. Timer values are adjusted to the module timing resolution, which can be 2nS or 4nS, depending on the module type.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Combination of Events	
Trigger on (A and B)	Triggers when Event A and Event B occur simultaneously. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger on (A and B and C)	Triggers when Events A, B, and C occur simultaneously. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger on (A and not B)	Triggers when Event A occurs and simultaneously Event B does not occur. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger on (A or B)	Triggers when Event A or Event B occurs. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger on (not A and not B)	Triggers when neither Event A nor Event B occurs. This program is not designed to work with Timer or Counter event types for user selectable events.
Trigger on channel A and channel B	Triggers when condition on both channels A and B are simultaneously met.
Trigger on channel A and not channel B	Triggers when condition on channel A is met and simultaneously, condition on channel B is not met.
Trigger on channel A or channel B	Triggers if condition on channel A or channel B is satisfied.
Trigger on not channel A and not channel B	Triggers when neither condition on channel A nor condition on channel B is met.
Storage	
Store all writes to a specific memory location	Stores a sample when the defined word is matched. The word definition should include the Write control line and the Address of the desired memory location. The program triggers on the first occurrence of the word.
Store between A and B	Stores samples between Event A and Event B and triggers on the first occurrence of Event A.
Store except between A and B	Stores everything except samples between Event A and B and triggers on the very first sample.
Store on A and B	Stores on simultaneous occurrence of Event A and Event B and triggers on the first simultaneous occurrence of Event A and Event B. This program is not designed to work with Timer or Counter event types for user selectable events.
Store on A and not B	Stores a sample when Event A occurs and simultaneously Event B does not occur and triggers when this condition occurs for the first time. This program is not designed to work with Timer or Counter event types for user selectable events.
Store on A, trigger on B	Stores on occurrence of Event A and triggers on occurrence of Event B. This program is not designed to work with Timer or Counter event types for user selectable events.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Store on A, trigger on B, then store on C	Stores Event A as pre-trigger samples, triggers on occurrence of Event B then stores Event C as post-trigger samples. This program is not designed to work with Timer or Counter event types for user selectable events.
Store on (A or B)	Stores on occurrence of Event A or Event B and triggers on the first occurrence of Event A or Event B. This program is not designed to work with Timer or Counter event types for user selectable events.
Store on all transitions	Stores samples if any of the channel groups change state. Program triggers on the very first sample.
Store on channel A is low/high and channel B is low/high	Stores a sample if the conditions specified on channel A and channel B are simultaneously satisfied and triggers when the conditions are satisfied for the first time.
Store on channel is low/high	Stores a sample if the desired channel satisfies the specified condition and triggers when the condition is satisfied for the first time.
Store on channel transitions (edge)	Stores a sample for every specified transition of the desired channel and triggers on the first transition. Choose 'Low' for storing on falling edge, 'High' for storing on rising edge, or 'High or Low' for storing on both the edges.
Store on group transition	Stores a sample for every change in value of the selected group and triggers on the first change in group value.
Store on group value	Stores a sample for every occurrence of the specified group value and triggers on the first occurrence of the value.
Store on group value outside of a range	Stores samples when group value is not in the specified range and triggers when this condition occurs for the first time. For proper functioning of this program, the probe groups and probe channels must be in hardware order.
Store on group value within a range	Stores samples if the group value lies within the specified range and triggers when this condition is satisfied for the first time. For proper functioning of this program, the probe groups and probe channels must be in hardware order.
Store on word value	Stores a sample for every occurrence of the specified word and triggers on the first occurrence of the word value.
Store when using transition storage and edge transitions	Stores all Transition 0 transitions and then triggers after Transitions 1, 2, 3 and 4 have been seen. This program shows that a storage transition as well as edge transitions can be defined. If a storage transition is defined, then up to fifteen additional edge transitions can be specified in the main body of the PowerTrigger program.

Table 3-3: EasyTrigger program list (Cont.)

File name	Description
Store when in a subroutine (excluding subroutines it calls)	Stores only the samples that occur during the specified subroutine. The program does not store the samples of nested subroutines called by the specified subroutine. Program triggers on the first sample belonging to the specified subroutine. For proper functioning of this program, the probe groups and probe channels must be in hardware order.
Store when in a subroutine (including subroutines it calls)	Stores samples that occur during the specified subroutine and triggers when the program enters the subroutine for the first time.
Inter-Module Communication	
Send a signal to another module when A occurs	Sends a signal (signal 1 is set) to another module and triggers when Event A occurs.
Trigger all other modules when A occurs	Triggers all other modules when Event A occurs. The triggering action of this program is equivalent to that of a system trigger.
Trigger on a signal from another module	Triggers if the selected signal is set by another module.

Using an EasyTrigger Program. You use an EasyTrigger program by selecting one from the EasyTrigger program list. Depending on the trigger program that you select, there may be event conditions for you to specify before clicking the Run button and acquiring data. If you require further modifications, or want to view the program details, you can view the program from the PowerTrigger tab.

PowerTrigger Properties

The PowerTrigger tab provides access to the full, low-level trigger capabilities of the logic analyzer. It can also be used to view and modify the underlying details of an EasyTrigger program. The Overview shows the general structure of the trigger program. The Trigger Detail summarizes activity within individual program states. You can click the If/Then button in the Trigger Detail to open the Clause Definition dialog box, which contains trigger programming details.

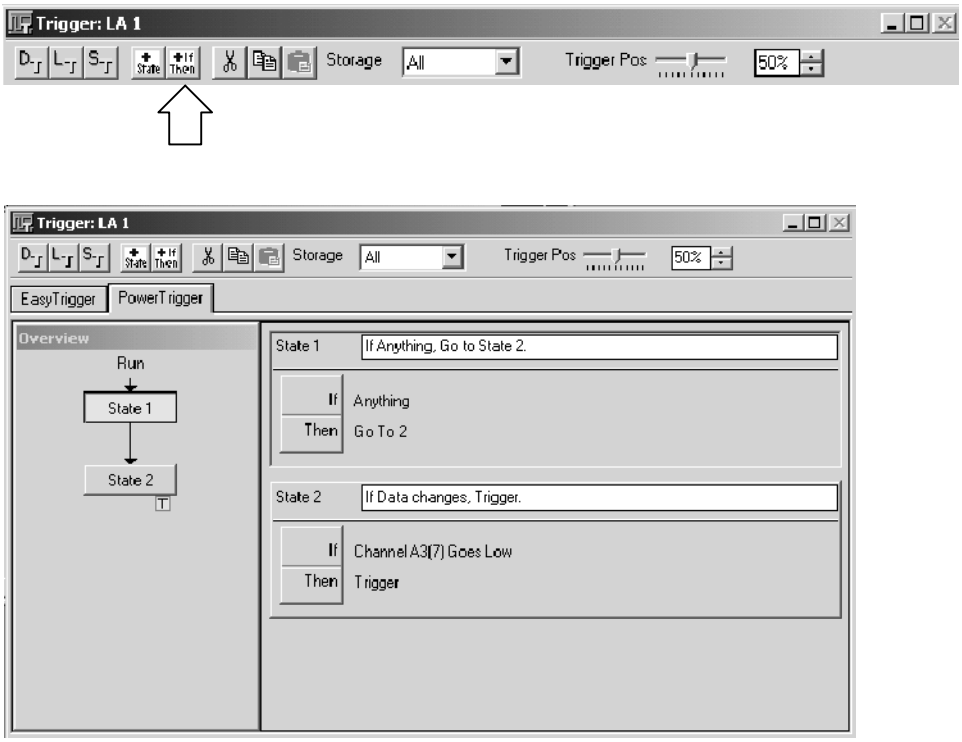


Figure 3-27: PowerTrigger tab structure

The Overview portion of the PowerTrigger tab shows the relationship of the states. See Figure 3–28. This example shows a branch occurring in State 2. This example also shows that a trigger (note the trigger indicator) occurs in State 2 and an Arm occurs.

To view the details in a particular state, double-click the State button in the Overview pane.

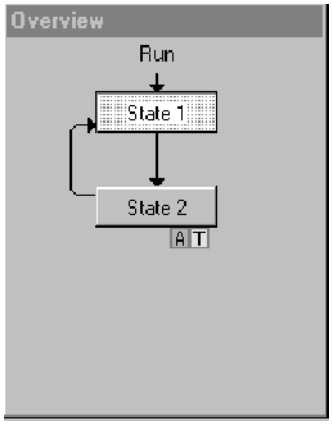


Figure 3-28: Overview portion of LA Trigger window

You can view the progress of the trigger states during acquisition using the Status Monitor (See *Viewing Acquisition Activity* on page 3–83).

The Trigger detail portion, located on the right side of the tab, shows summary information about the clauses within the states. See Figure 3–29. For lengthy trigger programs, click the State button in the Overview to jump to the corresponding Trigger programming details.

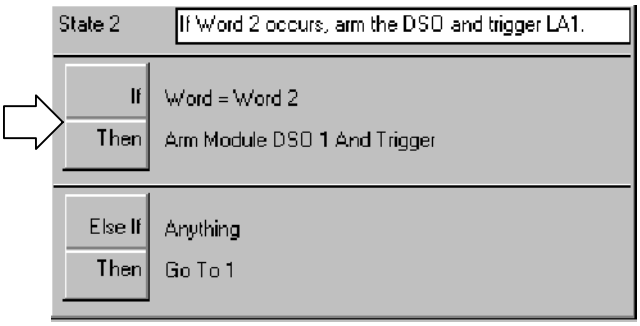


Figure 3-29: Trigger detail portion of LA Trigger window

The Clause Definition dialog box contains both events and actions that you define to specify the behavior of a given trigger clause. Click the If/Then button, located in the Trigger detail portion of the PowerTrigger tab, to display the Clause Definition dialog box.

Trigger Events. Use trigger events to define the If portion of the event clause in the trigger program. Figure 3–30 displays the Clause Definition dialog box with the trigger event list box selected. Table 3–4 lists the available trigger events and provides a description of each.

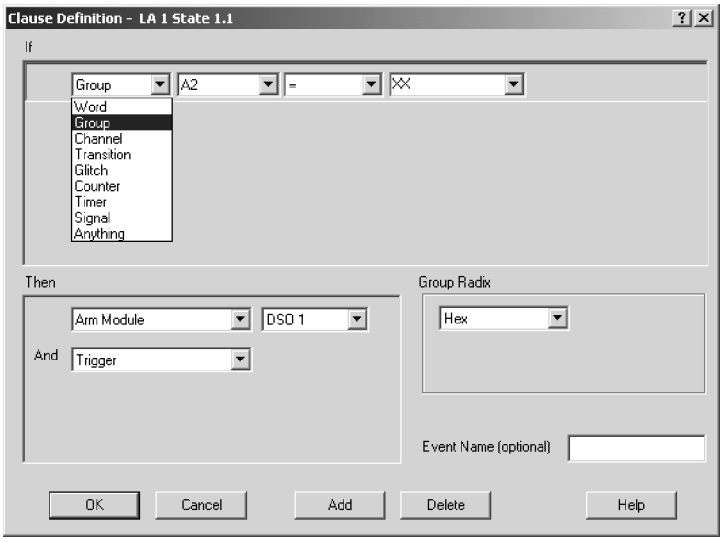


Figure 3-30: Clause Definition dialog box (Trigger Resources list box)

Table 3-4: Trigger events

Event	Description
Word	Tests the channel groups for the word values defined in the Word definition dialog box.
Group	Tests a specified channel group for a specific value, a range of values, or a value change.
Channel	Tests the specified channel for a value or a value change.
Snapshot	Available only in TLA7Axx modules, compares the current acquisition sample with a previously loaded sample in the snapshot recognizer.
Transition	Tests the specified channel groups for the transitions as defined in the Transition Definition dialog box.
Glitch	Detects glitches in channel groups as defined in the Glitch Detect dialog box. Only available with internal (asynchronous) clocking.
Setup & Hold fault	Tests setup and hold parameters as defined in the Setup and Hold Event dialog box. Not available with internal (asynchronous) clocking.

Table 3-4: Trigger events (Cont.)

Event	Description
Counter and timer events	Tests the specified counter or timer value. Timer events are supported by all LA Modules except TLA7Lx and TLA7Mx modules with serial numbers B019999 or lower.
Signal	Looks for one of the four internal system signals. Only one signal event is available in a trigger program.
Anything	All sampled data makes this event true.
Nothing	All sampled data makes this event false.

Trigger Resources. You can use up to 16 unique trigger resources (not including counters and timers) in a trigger program to define the events and actions. A trigger resource can be used more than once in a trigger program. However, some events use more than one trigger resource. Table 3–5 lists the trigger resources and any interactions that may occur when you use them.

Table 3-5: Trigger resources

Event	Operator	Restrictions and resources
Word	=, Is Not	One trigger resource across all defined channel groups.
Group		
Word recognizer	=, Is Not	One trigger resource per channel group.
Range recognizer	<, <=, >=, >, Is In, Is Not In	Three trigger resources per channel group.
Change detector	Changes	One trigger resource per group event, one change detector allowed in a trigger program, not available when transitional storage is used.
Channel		
Word recognizer	=	One trigger resource per channel group.
Change detector	Goes, Doesn't go	One trigger resource, one change detector allowed in a trigger program, not available when transitional storage is used.
Snapshot	=, Is Not, Is Loaded, Is Not Loaded	Two trigger resources and one timer event.
Transition	Occurs, Doesn't Occur	One trigger resource.
Glitch		One trigger resource, only available with internal (asynchronous) clocking.
S & H Fault		One trigger resource, only available with external (synchronous) or custom clocking.

Table 3-5: Trigger resources (Cont.)

Event	Operator	Restrictions and resources
Counter	>, <=	0 trigger resources, 2 counters or 2 timers. Maximum width 51 bits Maximum clocking 250 MHz Maximum count 2^{51} -1 Counter 1 and 2 events conflict with Timer 1 and 2 events respectively.
Timer	>, <=	0 trigger resources, 2 counters or 2 timers Maximum width 51 bits Maximum clocking 250 MHz Maximum time 2,000,000 S (23 days) Counter 1 and 2 events conflict with Timer 1 and 2 events respectively.
Signal (Signal in)	Is True, Is False	One trigger resource, uses one of four system signals. Only one signal event is available in a trigger program.
Anything		0 trigger resources. Used as a placeholder. Not available with the OR conjunction.
Nothing		0 trigger resources. Used as a placeholder with the OR conjunction.

Trigger Actions. After defining the events in the If (event) portion of the clause, you can select one or more trigger actions to complete the clause. Figure 3-31 displays the Clause Definition dialog box with the trigger Resources list box selected. Table 3-6 lists the trigger actions available for your trigger program.

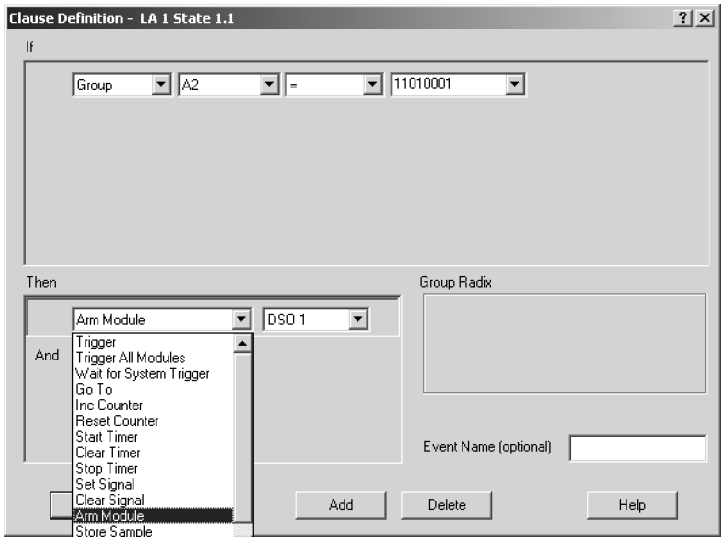


Figure 3-31: Clause Definition dialog box (Trigger Actions list box)

Table 3-6: Trigger actions

Action	Description
Trigger	Triggers the current module. When you use Trigger in the trigger program, you cannot use Trigger All Modules.
Trigger All Modules	Also known as a System trigger. This signal is also available at the System Trigger Out connector. When you use Trigger All Modules in the trigger program, you cannot use Trigger.
Wait for System Trigger	Causes this module to wait for a system trigger that is generated by another module.
Trigger Main	Available only on TLA7Axx modules, specifies that sample data will be stored in main memory. Only one type of main triggering (Trigger, Trigger Main, or Trigger System) can be used in the trigger program.
Trigger MagniVu	Available only on TLA7Axx modules, specifies that sample data will be stored in MagniVu memory. Trigger MagniVu can be used in conjunction with one of the main memory trigger actions.
Snapshot Current Sample	Available only on TLA7Axx modules, reloads the word recognizer. Snapshot data is not available during an acquisition therefore it is not be added to the status monitor.
Go To	Passes the program flow to a different trigger state. You can only use one Go To action in the clause definition.

Table 3-6: Trigger actions (Cont.)

Action	Description
Counter and Timer actions	Starts, stops, resets, or clears counters or timers. Counter 1 and 2 actions conflict with Timer 1 and 2 actions respectively. Counter/timer actions may conflict with counter/timer event usage.
Set and Clear Signal	Sets or clears one of the four internal system signals. You can use only one Set or Clear in a trigger program. The Set or Clear Signal is mutually exclusive with the Arm Module action.
Arm Module	Sends an Arm signal to another module. The other module begins running its trigger program. You can arm only one module in a trigger program. However, you can use actions throughout the trigger program. Arm Module is mutually exclusive with Set and Clear Signal actions.
Store Sample	Stores exactly one sample. Not available in Start/Stop storage mode.
Start & Stop Storing	Begins or ends storing of samples. Start and Stop Storing actions only appear when you select Start/Stop storage mode. Use Start and Stop Storing in conjunction with Start/Stop storage mode in the Trigger window. Available only in Start/Stop storage mode.
Do Nothing	Use as a placeholder when defining a complicated trigger program. Does not override other actions specified in a clause.
Don't Store	Available only on TLA7Axx modules, does not store this sample. Not available in Start/Stop storage mode.

Other Trigger Options. From the Trigger window, you can also make data storage and trigger position selections. In TLA7Axx modules, you have additional selections available for MagniVu storage rate, MagniVu trigger position, and Force Main Prefill.

Use the storage selections to avoid filling up the acquisition memory with data samples that do not interest you. You can use the storage selections to disqualify the unwanted data samples and fill memory only with the desired data.

Use the Storage box to select the default data storage rules for the module. Use one of the storage actions in the Then statement of the clause definition to override the default storage setting.

The example shown in Figure 3–32 is using conditional storage. Data is stored only when the specified event is true.

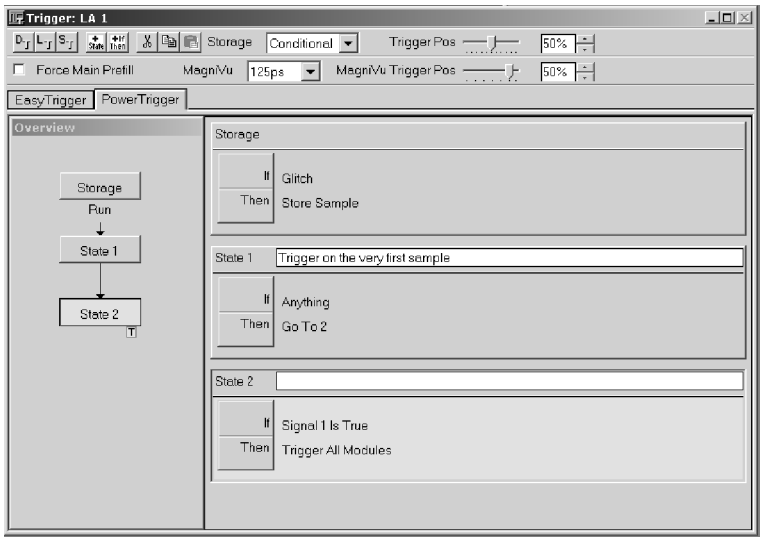


Figure 3-32: Using trigger storage

Table 3-7: Trigger storage

Storage option	Description
All	Stores all samples. You can exclude a sample from being stored by selecting the Don't Store action in the Then statement of the trigger clause. The trigger sample is always stored.
None	Does not store samples. You can explicitly store a sample by selecting the Store Sample action in the Then statement of the trigger clause.
Transitional	Stores samples only if one of the specified channel groups changes state. To select the channel groups that will detect a change in state for Transitional storage, click the Change Detect button, which is located in the Trigger Detail area of the PowerTrigger tab.
Conditional	Stores samples only if the storage clause is true. Program this clause in the same way as a regular trigger clause.
Start/Stop	Storage is controlled by the Start Storing and Stop Storing trigger actions in the Then statement of the trigger clause. Use the Start Storage/Stop Storage button that displays in the Trigger Detail area of the PowerTrigger tab to select whether storage is initially enabled.

The Trigger Position selects the amount of post-trigger data that is stored and determines the position of the trigger in the data record.

After a module has triggered, it continues to acquire data until it fills a specified amount of memory. The total memory depth that the module fills is set in the Memory Depth box in the Setup window. The proportion of data that is stored before and after the trigger is determined by the Trigger Position field. For example, if the Trigger Position is set to 10%, and the module triggers, then the module continues to acquire post trigger data until the remaining 90% of memory is filled.

If the trigger event occurs on any data sample before the specified amount of pretrigger data has occurred, then the logic analyzer triggers and begins filling memory with post trigger data regardless of the amount of pretrigger data specified. For example, if you set the trigger position to 50% and set the logic analyzer to trigger on a processor reset, start the logic analyzer, and then power on your target system, the logic analyzer will trigger. However, the logic analyzer memory will be filled only with post trigger data, not any pretrigger data. This is due to the trigger event, which has higher precedence, occurring before the pretrigger condition is satisfied.

Forced main prefill, available in TLA7Axx modules, sets the main prefill amount that must be met before the trigger state machine is activated.

When you use Force Main Prefill functionality, you specify which data samples are stored by selecting the desired sample type from the Storage drop-down list. Note that when you select either the None or Stop/Start storage settings, the Force Main Prefill check box and related functionality become unavailable.

System triggers produced by modules other than the TLA7Axx module override force prefill functionality and immediately start execution of the trigger state machine. An externally generated system trigger does not purge the force prefill data samples stored in main memory. However, the TLA7Axx module stops acquiring further prefill data samples and begins acquiring postfill data samples until main memory allocated for postfill data samples is filled.

With TLA7Axx modules you can adjust the MagniVu storage rate downward, allowing for a lower resolution of data samples from a longer time period.

The MagniVu trigger position, available with TLA7Axx modules, selects the amount of pretrigger MagniVu data to store and determines the position of the trigger in the data record. You can control the MagniVu trigger position independently of main trigger position by a set of controls in the advanced toolbar.

The MagniVu trigger position controls mirror the corresponding controls for main memory trigger position. They consist of a slider control, an edit box, and a spin control positioned beneath the main memory trigger controls. They behave like the main memory counterparts, except that the MagniVu trigger position is constrained by the MagniVu storage rate as shown in Table 3–8.

Table 3-8: MagniVu trigger position

Storage rate	Resulting trigger position constraint
125 ps	0% to 58% in 1% increments
250 ps	0% to 79% in 1% increments
500 ps	0% to 89% in 1% increments
1 ns	0% to 94% in 1% increments

***NOTE**. MagniVu data acquisition starts prior to the run line and fills memory before any possible trigger event. Therefore, there should be no need for a MagniVu forced prefill.*

Saving Trigger Programs

You can save trigger programs that you have created or modified for future use. When saving a trigger program from the EasyTrigger tab, use the Save Trigger button from the Trigger window toolbar to save your TLA file. This file contains trigger state information as well as information about the currently selected EasyTrigger program. If you do not use an EasyTrigger program as the basis for your trigger design, but instead use the PowerTrigger tab to develop a new trigger program, only the state information is saved.

Saving your trigger program requires that you specify both a filename and the name of the folder where you would like your customized trigger programs to reside. In addition, you can enter comments about trigger program construction or functionality in the dialog box.

Loading a Saved Trigger Program

You load a saved trigger program by clicking the Load Trigger button from the Trigger window toolbar. Then browse to the location where your trigger folder resides and select the desired trigger program. You can then view the loaded program from the trigger window. The TLA application displays the program you chose to load using the trigger tab from which the program was saved.

You can also load a trigger program from a list of recently used trigger program files. The logic analyzer maintains a list of the ten most recently used trigger files that you load by clicking Recent Trigger Files from the File menu, and then selecting the desired trigger file.

Setting Up the DSO Module

Before acquiring and displaying an analog waveform, you must first set up the DSO using the DSO Setup window. You can set the vertical, horizontal, and trigger parameters manually, or you can use Autoset for a quick automatic setup based on the input signal.

***NOTE**. The setup and data windows operate independently; you cannot change setup parameters by changing the data display. Once you acquire data, you can manipulate the display, but that will not change the input settings used to acquire the data. You must return to the DSO Setup window to change input settings, which take effect with the next acquisition.*

To open the DSO Setup window, go to the System window and click the DSO Setup button.

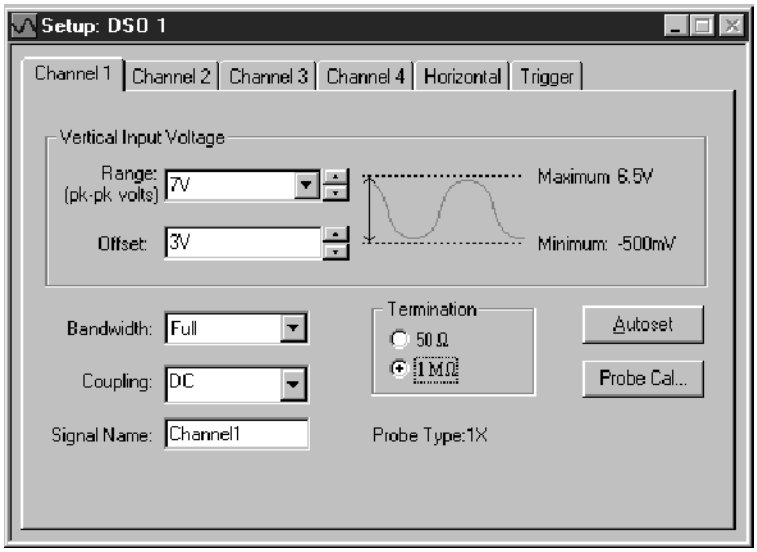


Figure 3- 33: DSO Setup window

DSO Probe Calibration

Probe calibration optimizes the signal path for this probe/channel/module combination. For maximum accuracy, execute Probe Cal if either of these conditions have occurred:

- The ambient temperature has changed more than 5 °C
- You reconnect the probes to different DSO module input channels

The Probe Calibration dialog controls all DSO probe calibration cycles and directs you to perform any necessary steps. You can calibrate all attached probes or only the probe on the selected channel.

***NOTE**. Passive or unknown probes are not calibrated.*

You can start a calibration cycle, view the progress of calibration, and see the results of calibration. Once calibration starts, the calibration cycle of a single probe cannot be stopped. After a calibration cycle completes, you can see the status of probe calibration.

To open the Probe Calibration dialog, go to the System window and click the DSO Setup button, select a vertical tab (Channel x), and click the Probe Cal button.

***NOTE**. You should execute the DSO module self-calibration if the ambient operating temperature has changed more than 5 °C since last calibration. Also, you should execute the self calibration once a week if vertical settings of 50 mV full scale or less are used. Perform self calibration after a 30 minute warm up.*

To open the Self Calibration tab from the System menu, click Calibration and Diagnostics. and then click the Self Calibration tab.

Autoset

Use Autoset when you need to see a signal in a circuit, but do not know the signal amplitude or frequency. Autoset automatically chooses the DSO setup values based on the input signal at the time you clicked the Autoset button.

Autoset works best on repetitive signals that do not have a DC offset component. If the Autoset setup does not display the waveform as you want it, you can easily change the setup manually.

To set the DSO input values based on the input signal:

1. From the System window, click the DSO Setup button.
2. Click the Autoset button from any tab in the DSO Setup window.

   The Autoset selections apply to all input channels, the horizontal setup, and the trigger setup, regardless of which Autoset button was clicked.
3. If the signal changes, or you move the probe to another signal, click Autoset again to reset the setup values.

Autoset affects only the DSO setup; it does not affect data window settings. You may need to adjust data window settings for optimum display of the data.

Vertical Controls

Use the vertical controls to adjust vertical input voltage parameters. See Figure 3–34.

To open the page containing the vertical controls from the System window, click the DSO Setup button and then select one of the Channel tabs.

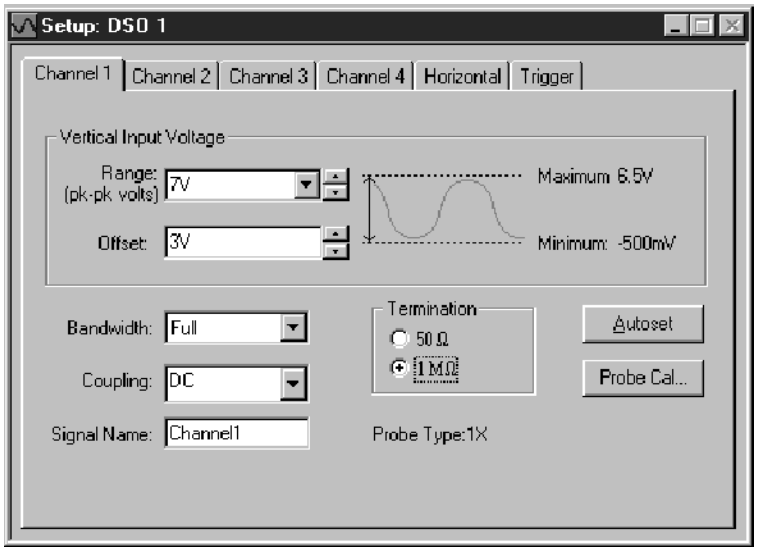


Figure 3-34: DSO Setup window vertical input settings

For best vertical resolution, set the range just slightly larger than the expected input signal. Autoset automatically sets the vertical range for the signal, assuming a 0 VDC offset.

Offset. Offset is the offset voltage applied to the probe. If Range is changed using the preset values, then Range also sets the Offset. The Offset default is 3 V for TTL signals.

Bandwidth. Bandwidth is the range of frequencies that can be acquired and displayed accurately. Your bandwidth selection sets the upper limit of frequencies that will be acquired and displayed. Bandwidth filters reduce unwanted noise and aliasing.

Coupling. Coupling selects how the input signal is coupled to the vertical input channel.

Horizontal Controls

Horizontal settings control the rate at which the data is sampled and the amount of data acquired. See Figure 3–35.

To open the horizontal page, from the System window, click the DSO Setup button and then click the Horizontal tab.

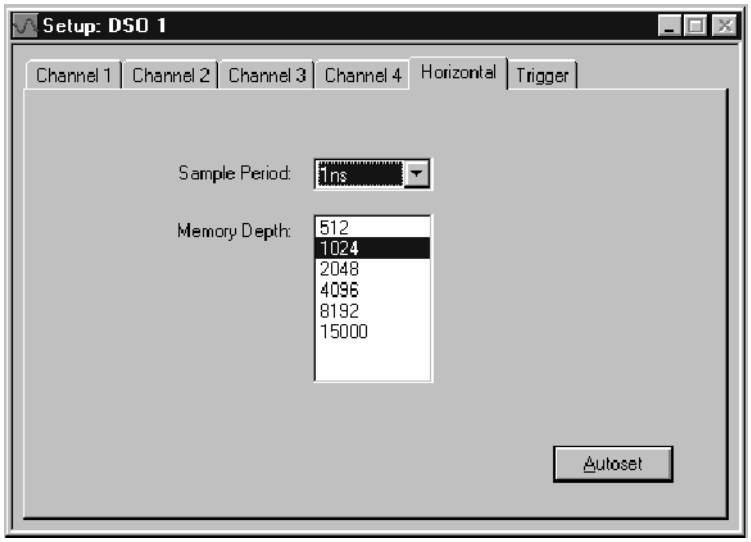


Figure 3-35: DSO Setup window Horizontal settings

Sample Period. The Sample Period sets the interval between successive samples in a waveform record. Choose a sample period that is fast enough that the waveform will not be aliased, and slow enough to provide the waveform record length that you need. For repetitive waveforms, you should set the sample period to at least five times faster than that of the waveform.

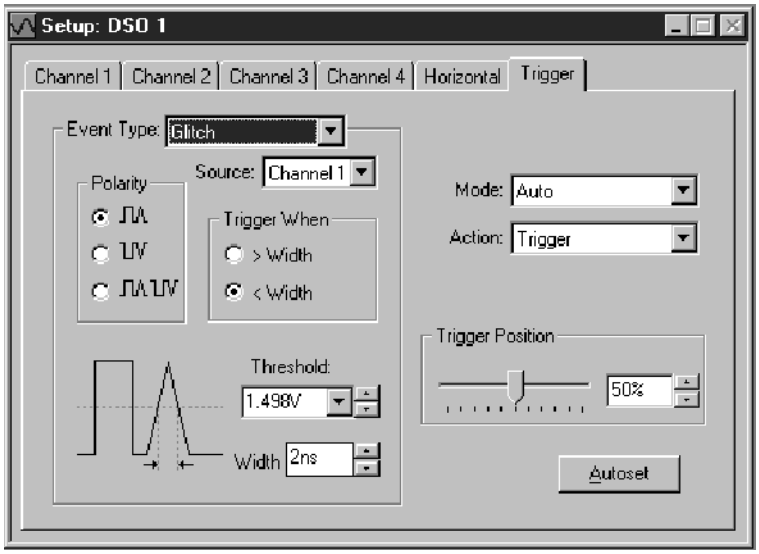
Memory Depth. The Memory Depth sets the total number of data samples to be acquired. If you do not need to use the full memory depth to acquire the data of interest, select a smaller memory depth to get faster acquisitions.

Trigger

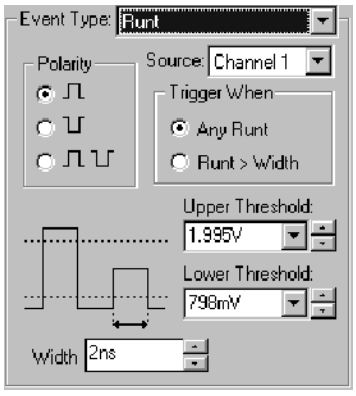
The DSO Trigger page contains all controls for setting DSO trigger events and actions. Threshold changes are recognized and executed immediately during acquisitions. Execution of all other controls are delayed until the next acquisition.

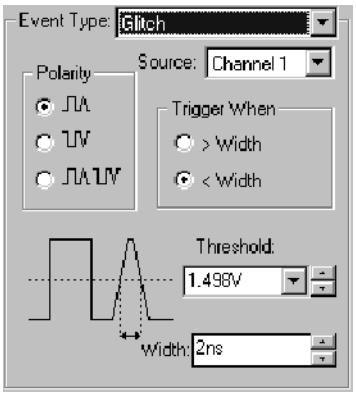
To display the Trigger setups from the System window, click the DSO Trigger button and then click the Trigger tab.

Select a trigger event from the list of event types, and then modify it for your application.



Event Type. Event Type selects the type of event the DSO will recognize as a trigger. Choose from the list of trigger event types. The following figure shows two of the available trigger event selections.



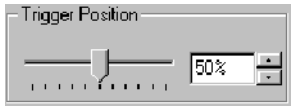


Mode. Mode selects whether the DSO waits for a trigger (Normal) or forces a trigger after a set length of time has passed without a trigger (Auto).

Action. Action selects what happens when a trigger is recognized. Choose from a list of actions. Actions include triggering the DSO, triggering all modules, or triggering and arming another module.

Trigger Position. Trigger position sets the amount of data in the data record that occurs before the trigger.

To set the Trigger Position, use the slider or enter a numeric value, as shown below.



Event-Based Selections. Depending on the trigger event you choose, other selections may become available. Refer to the online help for further information.

Setting Up the External Oscilloscope

The iView External Oscilloscope Cable allows you to connect your logic analyzer to an external oscilloscope, enabling communication between the two instruments. The Add External Oscilloscope wizard, which is available from the TLA application System menu, will guide you through the process of connecting the iView cable between your logic analyzer and external oscilloscope.

A setup window is also available to assist you in verifying, changing, and testing the external oscilloscope settings. Before acquiring and displaying a waveform, you must establish a connection between your Tektronix Logic Analyzer and external oscilloscope using the Add External Oscilloscope wizard.

Table A–73 in Appendix A on page A–70 includes a list of supported TDS oscilloscopes available at the printing of this manual. For a current list of supported TDS oscilloscopes, visit our web site at www.tektronix.com/la.

External Oscilloscope Setup

The Setup tab contains the external oscilloscope model number, the assigned GPIB address, and indicates whether the external oscilloscope is currently enabled. It also contains a Test button that allows you to confirm communication between the logic analyzer and external oscilloscope, and provides controls for viewing or modifying aspects of the external oscilloscope setup.

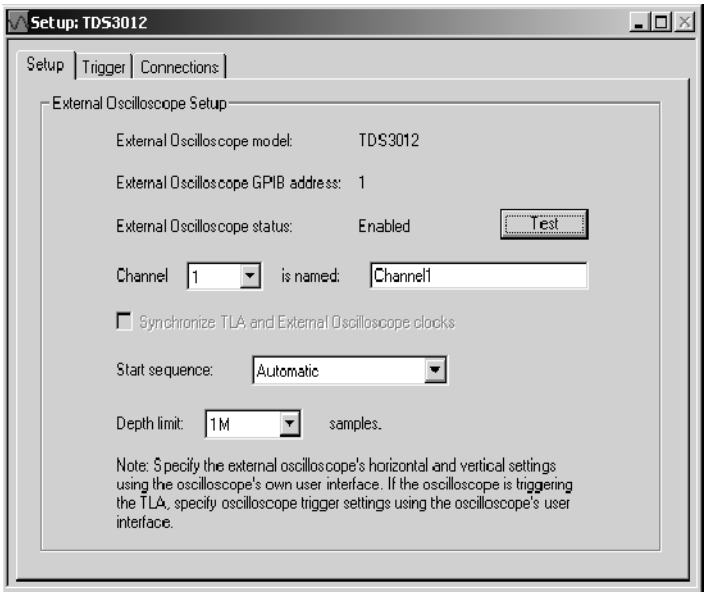


Figure 3-36: External Oscilloscope Setup tab

You can view and modify the following external oscilloscope setups:

Table 3-9: External Oscilloscope Setups

Setup	Description
Channel	Lists the available external oscilloscope channels.
is named	The name associated with the waveform channel. This name is used to identify external oscilloscope channels in the data windows.
Synchronize TLA and External Oscilloscope clocks	Check box that indicates whether the logic analyzer and external oscilloscope clocks are synchronized. This functionality is not available for all external oscilloscopes.
Start sequence	Indicates which instrument will start first.
Depth limit	The data depth limit that the logic analyzer uses to store external oscilloscope samples.

External Oscilloscope Trigger Settings

The Trigger tab contains controls for viewing or modifying external oscilloscope trigger events and actions.

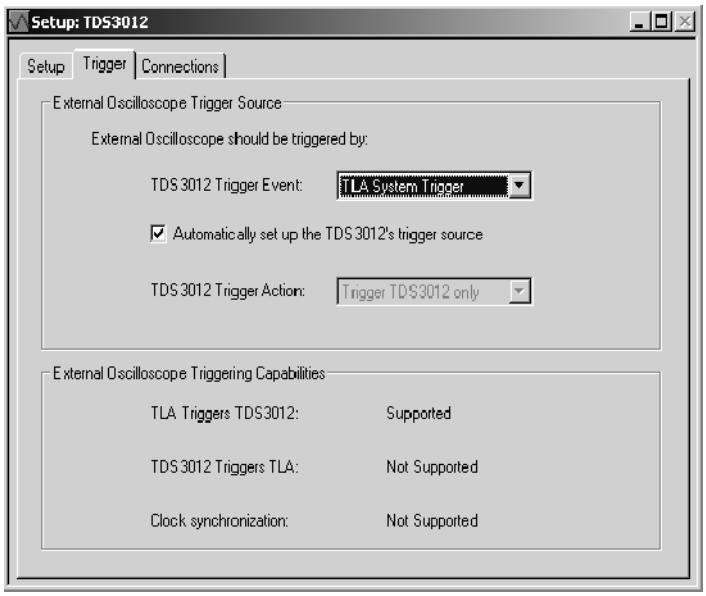


Figure 3-37: External oscilloscope trigger tab

You can view and modify the following external oscilloscope trigger settings:

Table 3-10: External oscilloscope trigger settings

Trigger setting	Description
Trigger Event	The instrument that will provide the trigger event.
Automatically set up the TDS trigger source	Check box that indicates whether the logic analyzer sets up the external oscilloscope trigger source.
Trigger Action	Determines whether or not the external oscilloscope triggers the logic analyzer after it has recognized a trigger event. This capability is not available for all external oscilloscopes.
TLA Triggers TDS	Indicates whether the external oscilloscope is capable of being triggered by the logic analyzer.
TDS Triggers TLA	Indicates whether the external oscilloscope is capable of triggering the logic analyzer.
Clock synchronization	Indicates whether you can synchronize the logic analyzer and external oscilloscope clocks.

External Oscilloscope Connections

The Connections tab contains diagrams that help you to confirm that your logic analyzer and external oscilloscope are physically connected correctly. Two diagrams are available for confirming the physical connection of both your logic analyzer and your specified external oscilloscope. Click the TLA Connections button to display the logic analyzer diagram, or click the TDS Connections button to display the diagram for the external oscilloscope that you specified in the setup wizard.

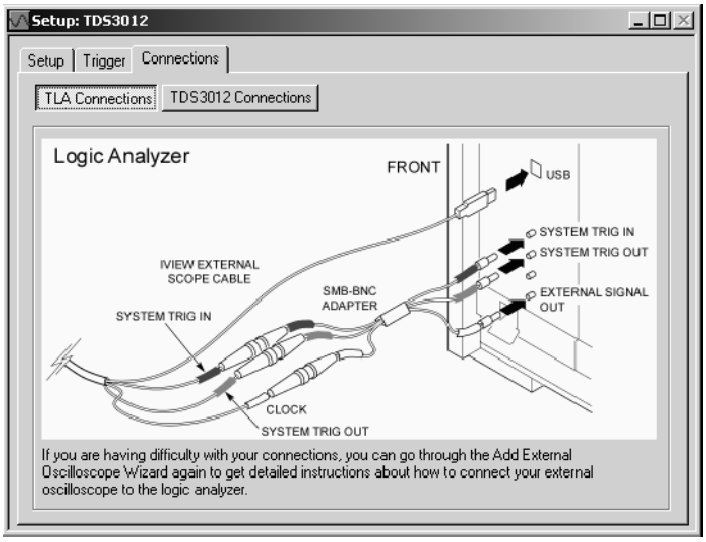


Figure 3-38: External Oscilloscope Connections tab

For further information about external oscilloscope setup, refer to the online help.

Setting Up the Pattern Generator Module

The pattern generator modules, like the LA modules, have a Setup window where you can specify the individual module setups, channel setups, probe setups, and signal setups. You should define these parameters before setting up the pattern generator program in the Program window.

Module Setup Window

Use the Module Setup window to define the channel mode, Run mode, clocking, and event setups. Figure 3–39 shows an example of the Module Setup window.

- Use the channel mode to select the speed and width of the logical module. Define the channel mode before defining other parameters. Otherwise, all module information will be lost when you change the channel mode.

- Set the Run mode to Step to output the patterns vectors one at a time. Use the Step button in the Status Monitor window to advance the steps. Set the Run mode to Continuous to output all vectors in a single step.
- Select the Hi-Z on Stop to cause the probes data and strobe outputs to go to a high-impedance state when the program stops.
- Use the Clocking to select an internal or external clock. When you select an external clock, you can also select the polarity and the threshold levels.
- Use the Event setups to filter out events, enable inhibit functions, and to define whether the pattern generator responds to events due to edges or levels.

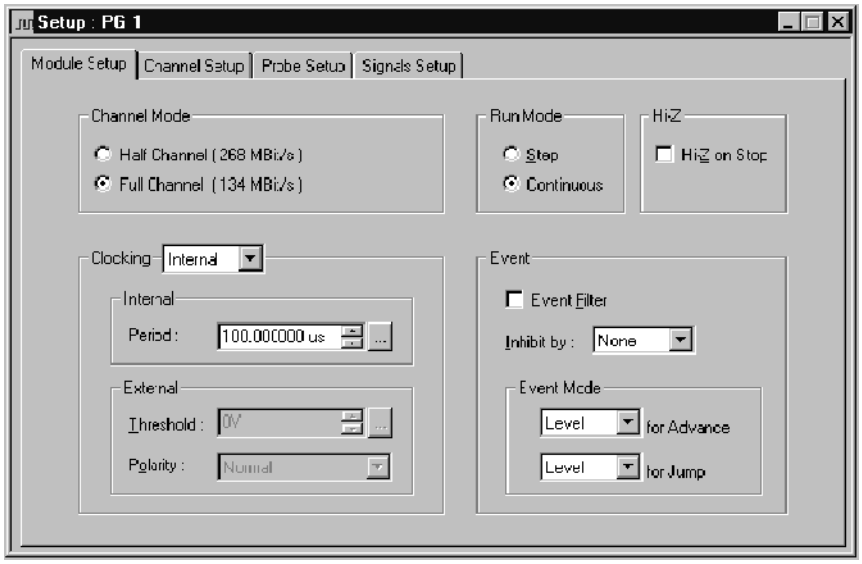


Figure 3-39: Module Setup window

Channel Setup Window

The Channel Setup window functions like the Channel Setup window in the LA modules. Use this window to define the channel group names, the logical grouping of channels, and the individual channel names. Figure 3-40 shows an example of the Channel Setup window.

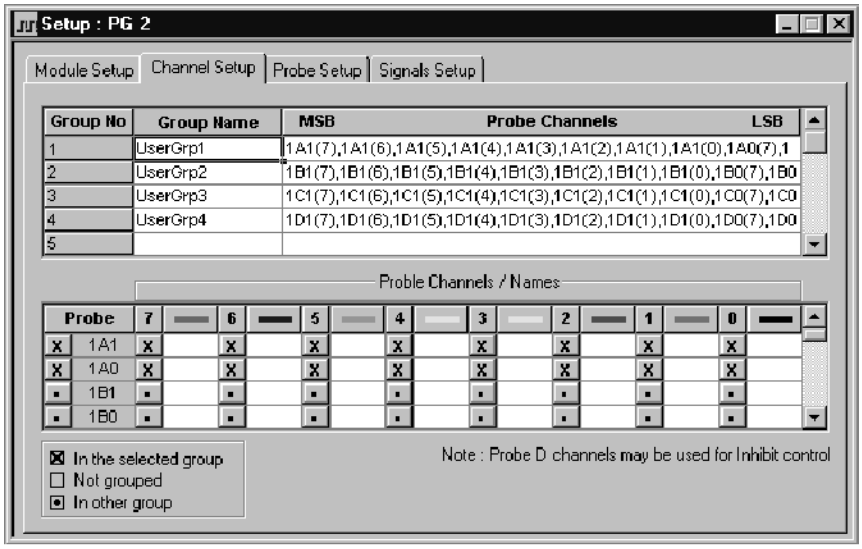


Figure 3-40: Channel Setup window

Probe Setup Window

Use the Probe Setup window to specify the probe details such as the output threshold voltage and inhibit information. Figure 3–41 shows an example of the Probe Setup window.

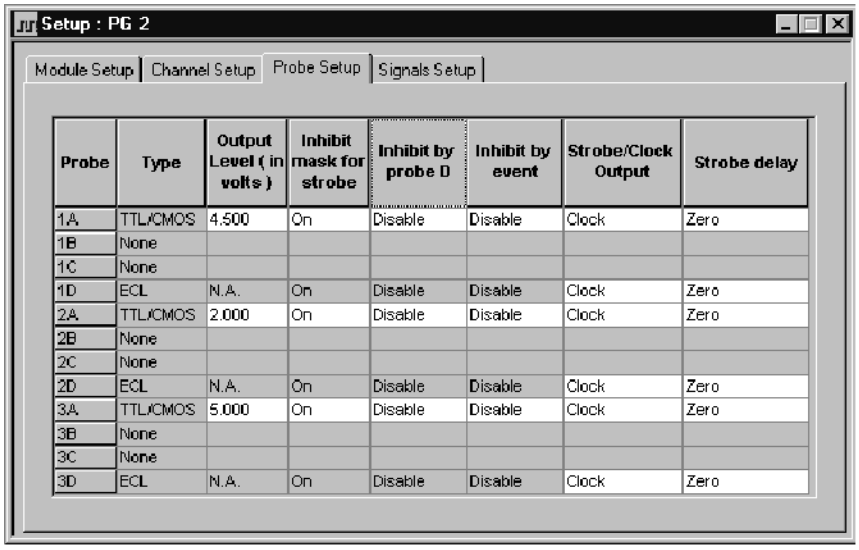


Figure 3-41: Probe Setup window

Signal Setup Window

Use the Signal Setup window to define the input and output signals. After defining these signals, you can use them in the Program window to control the flow of the pattern generator program. You can use one of the backplane signals as an input to the pattern generator module and another backplane signal as an output signal. For more information on using signals, refer to *Intermodule and External Signaling* beginning on page 3–71.

Figure 3–42 shows an example of the Signal Setup window.

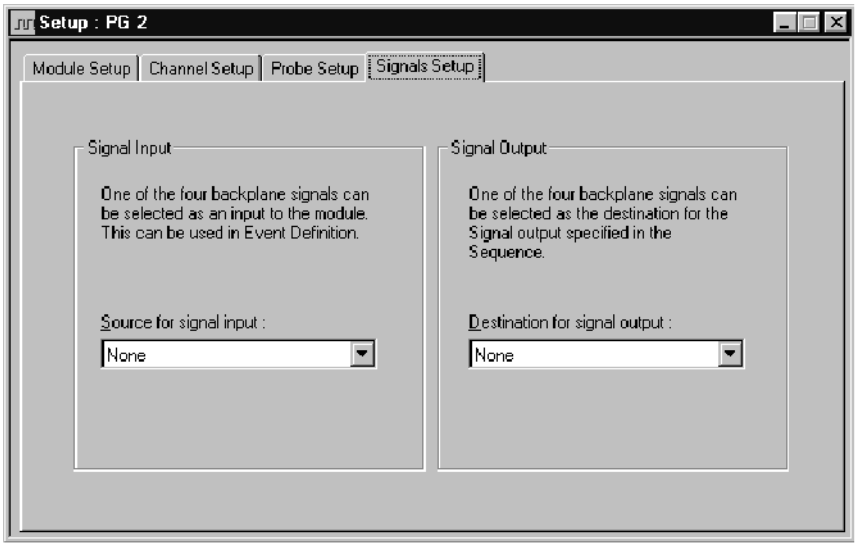


Figure 3-42: Signals Setup window

Setting Up the Pattern Generator Program

After you have defined the module setups, you can use the Program window to define the pattern generator program. Use the Program windows in the following sequence:

1. Use the Block Definition window together with the Listing or Waveform window to define the data blocks and the vectors in each block.
2. Use the Sequence Definition window to define a high-level sequence flow of the pattern generator program.
3. Use the Subsequence Definition window to define subsequences or macros. You can call these subsequences in the Sequence Definition window.
4. Use the Event Definition window to define how events are used with the pattern generator program.

Block Definition Window

Use the Block definition window to define blocks of output data. You can define the size of each block and assign each block a meaningful name (such as Init, Read Cycle, Interrupt). Each block has its own associated Listing or Waveform window. Figure 3–43 shows an example of the Block Definition window.

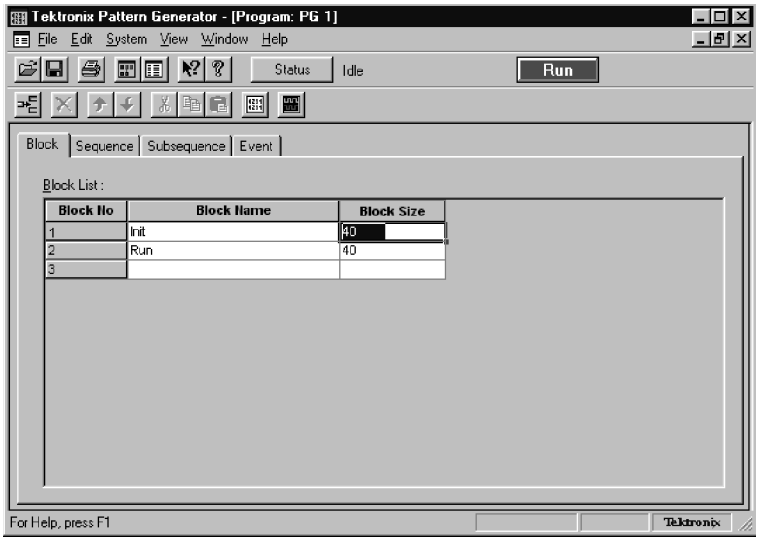


Figure 3- 43: Block Definition window

Use the Listing and Waveform windows to enter the data vectors. Click the Listing window icon to open the Listing window for the current block and enter the vector data. You can edit the vectors in either the Listing or Waveform windows.

Sequence Definition Window

After defining the data blocks, use the Sequence Definition window to create a high-level overview of the pattern generator program. Figure 3–44 shows an example of the Sequence Definition window. You can do the following tasks with sequences:

- Output the data blocks. Use the data blocks that you defined in the Block Definition window. You can specify how many times you want to output the data blocks.
- Determine the program flow. You can wait for an external event to occur before outputting the data blocks. You can also pass the program control to another sequence by jumping to a specific sequence label.
- Use Subsequences to execute or control the program flow. Subsequences are macros that you define in the Subsequence Definition window. For example, you can use a subsequence to output a read cycle five times and then output a write cycle before returning control to the main program sequence.

- Output a high or low signal to a defined event line. The event line is the one you defined in the Signal Setup window.

Each sequence has its own line. Use labels for each line to help with the program flow. Unless you set up a data block to be repeated an infinite number of times, the program flow will pass to the next sequence (or jump to a defined label). When the last sequence has been executed, the program flow stops.

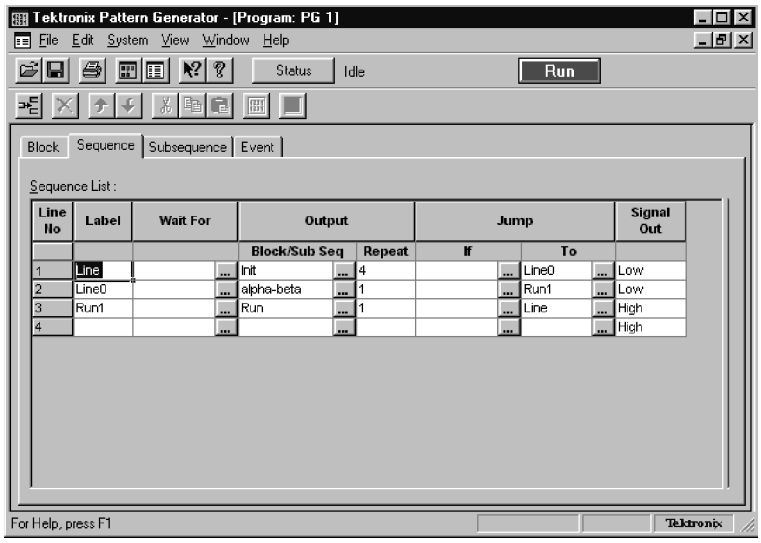


Figure 3-44: Sequence Definition window

After defining a sequence, you can display a graphical image of the sequence flow by clicking and dragging the vertical bar on the right side of the Sequence Definition window (see Figure 3-45).

The appearance of the sequence flow depends on the sequence definition. Each sequence line has its graphic (see Figure 3-46).

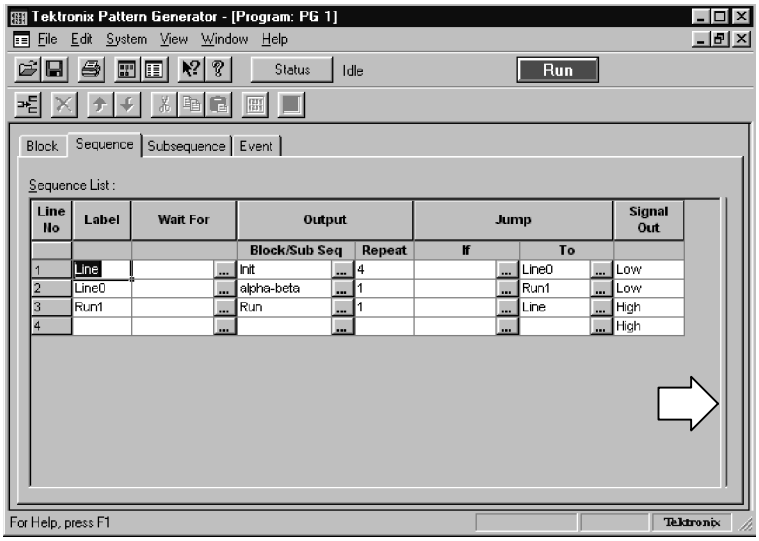


Figure 3- 45: Drag the vertical bar to the left to display the sequence flow graphic

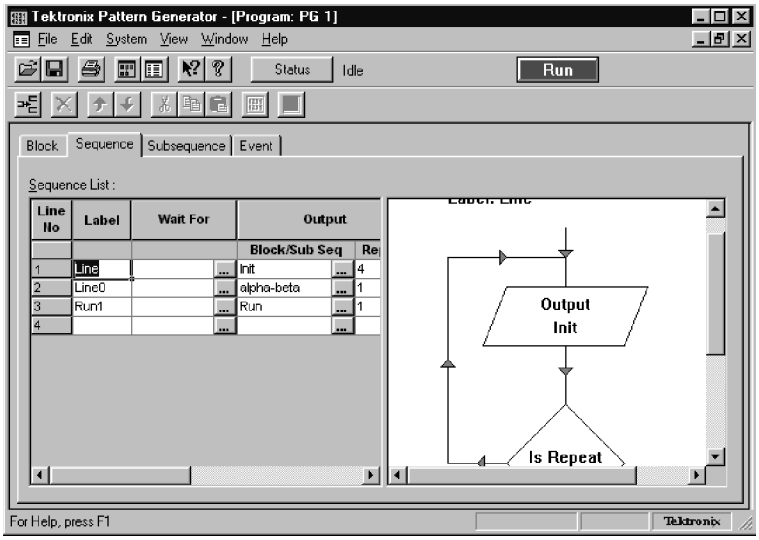


Figure 3- 46: Sequence flow graphic

Subsequence Definition Window

Use the Subsequence Definition window to define macros to use in the Sequence Definition window. Subsequences are useful for defining tasks that you may not want to appear directly in the Sequence Definition window.

Assign a name for the subsequence in the left side of the window. This name will appear in the Sequence Definition window. Define the actual tasks (data blocks) in the right side of the window. The block names are the ones you defined in the Block Definition window. Figure 3–47 shows an example of the Subsequence Definition window.

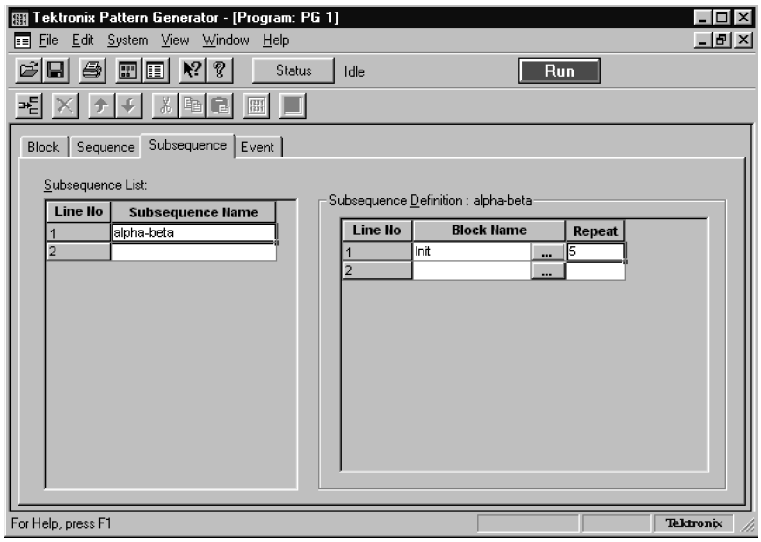


Figure 3-47: Subsequence Definition window

Event Definition Window

Use the Event Definition window to define events that you can use in the Sequence Definition window. Enter an event name in the left side of the window and then define events in the right side of the window.

Signal events refer to the input backplane input signal that you defined in the Signal Setups window. The Probe events refer to the input signals on each probe; each probe can have two event lines. Figure 3–48 shows an example of the Event Definition window.

The events in each row are logically ANDed together while the rows are logically ORed together.

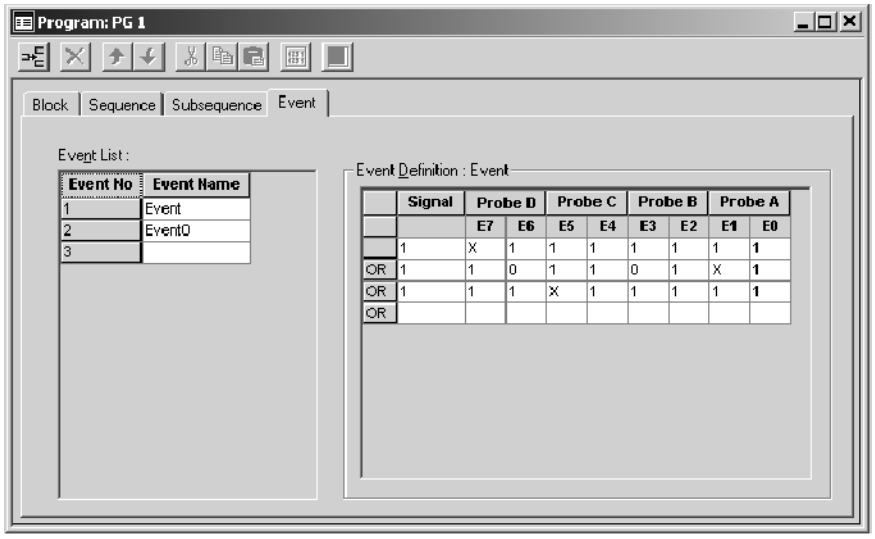


Figure 3- 48: Event Definition window

System Trigger

The system trigger is a global trigger event that forces all untriggered modules to arm immediately and trigger. Only one system trigger occurs per acquisition. When displaying data, the logic analyzer uses the system trigger as the primary reference point for the acquisition. The data windows show the system trigger and all module triggers. Module triggers can be forced by the system trigger or specified by module trigger programs.

The system trigger can be generated from any of several sources. Often, the system trigger is specified in a module's trigger program. Any module can specify the system trigger as a trigger action (Trigger All Modules). However, modules can specify trigger actions other than system triggers, and the system trigger does not have to originate from a module. The logic analyzer can also accept a system trigger generated by an external source. External system triggers are input through the SYSTEM TRIG IN connector. Regardless of the source of the system trigger, all modules must respond.

Use the System Trigger dialog box to specify triggering for the overall system. The following options allow you to change the trigger programs of all modules from one location.

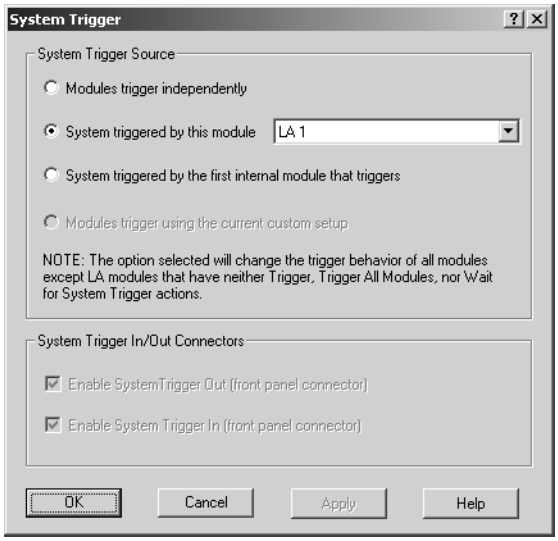


Figure 3-49: System Trigger dialog box

Table 3-11: System trigger source

System trigger source	Description
Modules trigger independently	Trigger All Modules and Wait for System Trigger actions in all trigger programs are changed to trigger actions.
Systems triggered by this module	The selected module's trigger program uses the Trigger All Modules action; all other programs will wait for the system trigger. Use the associated list box to select which module is used to trigger the system.
System triggered by the first module that triggers	Trigger actions in all programs are changed to Trigger All Modules. If the system has an external oscilloscope, it is set up to wait for the system trigger.
Modules trigger using the current custom setup	Enabled by default when your trigger setups do not match one of the previous system trigger options.
Enable System Trigger Out	Check box that enables or disables the System Trigger Out connector.
Enable System Trigger In	Check box that enables or disables the System Trigger In connector.

NOTE. *When you apply a system trigger option, your choice will only affect those modules that currently have a trigger action. Logic analyzer trigger actions include "Trigger," "Trigger All Modules," and "Wait for System Trigger." DSO and external oscilloscope modules are always affected because all of their actions result in triggering the module.*

It is not uncommon to have a condition in which the acquisition completed, but an explicit system trigger did not occur. (This means that there was neither an external system trigger, nor a system trigger generated internally by a module trigger program.) To ensure that a time reference exists for the acquisition, the logic analyzer must designate a system trigger. If no system trigger is generated during an acquisition (the modules are internally triggered), the logic analyzer designates the latest-occurring module trigger as the system trigger.

NOTE. *If an acquisition does not complete, due to one or more modules not receiving a trigger or not completing post-trigger acquisition, then you can manually stop the acquisition by clicking the Stop button. Clicking the Stop button effectively generates a system trigger and completes the acquisition.*

The system trigger is a latched event and it resets to a false state between acquisitions. The external system trigger input uses real-time gating and is only active (capable of latching system triggers) during the actual acquisition period.

The logic analyzer can also send an internally-generated system trigger out to the target system or to other test equipment through the SYSTEM TRIG OUT connector. All the external signal inputs and outputs operate at TTL levels. The connectors are located at the rear of the portable mainframe and at the front of the benchtop mainframe. For more information about external signaling capabilities, see *Intermodule and External Signaling* on page 3–71.

Arming Modules

Using the arm feature, you can use one module to control when another module accepts triggers. When module A arms module B, this means that module B does not begin looking for a trigger until it receives an arm signal.

Arming is accomplished through trigger actions. For the LA module, arming is specified in the Clause Definition dialog box; for the DSO module, arming is specified in the Trigger page. A module can arm any one of the other modules. The designated module can be armed by only one module. The same arming action can, however, appear multiple times within the same trigger program.

Arms are latched events that, once set, cannot be cleared until the acquisition is completed.

***NOTE**. For a single module, arming and internal signaling are mutually exclusive. You cannot simultaneously arm modules and set signals. You can test for a set signal (for example, If Signal X Is True), but you must designate an external signal for this purpose; otherwise you will be unable to set the signal when using the arming feature.*

Intermodule and External Signaling

The logic analyzer has four internal signals that you can use to set up trigger conditions between modules or to send or receive signals external to the logic analyzer. Use the Signals tab, shown in Figure 3–50, in conjunction with the module trigger programs to configure these signals for your application. The trigger programs determine when the signals occur. The Signals tab specifies characteristics of the signals.

***NOTE**. Observe the bandwidth and latency specifications when using internal and external signals. Refer to Tables A–19 and A–20 on pages A–18 and A–21 for information.*

To configure signals for your application from the System menu, click System Configuration and then click the Signals tab.

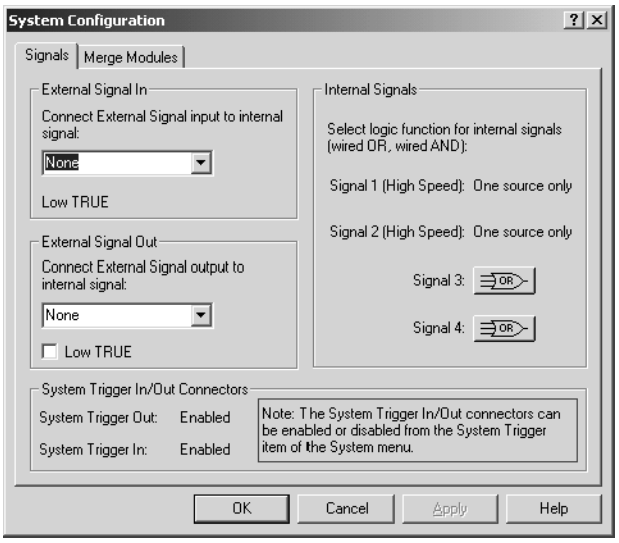


Figure 3-50: Signals property page

Only one module in the system can drive Signal 1 and only one module can drive Signal 2. When used with the expansion mainframe, all modules that drive Signal 3 should be in the same mainframe and all modules that drive Signal 4 should be in the same mainframe.

The logic analyzer and DSO modules use a logical expression (True/False) for Signals 1, 2, 3, and 4. However, the pattern generator module uses a physical expression (High/Low) for these signals. Figure 3-44 shows an example of the Sequence Definition window. Figure 3-44 shows an example of the Sequence Definition window. Use the tables in *Appendix C: Pattern Generator Physical-Logical Conversion* to convert physical expressions to logical expressions or vice versa.

Internal Signals

All logic analyzer modules can set and clear any of the four internal signals. The DSO can set but not clear any signal. The logical output of these signals can be used as an event in other modules' trigger programs. You can also connect the internal signals to the External Signal In and External Signal Out connectors on the mainframe, so that you can use an external signal as a trigger event or send a signal out when a trigger condition is met.

Internal signaling is for users with special trigger programming requirements. Internal signaling adds flexibility to trigger programming, but also adds complexity. When using internal signaling you must take care that the signals are correctly set and cleared, and that the trigger programs for all modules are compatible with regard to signal usage. Also, you must have correctly set the internal signal attributes in the Signals tab of the System Configuration dialog box.

Internal signaling is accomplished through trigger actions specified in the Clause Definition dialog box and the DSO Trigger tab.

***NOTE**. Arming and internal signaling are mutually exclusive. You cannot simultaneously arm modules and set signals. You can test for a set signal (for example, If Signal X Is True), but unless you have designated an external signal for this purpose, you will be unable to set the signal when using the arming feature.*

Signal Logic Function. To use internal signals, you must select which internal signal logic function is appropriate for your trigger program. Signals 1 and 2 (high speed) can be asserted by only one module each. For signals 3 and 4, the modules can be wired-OR or wired-AND. Selecting the OR function means that any module can assert the signal. Selecting AND means that all modules must set the signal for it to be asserted. The same logic applies to clearing signals.

The logic function applies only at a module level, not to multiple set/clear statements within a single module.

***NOTE**. Be careful when using wired-AND internal signals. If your trigger depends on an internal signal, all modules must set the signal for it to be asserted, or the trigger will not occur. If you change your trigger program, remember to update the logic function settings accordingly.*

External Signals

The logic analyzer can send and receive signals to/from the target system using the External Signal In and External Signal Out connectors on the mainframe. Use the External Signal In function to include a signal from your target system as part of the trigger setup. Use the External Signal Out function to send a signal to the target system or other test equipment when a trigger condition is met.

The connection from the module to the external connector is made by one of the four internal signals. You must designate which internal signal is to be used for this purpose.

The external signal connectors are located at the rear of the portable mainframe and at the front of the benchtop mainframe. The external signals all operate at TTL logic levels.

System Trigger In/Out Connectors

System Trigger In/Out Connector check boxes reflect the current state of the System Trigger In and System Trigger Out connectors, and can be used to both enable and disable them.

If an external scope is enabled, the options chosen in System Trigger Source can affect the values and sensitivity of the System Trigger In/Out checkboxes.

Merging Modules

A merged LA module set consists of a master module and up to four slave modules. A merged pattern generator module also consists of a master module and up to four slave modules.

LA Modules must have the same maximum state speed and must be physically connected in the mainframe before they can be merged by software. Modules must be adjacent and connected as described in *Appendix E: Merging Modules*.

Merged pattern generator modules are not physically connected in the mainframe but must be in adjacent slots in the same mainframe.

Modules that are capable of being merged, are shown in the Merge Modules property page with a merge button. See Figure 3–51.

To open the Merge Modules tab from the System menu, click System Configuration, and then click the Merge Modules tab.

To merge or unmerge modules, click the merge button between the module icons. You can unmerge the modules at any time for independent operation.

***NOTE**. After the LA modules have been physically merged, you should run the self-calibration procedure on the modules as a merged pair. To run the self-calibration procedure from the System menu, click Calibration and Diagnostics, and then click the Self Calibration tab.*

Merged pattern generator modules do not need to be calibrated as a merged pair.

In setup and data windows, merged module probe names use the following convention: master module probe names are displayed normally, and slave module probe names are prepended with an S. If you have more than two merged modules, the probe names are prepended with an additional number (such as S2). If the module is part of a five way merge, S, S2, S3, and S4 are prepended to probe-based names. No text is displayed for multiple waveform selections.

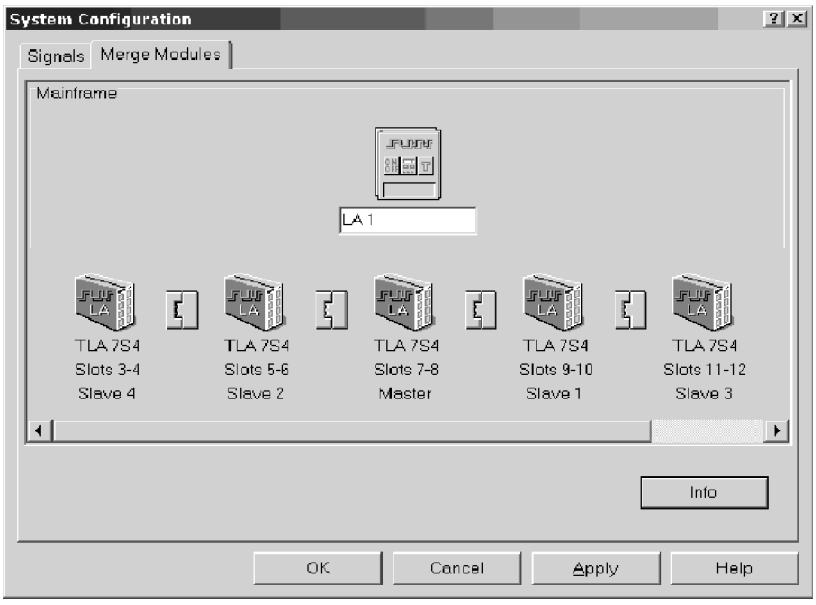


Figure 3-51: Merging modules

Saving and Loading Setups, Triggers, and Data

Once you set up the logic analyzer to your satisfaction, you will probably want to save the setup for future use. You can save setup information in two ways, via a saved system file or a saved module file.

Refer to the *Logic Analyzer Conceptual Model* described on page 2–33. The modules consist of the setup, trigger, and data associated with the physical LA or DSO module installed in the logic analyzer. The system consists of the setup and data for the whole logic analyzer, including all the modules and all data windows. See Figure 3–52.

When you save a module, you save all the setup and trigger information for that module. When you save a system, you save all the setup information for the system, including data window display settings, and all the module information, as well. In either case, you have the option of saving acquired data.

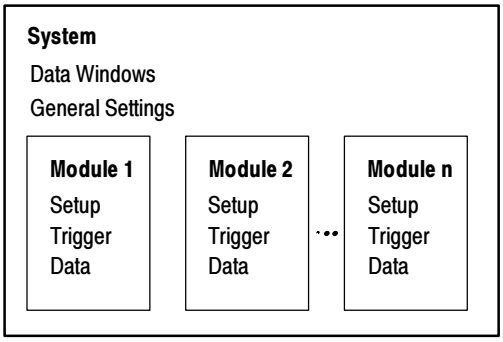


Figure 3-52: Logic analyzer conceptual model

Saving System and Module Files

Determine whether you want to save the information from a single module or from all modules. Select Save System or Save Module from the File menu.

In the Save As dialog box select one of the save options (see Figure 3–53):

- Click the Save all Acquired Data option button to save setups and all data.
- Click the Save only Unsuppressed Data option button to save the setups and unsuppressed data (only the data displayed in the Listing or Waveform window). Be aware that if you select this option, the suppressed samples are lost. If you want to save the suppressed samples select Save all Acquired Data.
- Click the Don't Save Acquired Data option button to save the setups without any acquired data.

Saved system and module file names have a .tla file name extension (*file-name.tla*). The initial default location for saved files is C:\My Documents.

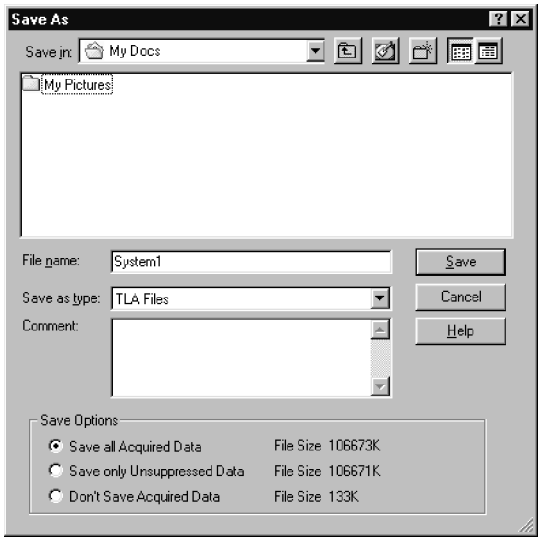


Figure 3-53: Saving a system with data

Loading Saved System and Module Files

The logic analyzer stores all the setup, trigger, and data information in just two types of files: saved module and saved system. However, the logic analyzer can extract different types of information individually from these files. From a saved module file, you have the option of loading any of the following:

- An LA module trigger program
- A module setup and trigger program
- Saved data from the module (accomplished by opening a saved data window; see *Opening a Saved Data Window* on page 3–89)

From a saved system file, you can load any of the following:

- Any of the previous module-related choices
- Full system setup, including data windows
- Saved data from one or more modules

You execute Load operations from the File menu. For module Load operations, you must first go to the module Setup or Trigger window before accessing the File menu.

Loading a System. When you load a system you load the full system setup, which includes setup, data, and trigger information for the logic analyzer and all installed modules. If the saved system file included data, the data windows and saved data are also loaded.

When you try to load a saved system with a different module configuration than your current system, the logic analyzer displays a dialog box (see Figure 3–54), giving you the option of using a suggested configuration. The suggested configuration is listed at the bottom of the dialog box. Click OK to accept the suggested configuration.

***NOTE**. If you load a setup that you saved with suppressed samples, the suppressed samples are not present in the setup.*

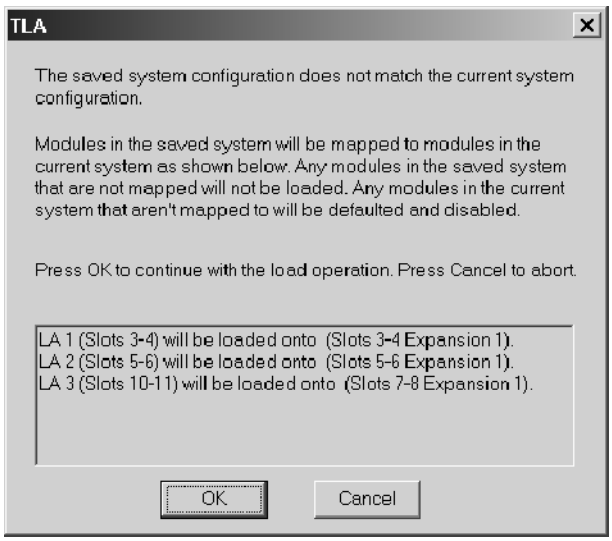


Figure 3-54: Loading a saved system that does not match the current system

If you click the Cancel button, the logic analyzer displays the Load System Options dialog box. Use this dialog box to load specific modules from the saved system. To load a module from the saved system, drag the module icon from the top of the dialog box to a module icon in the bottom of the dialog box. Figure 3–55 shows an example of the Load System Options dialog box.

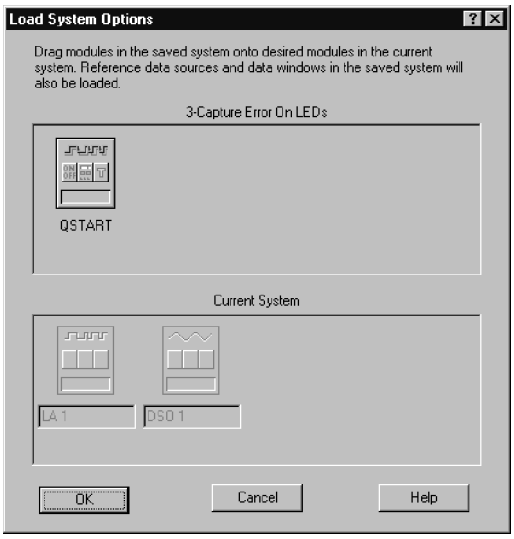


Figure 3-55: Load System Options dialog box

Loading a Setup and a Trigger Program. When you execute a Load System or Load Module operation, you load a saved setup and its related trigger program(s) to the logic analyzer (system) or specified module.

Loading Saved Data. You can load saved data using the Load Data Window selection in the Window menu. See *Opening a Saved Data Window* on page 3–89 for more information.

Loading a Saved Trigger. You can load an LA module trigger without loading a full setup. Saved system and module files contain trigger program information. When you load a trigger from the LA Trigger window, you can select a saved system or module file as the source. When you do so, the logic analyzer extracts only the trigger information from the file and loads it to the module.

***NOTE**. An error message displays when you are loading a setup file that contains a module self-trigger that will overwrite the existing system trigger setup. If you want to keep your current system-level triggering, click Yes. Otherwise, click No.*

Creating a Personalized Trigger folder. To create your own list of trigger programs, follow these steps:

1. Create a folder in a convenient location.
2. Go to the Trigger window containing the trigger program you want to save.
3. Go to the File menu and select Save Module As.
4. In the Save As dialog box, navigate to your trigger program folder.
5. Name the new file and use the Comment box to enter descriptive comments.
6. Make sure that Save Acquired Data is not selected.
7. Click Save.

Loading Default Settings

To return the logic analyzer to its default condition, go to the File menu and click Default System.

System Options

The logic analyzer provides several property pages where you can set or change system options. To access the system options, select Options from the System menu and choose the property page you are interested in.

- Use the Color tab to create, remove, and modify color schemes.
- Use the Defaults tab to specify the defaults throughout the application. The settings you enter will be the default settings when you create new data windows.
- Use the Preference tab to specify user preferences, such as changing the color of the Run or Stop buttons or hiding the Status bar.
- Use the Presets tab to view and modify preset names and values such as probe threshold voltages and DSO vertical range or vertical offset values.
- Use the Start-Up tab to select which system setup (such as a previous system or a saved system setup) to open after you power on the logic analyzer.
- Use the System Source Files tab to define the location of source files and suffixes used to create new Source windows.

Menu Shortcut Keys

You can use the shortcut keys listed in Table 3–12 to manipulate menus and edit windows. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

Table 3-12: Menu shortcut keys

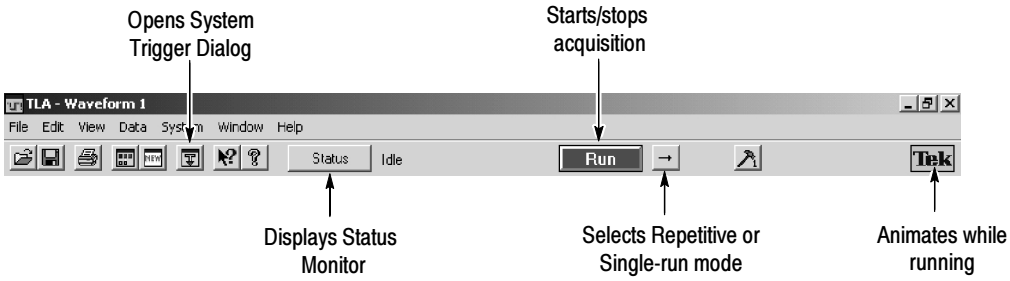
Desired action	Key combination
File menu	
Return system to the default setups	CTRL + D
Load a saved system	CTRL + O
Save a system setup	CTRL + S
Print the active window	CTRL + P
Edit menu	
Cut a selected item to the clipboard	CTRL + X
Copy a selected item to the clipboard	CTRL + C
Paste items from the clipboard	CTRL + V
Undo edit	CTRL + Z
Data menu	
Search backward	CTRL + B
Search forward	CTRL + F
System menu	
Display the Status Monitor	CTRL + M
Run or Stop	CTRL + R
Window menu	
Create a new data window	CTRL + N
System	F9
Next Setup	F10
Next Trigger	F11
Next Data	F12

Acquisition

When you start an acquisition, all modules start acquiring data together. (Exceptions are when one module has been programmed to arm another or when a module has been turned off.) Modules stop acquiring data individually, according to their trigger programming.

Starting and Stopping Acquisition

You control acquisition from the Control bar, shown below:



1. In the Control bar, click the System Trigger button to define system trigger parameters.
2. In the Control bar, click Run to start an acquisition.
3. The Tek icon on the right animates while the logic analyzer runs. Point at this icon with the mouse to display a tooltip showing the instrument status.
4. Wait for the logic analyzer to trigger and display data, or click Stop to manually stop an acquisition.

There are two ways to acquire data: Single-run or Repetitive mode. Within Repetitive mode, you can specify the following three conditions:

- Save Module and Data
- Stop if Compare with Reference is Equal or Not Equal
- Stop After N Acquisitions

When comparing acquisition data against reference data, you can view the results in either a Listing window or in a Waveform window.

Single Run Mode

In Single-run mode, the logic analyzer automatically stops acquiring and displays data when it fulfills the setup conditions. Use Single-run mode to find and display a specific event.

During acquisition, the logic analyzer monitors the data, looking for the events you specified in the Trigger windows. When the specified events occur, the logic analyzer responds according to the selections you made in the Setup and Trigger windows.

Repetitive Mode

In Repetitive mode, the logic analyzer keeps acquiring data until you click Stop or until it fulfills the stop conditions.

You can use Repetitive mode as follows:

- To observe the same waveform or listing for a period of time
- To stop after a set number of acquisitions for a period of time and look for differences

After each acquisition you can have the logic analyzer do the following tasks:

- Save the system or module setups and data
- Export the data to separate files or overwrite the same file
- Compare the acquisition data against data in another LA module or a saved LA module file
- To open a file or execute a set of defined tasks after the acquisition is complete. For example, you can execute a command such as sending email or paging you that the logic analyzer has stopped.

Select Repetitive Properties from the System menu to select the different options for the Repetitive mode. Figure 3–56 shows an example of the Repetitive Properties dialog box.

NOTE. *You can minimize the time between acquisitions by specifying compare conditions under the LA Setup window, deleting (not just minimizing) all data windows, and then starting the logic analyzer. When the logic analyzer fulfills the compare conditions, you can create a new data window with the New Data Window wizard to view the data.*

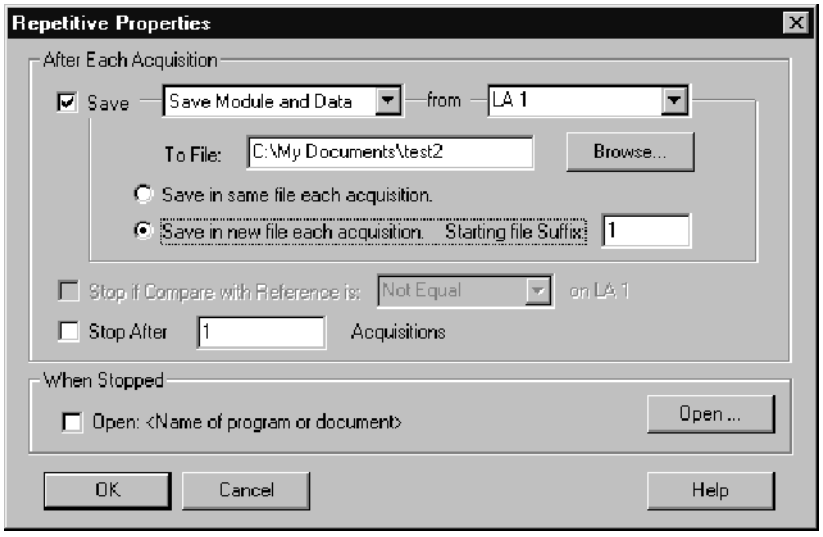


Figure 3-56: Defining setups for Repetitive mode

Viewing Acquisition Activity

While the logic analyzer is acquiring data, you can check its progress to see how much data it has acquired or to view channel activity.

Use the Status Monitor for a brief summary of acquisition, trigger, and data storage progress. See Figure 3–57.

To display the Status Monitor click Status on the Control bar.

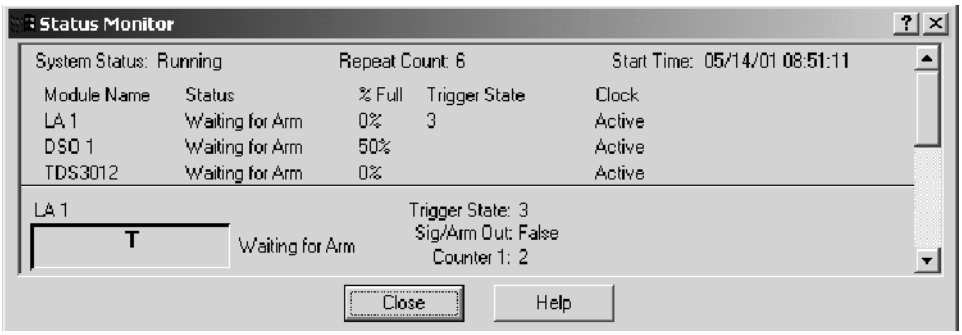


Figure 3-57: The Status Monitor

The Status Monitor is also useful to debug a trigger program. From the Status Monitor you can view the current status of various resources of the logic analyzer during acquisition. Be aware that rapid changes in trigger state, counter

values, timer values, and the internal signals cannot be accurately displayed in real time in the Status Monitor.

If the Logic Analyzer Does Not Trigger

If the logic analyzer does not trigger, you should check the following:

- Check that your target system is powered on.
- Check the System window to verify that required modules are turned on.
- If the module has correctly clocked data, acquired the specified events, triggered, but has not stopped, the module probably has not acquired enough additional data to fill acquisition memory. Click Stop to manually stop the acquisition, and then change the module Memory Depth (reduce) or Trigger Position (increase).

LA Module

The following conditions apply to the LA module only:

- Check the Status Monitor for an external clock warning. If the LA is not receiving an external clock, the Status Monitor displays the following message: External Clock Source Idle.
- Check for signal activity at the probe tip. If there is no activity, check the probe connections.

  Check the clock signal to make sure that the LA module is actually clocking data. Problems with the clock signal can impact setups using external clocking, custom clocking (microprocessor support packages only), or storage qualification.
- Similar to the previous item, check clock qualifier signals and clocking equations.
- Check the threshold voltages for probes and clocks.
- If the module is correctly clocking data and the data events have occurred, but the trigger program did not generate a trigger, you should check the trigger program itself. The trigger program might not be reaching the state that generates the trigger. Use the Status Monitor to track trigger program progress and identify the state in which trigger progress stops.
- Check the complexity of your trigger program. If your trigger program is too narrowly defined, or over-specified, the trigger program might not acquire the desired data or might not trigger. A less-specific trigger program might acquire the desired data and also verify that you have set up the proper clocking and threshold levels.

DSO Module

The following condition applies to the DSO module only:

- Check the trigger Mode setting. If Mode is set to Normal, and the data does not meet the trigger conditions, the module will not trigger. (Conversely, if Mode is set to Auto, the module will trigger after a set length of time, even if the specified data does not occur.)

Arming or Intermodule Triggering

The following conditions apply only if you are using arming or intermodule triggering:

- Internal signal logic function. If your trigger depends on setting an internal signal, and that signal has been set to Wired-And, all modules in the system must set the signal or it cannot assert.
- If any modules are turned off, check that the trigger program is not waiting for input from an inactive module.

First Transition Indication Problems

Because the logic analyzer does not clear the first transition indication, check that the LA modules always show a first transition indication (even if there are no probes attached).

To avoid triggering on a false first transition indication, set the first state to “If Anything, Go to Next State.” This will use a state, but it ensures that you do not trigger on a false transition indication.

Display

To view acquired data, open one of the data windows. The Listing window and the Waveform window are the data windows that you will use for most applications; see Figure 3–58. You can also create Source windows to use with high-level language support applications or Histogram windows to use with performance analysis applications. You can have multiple data windows to display different data or different views of the same data.

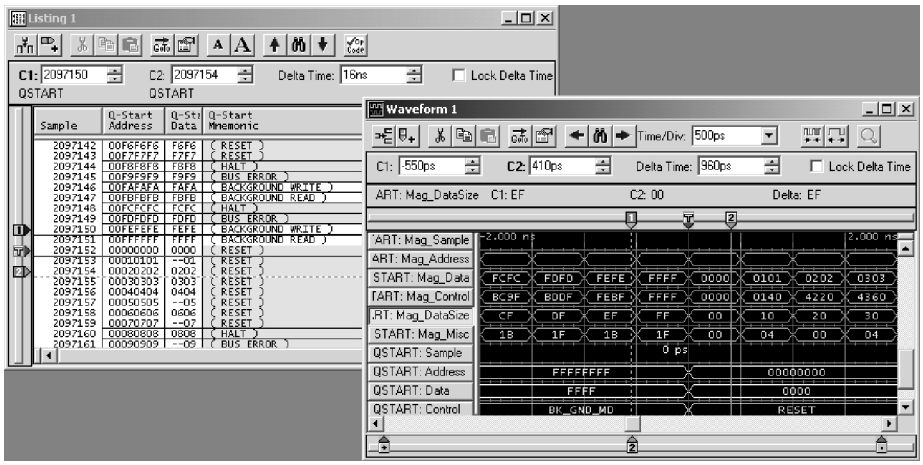


Figure 3-58: The Listing and Waveform windows

Setup window and data window controls act independently of one another. Controls in the Setup windows affect how the modules acquire data. Controls in the data windows affect how the acquired data is displayed.

***NOTE**. Logic analyzer Listing and Waveform windows are different from pattern generator Listing and Waveform windows. LA Listing and Waveform windows display acquired data from the target system while pattern generator Listing and Waveform windows are used to set up data to send to the target system.*

Opening an Existing Data Window

The System window shows the relationship between the modules and the data windows.

- To open a data window, go to the System window and select a data window button. See Figure 3–59.
- To see which modules supply data to a data window, go to the System window and click the data window label.

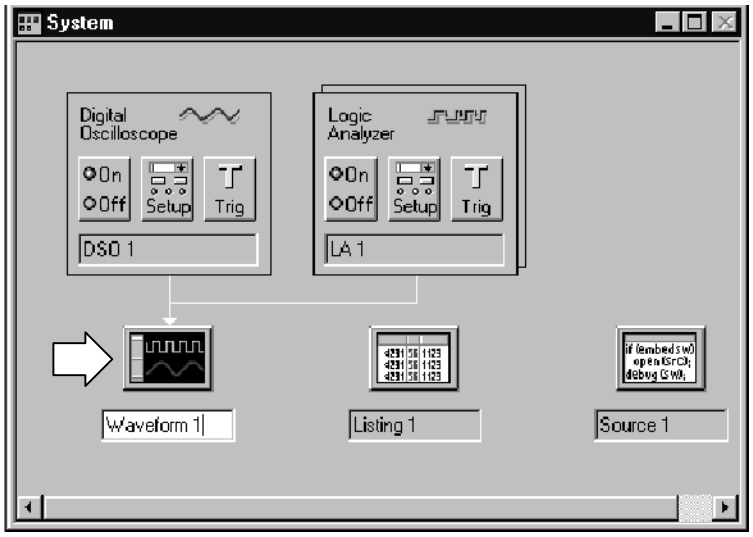


Figure 3- 59: Opening a data window

Opening a Saved Data Window

To open a window displaying data from a saved system file, do the following:

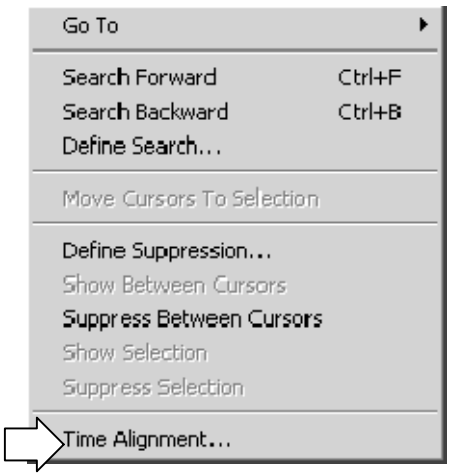
1. From the Window menu, click Load Data Window.
2. Click the Browse button to search for the file or enter a path to the file in the text box.

***NOTE**. The saved file must be a saved system file.*

3. Once the file is found, click the Open button.
4. Select the data window to load.
5. Click OK.
6. If the data window name is not unique, you will be prompted for a new name. Enter a name and click OK.

Aligning Saved Data with Current Data

Saved data and current data are time-correlated by aligning their system triggers. You can manually adjust this alignment using the Time Alignment dialog box. To access the Time Alignment dialog box, go to the Data menu and click Time Alignment, as shown below.



Creating a New Data Window

Use the New Data Window wizard to create a new data window for the data you want to display. You can select data from any module, a saved system file, or saved module file. See Figure 3–60.

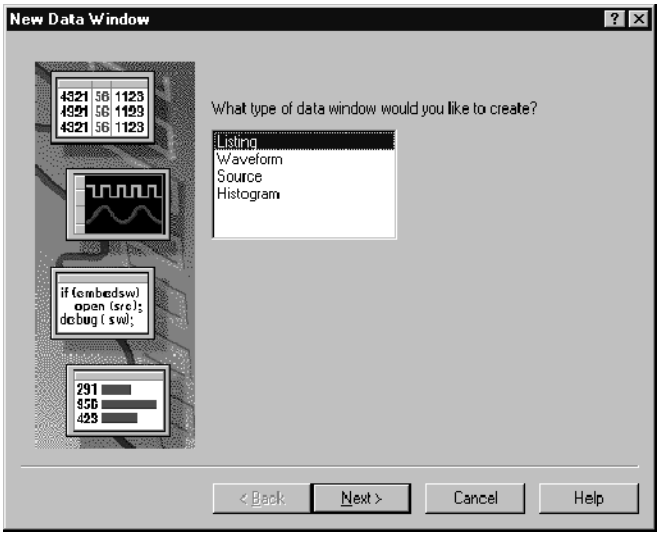
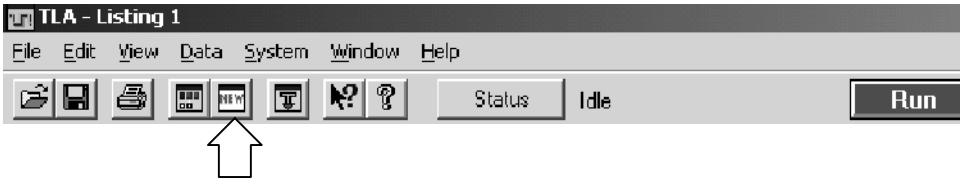


Figure 3- 60: New Data Window wizard

Create a new data window as follows:

1. Click the New Data Window icon in the toolbar.



2. Select the appropriate window type and click the Next button.

NOTE. *The contents of the New Data Window wizard will vary depending on the type of data window that you are creating.*

3. For each page in the wizard, enter the required information and click the Next button.

4. On the last page, enter the name for the data window or use the default name and then click the Finish button.

General Purpose Data Window Shortcut Keys

You can use the general-purpose shortcut keys listed in Table 3–13 to move data and cursors in data windows. You should also refer to the discussions of shortcut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- Arrow keys with the Control (CTRL) key move the active cursor.
- The Shift key increases movement by a factor of 10.

Table 3-13: General purpose data window shortcut keys

Desired action	Key combination
Scroll data up 10 pages	Shift + Page Up
Scroll data down 10 pages	Shift + Page Down
Scroll data to the top of the window	Home
Scroll data to the end of the window	End
Move active cursor up one page	CTRL + Page Up
Move active cursor down one page	CTRL + Page Down
Move active cursor to the top of the data	CTRL + Home
Move active cursor to the end of the data	CTRL + End
Move active cursor up 10 pages	CTRL + Shift + Page Up
Move active cursor down 10 pages	CTRL + Shift + Page Down
Move active cursor to the top of the data	CTRL + Shift + Home
Move active cursor to the end of the data	CTRL + Shift + End

Waveform Window

Use the LA, DSO, or External Oscilloscope Waveform window to display and evaluate acquisition data. You can display internal DSO waveforms, external oscilloscope waveforms, and LA waveforms simultaneously. Each window contains a data area, waveform labels, marks and several tool bars that allow you to measure and manipulate your waveforms. See Figure 3–61 for an example.

For the LA module, data values for each channel are shown as a digital (two-state) waveform. Logic level low is drawn at the bottom of the waveform area while a logic high is drawn at the top of the waveform area. For the DSO module and the external oscilloscope, data values for each channel are displayed as an analog waveform.

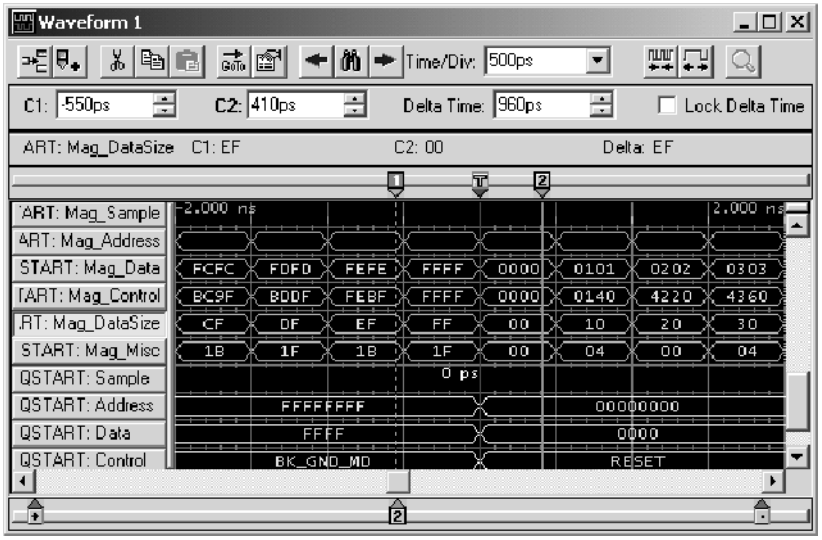


Figure 3-61: Waveform window

Types of Waveforms

Several types of waveforms can be displayed in the Waveform window, as shown in Figure 3–62.

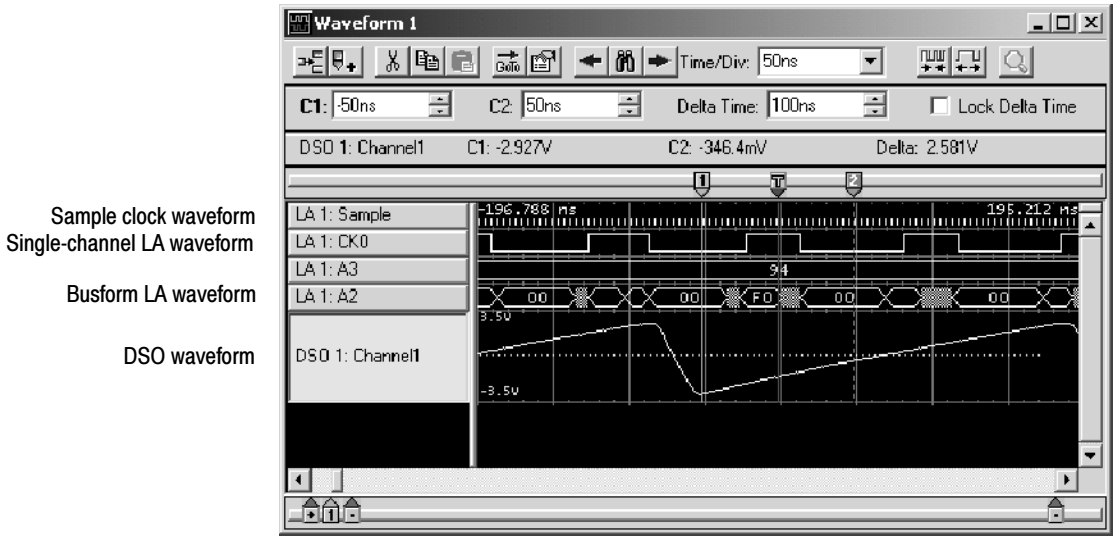


Figure 3-62: Waveform types

Sample Clock Waveforms

Each module that contributes current data to the window has its own sample clock waveform. The sample clock waveform consists of a row of short vertical tick marks placed along the time axis at each display point that represents an actual acquired sample for the module.

Single-Channel LA Waveforms

Digital timing diagrams that represent a single LA channel.

Busforms

Busforms display the value of an LA module channel group.

Magnitude Waveforms

Magnitude waveforms plot the numeric value of a channel group on a vertical axis over a period of time. For example, you can use magnitude waveforms with A/D and D/A applications for viewing the RGB components of a digitized video signal. Figure 3–63 shows such a component.

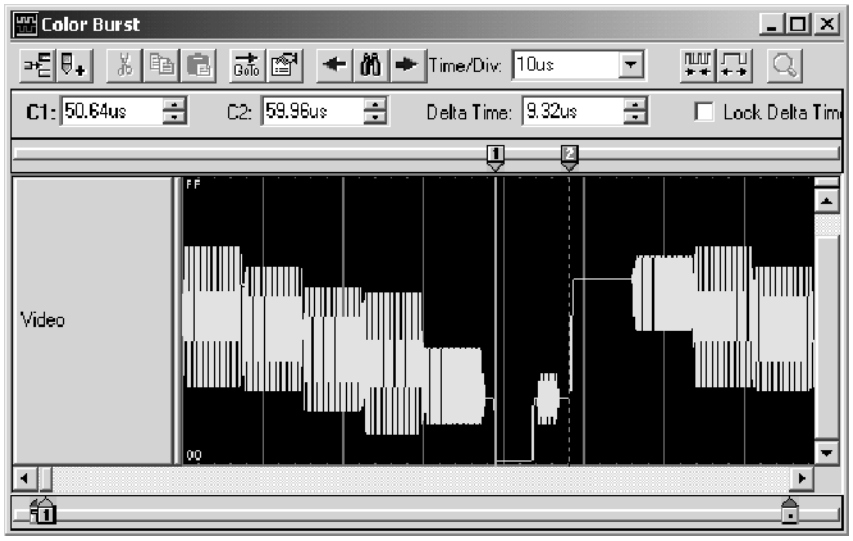


Figure 3-63: Magnitude waveform

DSO Waveforms

DSO waveforms are analog timing diagrams that represent a single DSO channel.

The size of the DSO waveform depends on signal size and the input voltage range selected in the DSO Setup Window.

Range readouts for DSO waveforms are located at top and bottom left of the waveform. The range readouts show the maximum and minimum vertical input voltage settings for the waveform. See Figure 3–64.

The ground line appears as a horizontal dotted line through each DSO waveform. If ground is outside the bounds of the waveform, the line is not shown.

The trigger threshold is indicated by a “T>” at the right side of the waveform. Set the trigger threshold in the Trigger page of the DSO Setup window.

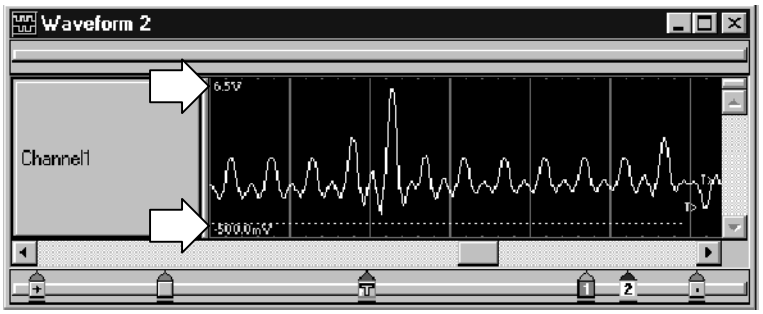


Figure 3-64: Range readouts

Reading the Waveform Indicators

Data marks, cursors, and other indicators help you navigate and identify the data. Figure 3–65 and Table 3–14 identify and describe data window marks.

To move cursors or marks, drag the cursor and mark handles. Trigger marks and Begin/End data marks cannot be moved. For more information on using marks, refer to the online help.

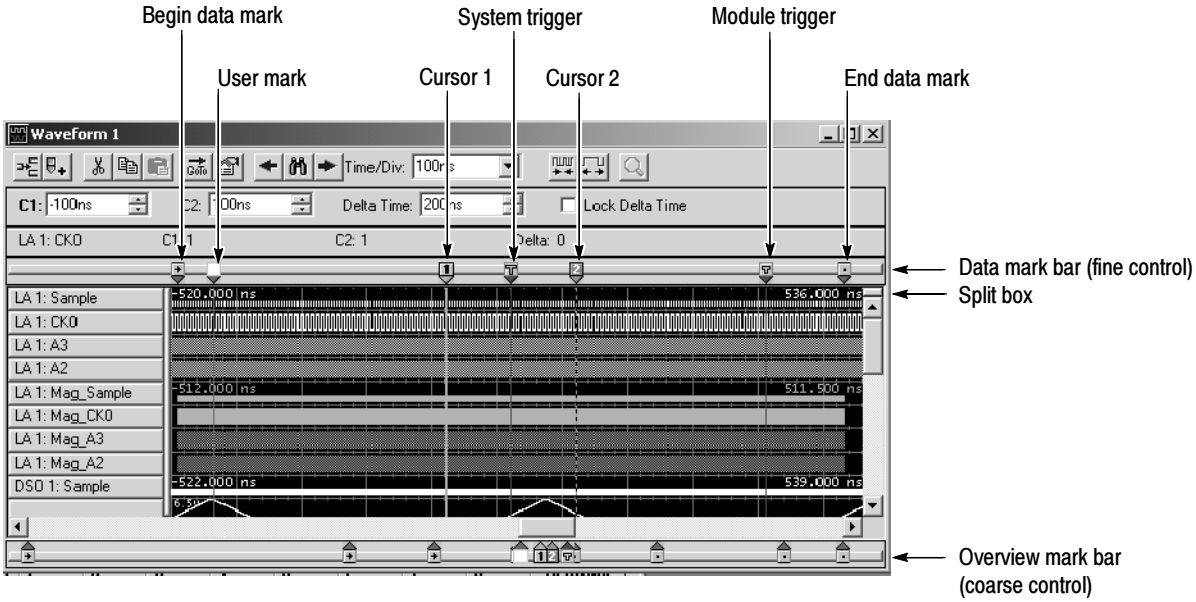


Figure 3-65: Waveform window cursors and marks

Table 3-14: Waveform window cursor and mark summary

Mark	Name	Description
	System trigger	The system trigger is the reference point for the acquisition. Timing and location information is relative to the system trigger. Trigger marks cannot be moved. Under some conditions the system trigger associated with a module's data might not be displayed in the data window. If the system trigger was caused by another module, whose data is not included in the current display, then the system trigger is not shown. Nevertheless, all time measurements still relate to that system trigger, even if it is not shown. The system trigger associated with the current data is called the active system trigger. The system trigger associated with saved data is called the reference system trigger. The active system trigger is indicated by a yellow T; the reference system trigger is indicated by a gray T.
	Module trigger	The point at which the module triggered. Trigger marks cannot be moved.

Table 3-14: Waveform window cursor and mark summary (Cont.)

Mark	Name	Description
+ ▪	Begin data / end data	The start and end of a module's data record. These data marks cannot be moved.
1 2	Cursors 1 and 2	Moveable marks used for visual reference and for data measurements.
☐	User mark	User-created marks. Use marks to make specific data more easy to identify and find.

Zoom Box

Use the Zoom box feature (see Figure 3-66) to zoom on waveform details with a click and drag of the mouse.

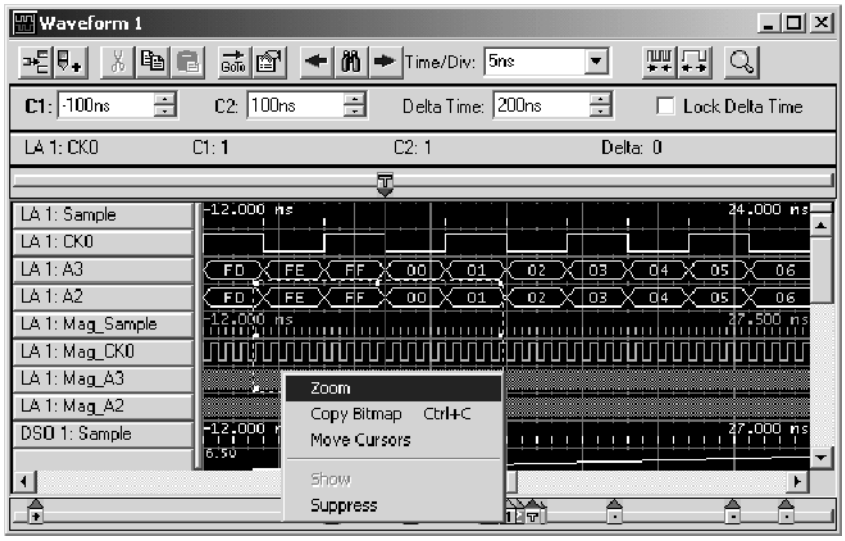


Figure 3-66: Waveform window zoom box

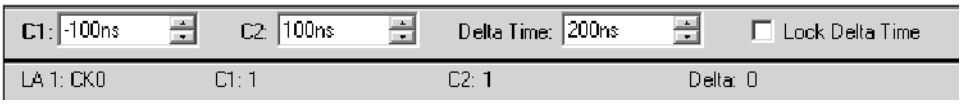
Point to the area of interest on the screen, click the left mouse button, and drag the cursor to create a zoom box. After you create the box, right click the mouse to display a menu containing several options. Instead of right-clicking the mouse, you can also click on the magnifying glass near the upper right corner of the window after you draw the zoom box.

- Click Zoom from the menu to zoom on the area of interest.
- Click Copy Bitmap to copy the area inside the zoom box to the clipboard. You can then use tools such as MS-Paint to edit the bitmap for use in different applications.

- Click Move Cursors to move the cursors to both sides of the zoom box. You can then easily make cursor measurements from the new cursor positions.
- Click Suppress to suppress or hide the waveforms under the boundaries of the zoom box. To unsuppress the waveforms, right-click the mouse, click Define Suppression, and click Show All acquired samples in the dialog box. Click OK to close the dialog box and the suppressed samples are restored.

Taking Cursor Measurements

Use the cursors to take time and voltage measurements. You take time and voltage measurements in the Waveform window, as shown below.



To take a time measurement, perform the following steps (Magnitude on an LA module waveform is expressed as a 1 or a 0.):

1. In the Waveform window, select a waveform.
2. Move Cursor 1 to the location on the waveform that you want to measure.
3. Read the time from the C1 readout on the measurement bar.
4. Move Cursor 2 to another location on the waveform that you want to measure.
5. Read the time from the C2 readout on the measurement bar.
6. Read the time difference between the two waveform locations from the Delta Time readout on the measurement bar.
7. Optionally select the Lock Delta Time check box to lock the current time difference between cursors.

The Delta readout is not an absolute delta because the delta can be either positive or negative. For example if you place Cursor 2 before Cursor 1, the result will be a negative value. Cursor time is relative to the active system trigger.

Automatic Waveform Measurements

Use the Measurement Setup dialog box to select the measurements that will be performed on the DSO waveform(s) and to select the new measurement setup parameters. To display the Measurement Setup dialog box, right-click the DSO waveform label, and select Add / Delete DSO Measurement from the context menu.

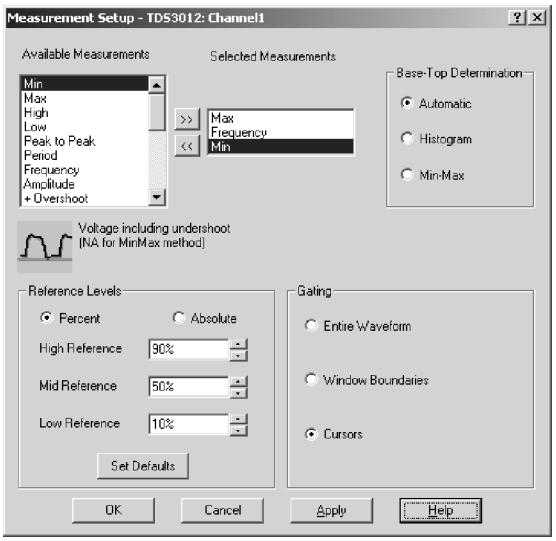


Figure 3-67: Measurement Setup dialog box

- Available Measurements lists all of the available measurements that are supported on the DSO waveform. When you select an available measurement, a graphic and a brief description of the measurement are displayed beneath the Available Measurements list box. Table 3–15 describes the available measurements.
- Selected Measurements displays up to three DSO waveform measurements that you select. You can modify the list of selected measurements using the Add >> and Remove << buttons. If more measurements are desired, you can duplicate a waveform and select three additional measurements.
- Base-Top Determination allows you to select the method for determining the base and top for a selected measurement: automatic, histogram, or min-max. The default setting is “automatic,” which lets the logic analyzer choose between histogram and min-max for the waveform under test. Changes made to the base-top determination apply only to the selected measurements.

- The Reference Levels group box enables you to select either absolute or percentage-based reference levels for the measured waveform. After selecting the type of waveform reference level, you can either set the High-, Mid-, and Low-Reference levels or elect to use the defaults. Changes made to the reference levels apply to all measurements. Table 3–16 lists the available reference levels and provides a description of each.
- The Gating group box enables you to select the area of the waveform over which the measurement is calculated. You can select the entire waveform, window boundaries, or cursor positions. The gating settings apply to all measurements.

Table 3-15: Automatic waveform measurements

Measurement	Description
High	The value used as 100% whenever high reference, mid reference, or low reference values are needed, such as in fall time or rise time measurements. This value can be calculated using either the min/max or histogram method.
Low	The value used as 0% whenever high reference, mid reference, or low reference values are needed, such as in fall time or rise time measurements. This value can be calculated using either the min/max or histogram method.
Amplitude	This voltage measurement is the high value less the low value measured over the entire waveform or gated region.
Maximum	This voltage measurement is the maximum amplitude. It is typically the most positive peak voltage and is measured over the entire waveform or gated region.
Minimum	This voltage measurement is the minimum amplitude. It is typically the most negative peak voltage and is measured over the entire waveform or gated region.
Peak to Peak	This voltage measurement is the absolute difference between the maximum and minimum amplitude in the entire waveform or gated region.
Positive Overshoot	This voltage measurement is measured over the entire waveform or gated region and is expressed as: Positive Overshoot = (Maximum – High) ÷ Amplitude x 100%
Negative Overshoot	This voltage measurement is measured over the entire waveform or gated region and is expressed as: Negative Overshoot = (Low – Minimum) ÷ Amplitude x 100%
Mean	This voltage measurement is the arithmetic mean over the entire waveform or gated region.
RMS	This voltage measurement is the true Root Mean Square voltage over the entire waveform or gated region.
Rise Time	This timing measurement is the time required for the leading edge of the first pulse in the waveform or gated region to rise from the low reference value (default = 10%) to the high reference value (default = 90%) of the final value.

Table 3-15: Automatic waveform measurements (Cont.)

Measurement	Description
Fall Time	This timing measurement is the time required for the falling edge of the first pulse in the waveform or gated region to fall from the high reference value (default = 90%) to the low reference value (default = 10%) of the final value.
Positive Width	This timing measurement is the distance (time) between the mid reference (default = 50%) amplitude points of a positive pulse. The measurement is made on the first pulse in the waveform or gated region.
Negative Width Measurement	This timing measurement is the distance (time) between the mid reference (default 50%) amplitude points of a negative pulse. The measurement is made on the first pulse in the waveform or gated region.
Period	The time required to complete the first cycle in a waveform or gated region. Period is the reciprocal of frequency and is measured in seconds.
Frequency	This timing measurement is a measure of the first cycle in a waveform or gated region. Frequency is the reciprocal of the period; it is measured in Hertz (Hz) where one Hz is one cycle per second.
Positive Duty Cycle	This timing measurement is the ratio of the positive pulse width to the signal period expressed as a percentage. The duty cycle is measured on the first cycle in the waveform or gated region. Positive Duty Cycle = (Positive Width) ÷ Period x 100%.
Negative Duty Cycle	This timing measurement is the ratio of the negative pulse width to the signal period expressed as a percentage. The duty cycle is measured on the first cycle in the waveform or gated region. Negative Duty Cycle = (Negative Width) ÷ Period x 100%.
Area	Area is a voltage-over-time measurement. The measurement is the area over the entire waveform or gated region expressed in volt-seconds. The area above the common reference point is positive and the area below the common reference point is negative.
Cycle Area	The voltage over time measurement. The measurement is the area over the first cycle in the waveform or the first cycle in the gated region expressed in volt-seconds. The area above the common reference point is positive and the area below the common reference point is negative.
Cycle Mean	This voltage measurement is the arithmetic mean over the first cycle in the waveform or the first cycle in the gated region.
Cycle RMS	This voltage measurement is the true Root Mean Square voltage over the first cycle in the waveform or the first cycle in the gated region.
Burst Width	This timing measurement is the duration of a burst and is measured over the entire waveform or gated region.

Table 3-16: Waveform Reference Levels

Reference Level	Description
High Reference	This defines the high reference level of a waveform; the default level is 90%. This reference level is used with the Low Reference level in the calculation of rise and fall times.
Mid Reference	This defines the middle reference level of a waveform; the default value is 50%. This reference value is primarily used for making measurements between edges such as pulse widths.
Low Reference	This defines the low reference level of a waveform; the default level is 10%. This reference level is used with the High Reference level in the calculation of rise and fall times.

The waveform shown in Figure 3-68, illustrates automatic waveform measurements that display within the Waveform window.

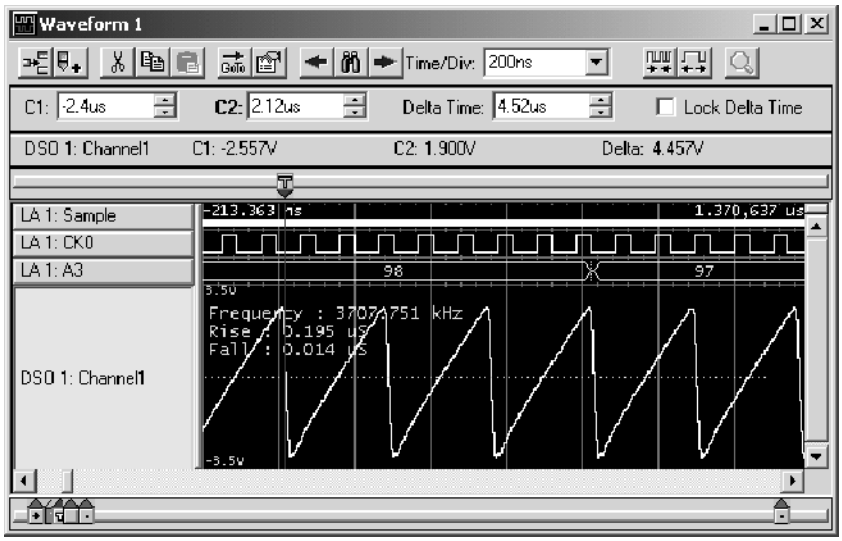


Figure 3-68: Sawtooth waveform with automatic measurements

Jumping to Specific Data Locations

You can use the Go To dialog box to jump to a new position by selecting any current mark or waveform. To open the Go To dialog box, open a Waveform window and click the Go To tool bar button, as shown in Figure 3-69.

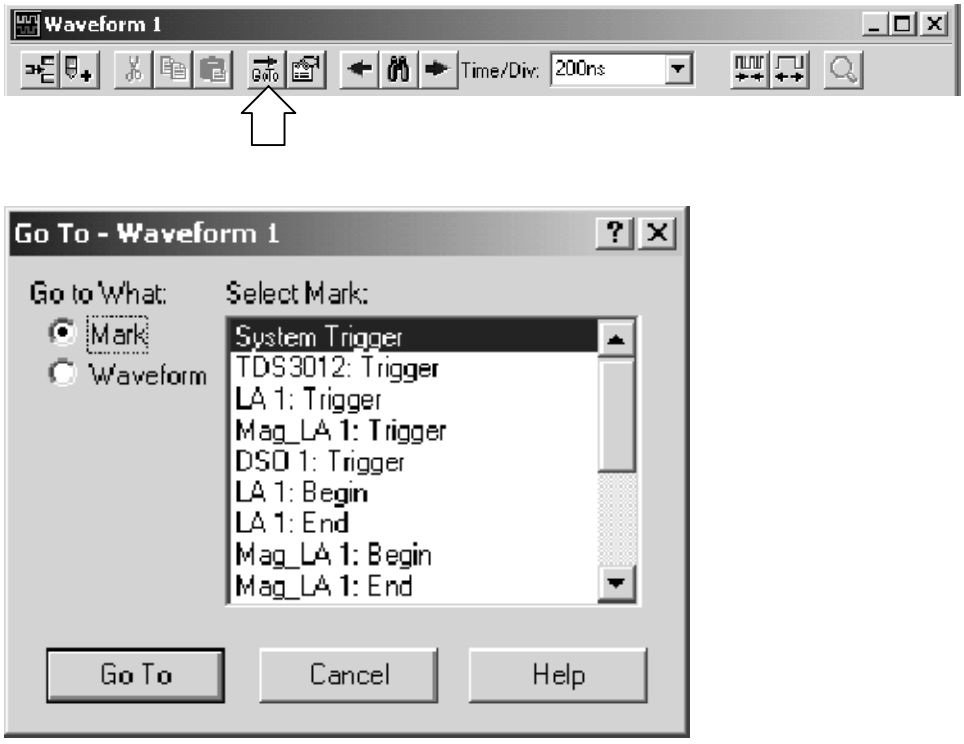


Figure 3-69: Using the Go To dialog box to jump to the system trigger

You can also use the Overview Mark bar to jump to another location. If you do not click on a mark, clicking in the Overview Mark bar scrolls to that location.

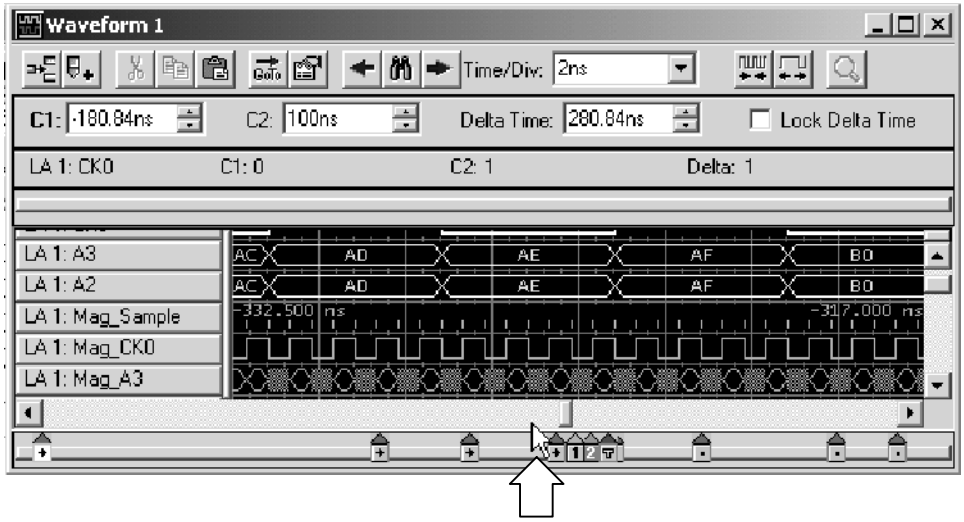
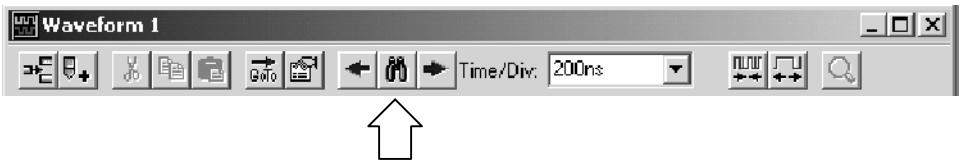


Figure 3-70: Using the Overview Mark bar to jump to a data location

Searching Data

Use the Define Search dialog box (see Figure 3–71) to search for specific data within the current Waveform window. Searches are specific to the selected data source and begin from the active cursor.

Click the search icon to open the dialog box and fill out the search conditions. Cursor 1 marks the first occurrence of the item you searched for.



You can search any data source available to the current data window, but you can only search one data source at a time. For additional searches of the same event, click the Search Forward and Search Back arrow buttons in the tool bar (on either side of the search icon).

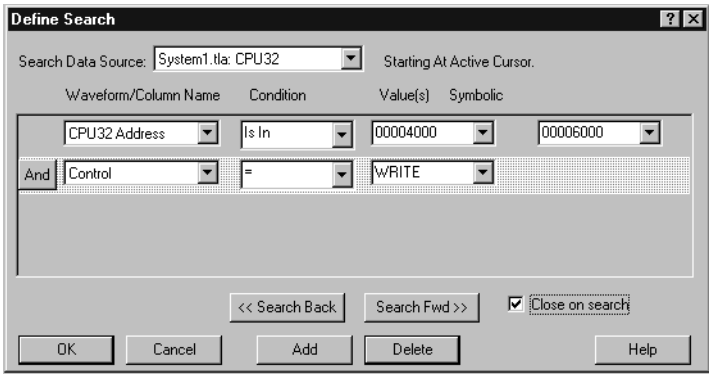


Figure 3-71: Defining search criteria

Hidden data or suppressed samples cannot be found by the search function. For example, if you turn off a waveform in the Waveform properties tab by deselecting Show Waveform, the search function cannot search for that waveform data.

Figure 3–72 shows a waveform window with suppressed samples (indicated by dashes). If you try to search for suppressed data, the instrument will skip over the suppressed area and search for visible data. If the suppressed data is still in memory, you can unsuppress the data (right-click the mouse, click Define Suppression, click Show All acquired samples in the dialog box, and then click OK to close the dialog box). You can then search for the data.

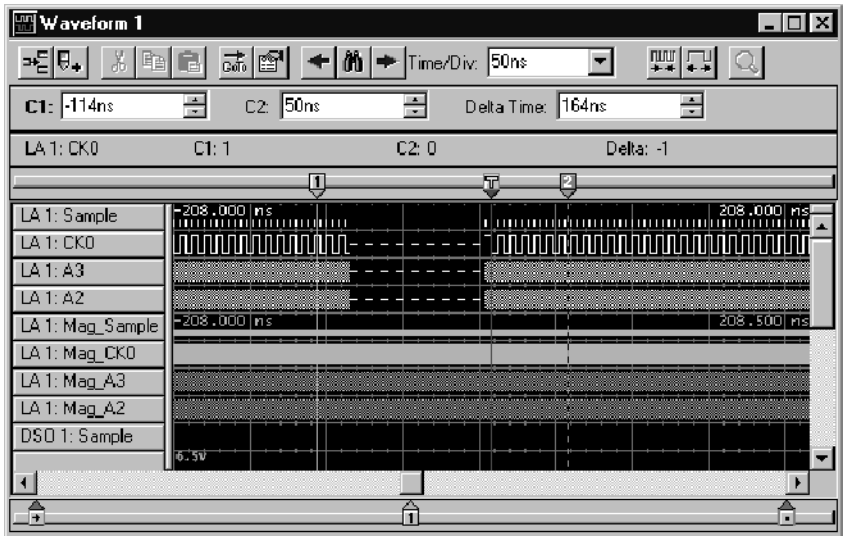


Figure 3-72: Suppressed samples in a Waveform window

Be aware, however, that you cannot unsuppress samples from a saved setup where you selected Save only Unsuppressed Data in the Save As dialog box.

Locking Windows

Locking windows provides an easy method to compare data from two different windows. Use the Lock Windows dialog box, shown in Figure 3–73, to select how windows are locked together.

To open the Lock Windows dialog box, go the System window and click the button for the data window you want to open. Then from the View menu, click Lock Windows.

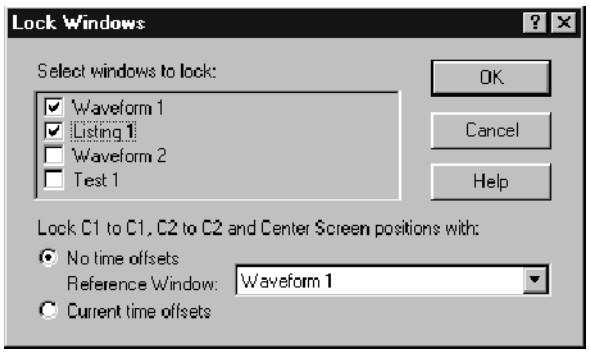


Figure 3-73: Lock Windows dialog box

MagniVu Data

The LA modules have MagniVu data acquisition as a standard feature. MagniVu data acquisition for TLA7Lx/Mx/Nx/Px/Qx modules offers 500 picosecond, high-speed timing simultaneous with 100 MHz or 200 MHz state on all channels through the same probe. MagniVu memory depth is set to a fixed 2K.

MagniVu data acquisition for TLA7Axx modules offers 125 picosecond high-speed timing simultaneous with 120 MHz, 235 MHz or 450 MHz state on all channels through the same probe. The record length for MagniVu data is 2015 samples. MagniVu memory depth is set to a fixed 16K.

MagniVu data is centered on the LA module trigger. Figure 3-74 shows an example of MagniVu data. You can view MagniVu data in both Listing and Waveform windows.

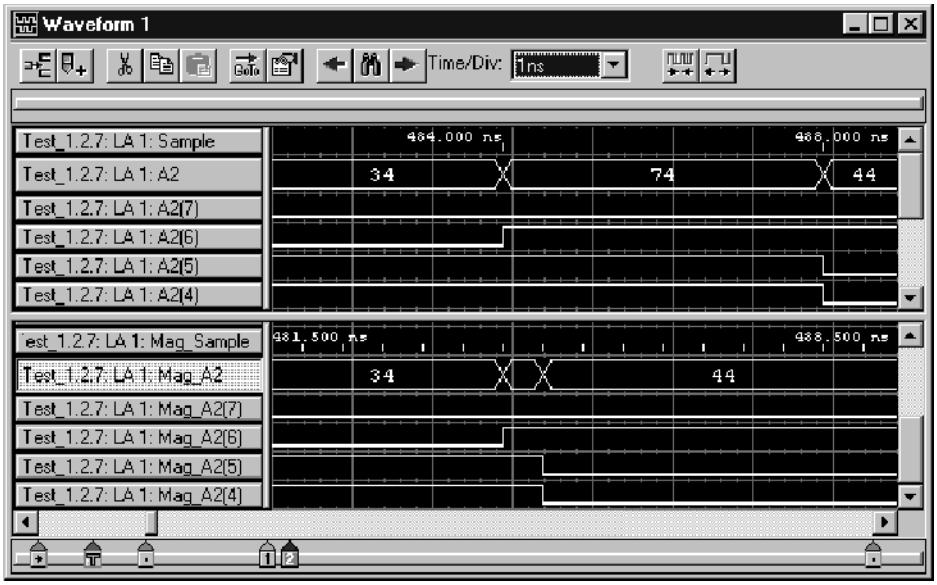


Figure 3-74: MagniVu data

In Figure 3-74, the top waveforms were acquired at the fastest normal sample rate. The MagniVu waveforms, in the lower part of the display, were acquired through the same probe channels at the same time as the top waveforms.

Take a close look at the difference in the acquired data. First view the regular data acquisition, which was sampled at 4 ns. The regular acquisition captured the address bus as it made the transition from 34 to 44. The data shows an invalid address of 74, and indicates that the invalid address lasts for the entire 4 ns sample period. At the next sample, the address is shown correctly as 44.

Now view the MagniVu data acquisition, which was sampled at 500 ps. The MagniVu data shows the same address bus transition from 34 to the invalid address of 74, before settling to the correct address of 44. Note, however, that the indicated settling time is different. The MagniVu data shows that the address bus took approximately 500 ps to complete the transition, and shows the address bus as 44 approximately 3.5 ns earlier than the regular acquisition data.

MagniVu Storage Rate

With TLA7Axx modules you can adjust the MagniVu storage rate downward from the sample rate allowing for a lower resolution of data samples from a longer time period.

The MagniVu storage rate cannot be set slower than the effective main memory rate, according to 1X, 2X, or 4X modes. The available rates are:

- 8 GHz <-> 125 ps
- 4 GHz <-> 250 ps
- 2 GHz <-> 500 ps
- 1 GHz <-> 1 ns

The MagniVu storage rates are limited by PowerFlex as well as by the fastest storage rate of the main memory under 1X, 2X, and 4X modes. The slowest MagniVu storage rate is half of the fastest storage rate of the main memory.

Table 3-17: MagniVu storage rates

1X MagniVu Storage Selections	2X MagniVu Storage Selections	4X MagniVu Storage Selections
125 ps 250 ps 500 ps 1 ns	125 ps 250 ps 500 ps	125 ps 250 ps

***NOTE**. MagniVu storage rate adjustments do not affect Setup and Hold violation or Glitch violation.*

MagniVu Trigger Position

The MagniVu trigger position, available with TLA7Axx modules, selects the amount of pretrigger MagniVu data to store and determines the position of the trigger in the data record. You can control the MagniVu trigger position independently of main trigger position by a set of controls in the advanced toolbar.

Once triggered, a module continues to acquire MagniVu data until it fills a specified amount of memory. MagniVu memory depth is set to a fixed 16K. The Trigger Position field determines the proportion of data that is stored before and after the trigger. For example, if the Trigger Position is set to 15% and the module triggers, then the module continues to acquire data until the remaining 85% of memory is filled.

The MagniVu trigger position controls mirror the corresponding controls for main memory trigger position. They consist of a slider control, an edit box, and a spin control positioned beneath the main memory trigger controls. They behave like the main memory counterparts, except that the MagniVu trigger position is constrained by the MagniVu storage rate as shown in Table 3–18.

Table 3-18: MagniVu storage rate

Storage rate	Resulting trigger position constraint
125 ps	0% to 58% in 1% increments
250 ps	0% to 79% in 1% increments
500 ps	0% to 89% in 1% increments
1 ns	0% to 94% in 1% increments

Changing Analog Multiplex Data

Using the Route to DSO dialog box, available from the Waveform window, you can change the analog multiplex data that is routed from a logic analyzer channel to one of the oscilloscope channels. You can additionally change the analog multiplex data that is routed from a logic analyzer channel to the currently selected oscilloscope channel, using the Route from LA dialog box, which is also available from the Waveform window. The channel waveform you select in the Waveform window determines the availability of the routing dialog box.

Routing Data to the DSO

The Route to DSO dialog box lists oscilloscope channels that have inter-probe connections defined to the logic analyzer. If no inter-probe connections are defined, the list is empty. Select an oscilloscope channel and click OK to feed the logic analyzer channel to the inter-probe connection attached to the oscilloscope channel.

The check box named Add new waveform to view is not selected by default because the waveform view typically already contains waveforms for the oscilloscope of interest. Selecting this check box and clicking OK will add a waveform of the selected oscilloscope destination to the view.

Click the System Inter-probing button to change the destination list contents by adding or deleting the connections for the logic analyzer.

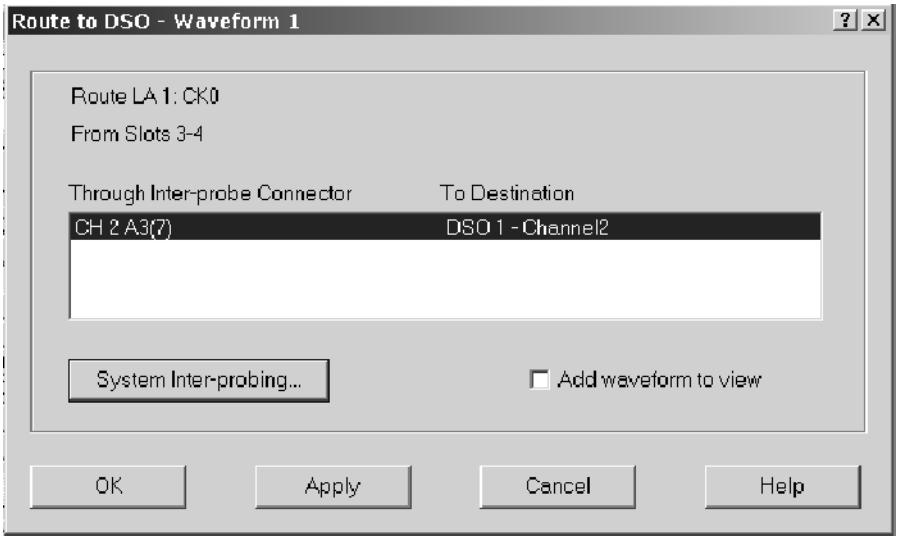


Figure 3-75: Route to DSO dialog box

To display the Route to DSO dialog box from the Waveform window, select Route to DSO from the context menu associated with a selected LA channel waveform. The Route to DSO context menu item is only enabled if the selected waveform is a TLA7Axx channel.

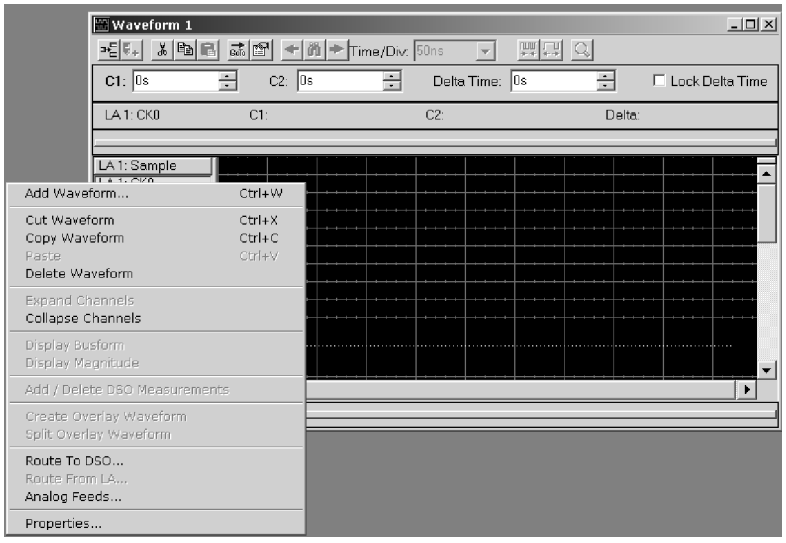


Figure 3-76: Changing analog multiplex data from the Waveform window

Routing data from the logic analyzer

The Route from LA dialog box displays the currently defined inter-probe connection and its feed for the oscilloscope channel. This item cannot be selected

and is displayed for information purposes only. If no inter-probe connection is defined for the oscilloscope channel, the field is empty.

Click the System Inter-probing button to change the contents of the scroll list by adding or changing the connection to the logic analyzer.

Click the Select Channel button to select a new logic analyzer channel to feed the inter-probe connection to the oscilloscope channel. This button is available when the inter-probe connection is defined.

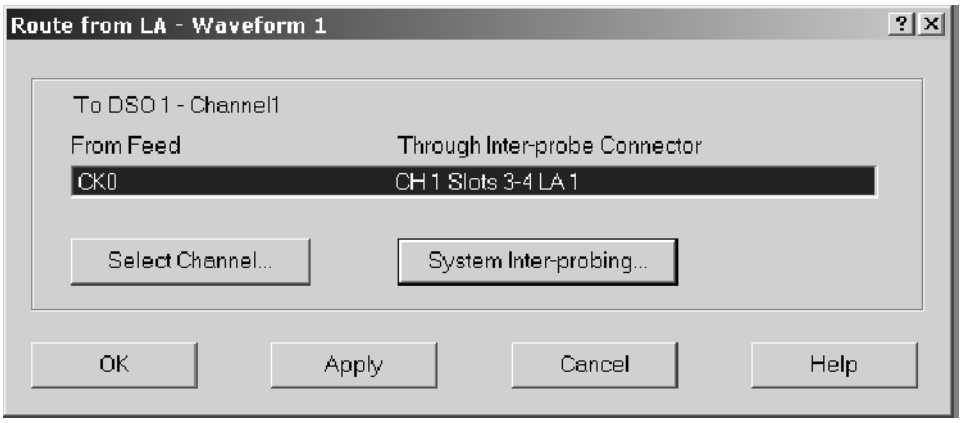


Figure 3-77: Route from LA dialog box

To display the Route from LA dialog box from the Waveform window, select Route to LA from the context menu associated with a selected oscilloscope channel waveform (see Figure 3-76 on page 3-109).

Comparing Waveform Data

When comparing data against reference data, you can highlight data that is equal to or not equal to the reference data.

NOTE. *Before you can display compare data, you must define the compare parameters in the Define Compare Dialog box in the LA Setup window. Refer to* Data Compare *beginning on page 3-5 for information on setting up the compare parameters.*

The following steps describe how to display compare data in the Waveform window.

1. Open a Waveform window and click the Properties tool bar button, as shown.

2. Click the Waveform Window tab.
3. From the Show Compare group box, select one of the colors to use when data does not equal the reference data (Acq!=Ref).

   If you want to highlight data that does equal the reference data, select Acq=Ref and the appropriate color (see Figure 3–78).
4. Click OK.

The data differences or equalities will be highlighted in the Waveform window in colors you specified.

NOTE. *For more information on comparing data, refer to* Guidelines for Memory Compare *on page 3–7.*

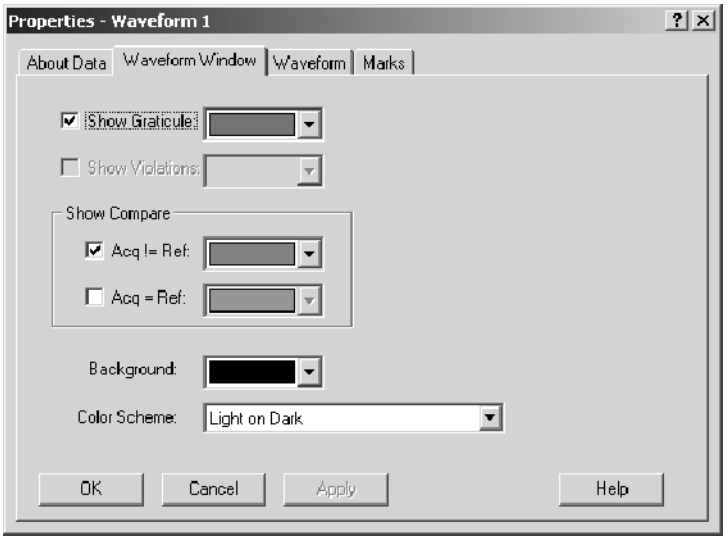


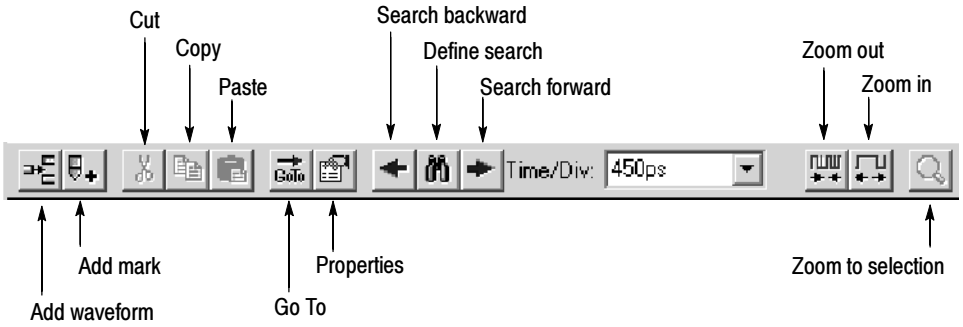
Figure 3- 78: Selecting compare data colors in the Waveform Window property page

Adjusting the Waveform Window

There are a number of actions you can perform in the Waveform window to get the exact view of the data that you want.

Waveform Window Tool bar

The tool bar has shortcut buttons for common operations, as shown in the following illustration:



Moving Waveforms

Select the waveform labels and drag them to their new location.

Adding a New Waveform or a Data Source

Click the tool bar Add Waveform button to open the Add Waveform dialog box. Then select the data source and its associated group or channel to add it to the display.

To select a group, first click By Group. (See Figure 3–79.) Then, from the list, select a group name indicated by the + symbol. Default groups are displayed as busforms. (You can also choose to display a group as a magnitude waveform. Double-click the waveform label. From the waveform properties page, click Options and select Magnitude.)

To select individual channels, first click By Probe. Then, from the list, select the channel(s). If you have named individual channels in the LA Setup window, you can click By Name to list just those channels.

If the data source you want is not listed, click Add Data Source and find and select the source. (The data source can be any logic analyzer data from a saved module file.) See Figure 3–79.

New waveforms are added after the selected waveforms or after all waveforms if none are selected.

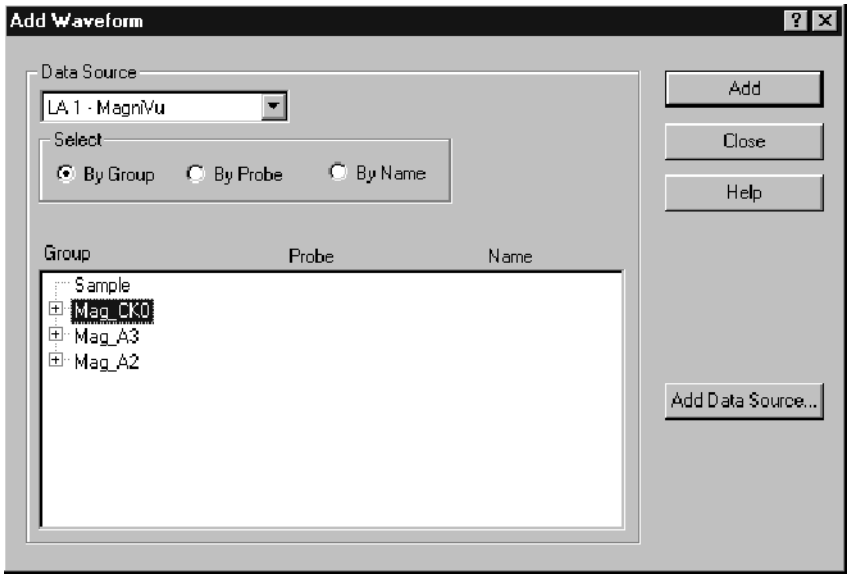


Figure 3-79: Add Waveform dialog box

Deleting Waveforms

Select the waveform labels, and then click the Cut button on the tool bar.

Changing Waveform Label Width

To change the width of a waveform label, select and drag the waveform label border.

Changing Waveform Height

To change the height of a waveform, double-click the waveform label to open the Waveform tab. Enter a new value or use the spinbox controls to change the value in the Height box.

In addition to adjusting the height using the Waveform tab, you can select the waveform and adjust the waveform from the front-panel Size control on the portable mainframe.

Changing the Displayed Time/Div

Change the displayed time per division using the Time/Div tool bar control. You can also use the Zoom In and Zoom Out tool bar buttons.

Cut, Copy, and Paste

You can cut, copy, and paste waveforms and marks.

Viewing Glitches

Both glitches and setup and hold violations are indicated in the display by highlighted text of the complete sample for all radixes except binary, octal, and hexidecimal. In those radixes, only the violation bits are highlighted. Turn the glitch or setup and hold display on or off from the Waveform window tab available from the Waveform Properties dialog box.

***NOTE**. To view glitches in a data window, you must enable Glitch storage in the LA Setup window before acquiring data. To view setup and hold violations, you must enable Setup/Hold storage in the Acquire box of the LA Setup window before acquiring data.*

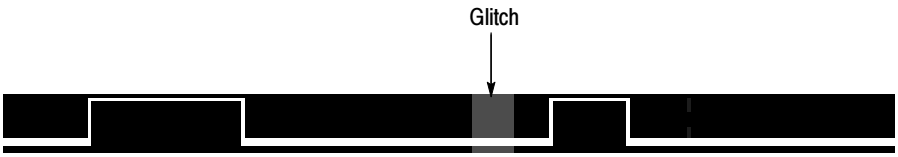


Figure 3- 80: Waveform with a glitch

Naming Waveforms

Rename a waveform by returning to the Setup window and changing the channel or channel group name.

Splitting the Data Area

You can split the data area to compare waveforms that are far away from each other within the display. Drag the split box from the top end of the vertical scroll bar.

Customizing the Waveform Window Data

Use properties to customize data windows. Properties control aspects of the display such as size, color, and in some cases, enabling or disabling whether an element is shown. Click the Properties tool bar button in the Waveform window to display the data window properties. Figure 3-81 shows the Waveform tab, which is available from the Waveform Properties dialog box.

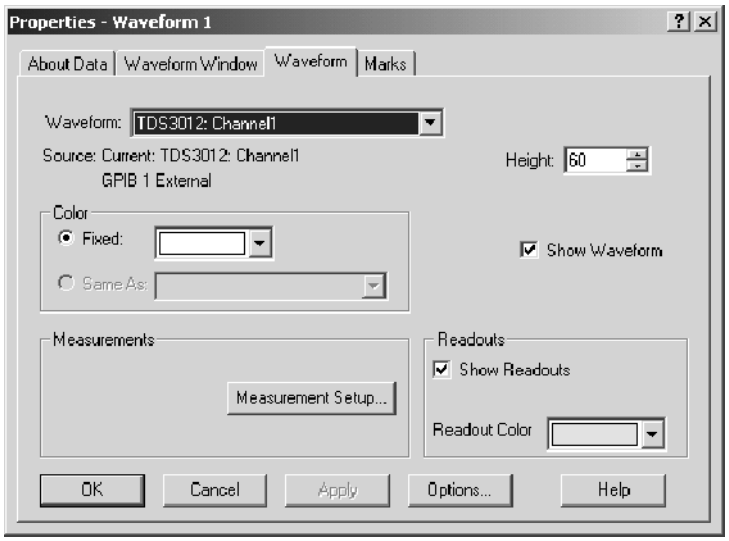


Figure 3-81: Waveform tab of the Waveform Properties dialog box

Exporting Waveform Data

You cannot export waveform data directly. However, you can add DSO waveform information as a column in a Listing window and then export the data as a listing file.

Refer to *Exporting Listing Data* on page 3-130 for more information on exporting data.

Waveform Window Shortcut Keys

You can use the general-purpose shortcut keys listed in Table 3–19 to move data and cursors in the Waveform window. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- Arrow keys with the Control (CTRL) key move the active cursor.
- The Shift key increases movement by a factor of 10.

Table 3-19: Waveform window shortcut keys

Desired action	Key combination
Go to next trigger	CTRL + T
Display Go To dialog box	CTRL + G
Move Cursor 1 to the center of the window	CTRL + 1
Move Cursor 2 to the center of the window	CTRL + 2
Zoom in	CTRL + I
Zoom out	CTRL + U
Add a mark	CTRL + K
Add a waveform	CTRL + W
Scroll data left 50 pixels	Shift + Left arrow
Scroll data right 50 pixels	Shift + Right arrow
Move active cursor left five pixels	CTRL + Left arrow
Move active cursor right five pixels	CTRL + Right arrow
Move active cursor left 50 pixels	CTRL + Shift + Left arrow
Move active cursor right 50 pixels	CTRL + Shift + Right arrow

Overlay Waveforms

Overlay waveforms provide you with the ability to visually compare two or more waveforms by dragging one waveform over the other. The overlay waveform can contain LA single-channel, DSO, external, and sample clock waveforms.

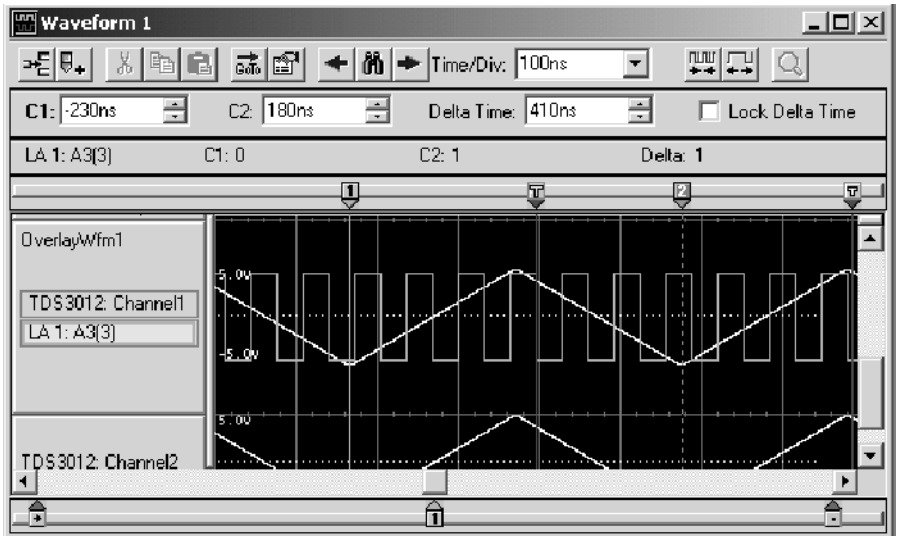


Figure 3-82: Example of an overlay waveform

Overlay Waveform Properties

The waveform properties tab displays overlay waveform properties when you double-click the label of an overlay waveform group in the Waveform properties tab.

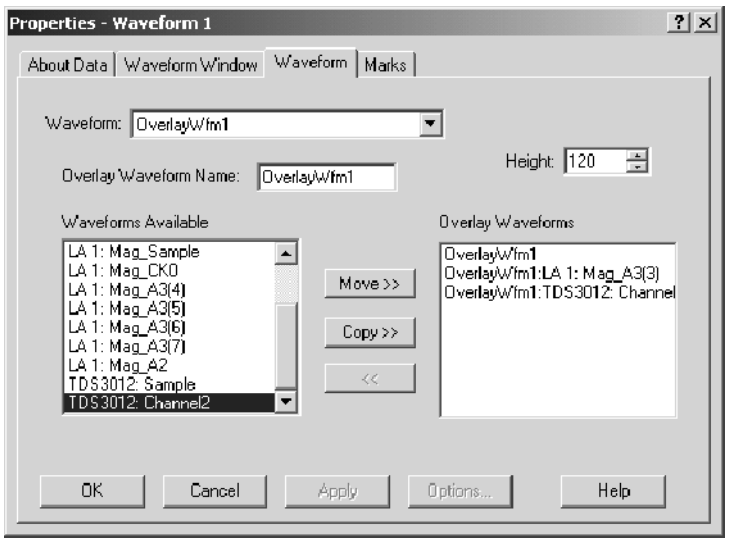


Figure 3-83: Waveform properties tab

The following properties are associated with overlay waveforms:

- **Waveform** lists the label that displays in the Waveform window. You can select a different waveform from the list. The list contains the names of all waveforms in the active window. The initial waveform is the selected waveform (or the first waveform if no waveform is selected). The list box is empty if multiple waveforms are selected.
- **Overlay Waveform Name** permits you to rename overlay waveforms.
- **Height** controls the height of the waveform. Height can range from 10 to 500 pixels. The default height of an LA waveform is 18 pixels; the default height of a DSO waveform or external oscilloscope waveform is 60 pixels.
- **Waveforms Available** lists all of the individual waveforms and preexisting overlay waveforms. You can move and copy waveforms in this list to the Overlay Waveforms list using the Move>> and Copy>> buttons, respectively. You can also remove waveforms from the Overlay Waveforms list and return them to the Waveforms Available list using the << button.
- **Overlay Waveforms** lists the waveforms currently in the selected overlay waveform group. You can move and copy waveforms from the Waveforms Available list to this list using the Move>> and Copy>> buttons, respectively. You can also remove waveforms from the Waveforms In Group list and return them to the Waveforms Available list using the << button.

To change waveform properties from the System window, click a Waveform data window icon, double-click the label of a waveform, and then click the Waveform tab.

To create an overlay waveform, click a waveform label and then drag it to a second waveform that you want to overlay. As you drag the waveform label, a drop marker displays at the left edge of the waveform label. Use this marker to determine which waveform label you will be selecting to form the overlay. When the Add Overlay Waveform Name dialog box appears, enter a name for the waveform or use the default name.

For more information about creating overlay waveforms, or removing a waveform from an overlay waveform, refer to the online help.

Listing Window

Use the LA Listing window to view and evaluate acquisition data. Data is presented as tabular text in columns that represent channel groups. Other columns are sample numbers and time stamp values. See Figure 3–84.

This window displays the amount of data you specified in Setup and Trigger windows. Each row in the table consists of data sampled on one acquisition cycle, and is assigned a sample number. Sample numbers are relative to the beginning of memory.

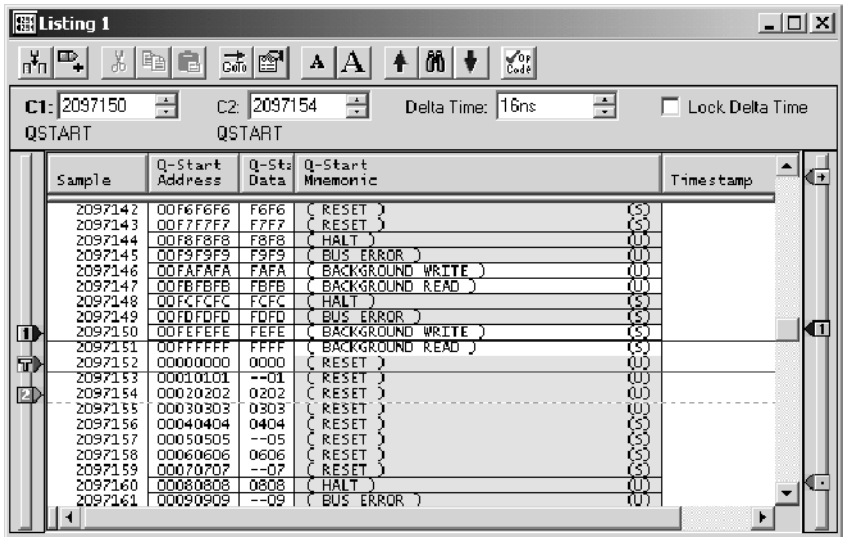


Figure 3-84: Listing window

Reading the Listing Window Indicators

Data marks, cursors, and other indicators help you navigate and identify the data. Figure 3–85 and Table 3–20 identify and describe data window marks.

To move cursors or marks, drag the cursor and mark handles. Trigger marks and Begin/End data marks cannot be moved.

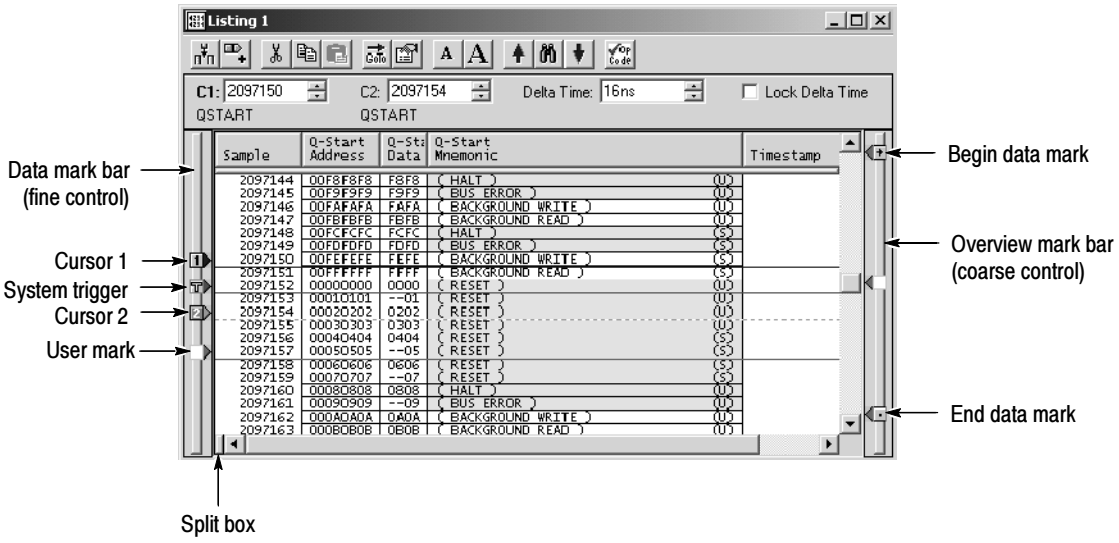


Figure 3-85: Listing window cursors and marks

Table 3-20: Listing window cursor and mark summary

Mark	Name	Description
	System trigger	The system trigger is the reference point for the acquisition. Timing and location information is relative to the system trigger. Trigger marks cannot be moved. Under some conditions the system trigger associated with a module's data might not be displayed in the data window. If the system trigger was caused by another module, whose data is not included in the current display, then the system trigger is not shown. Nevertheless, all time measurements still relate to that system trigger, even if it is not shown. The system trigger associated with the current data is called the active system trigger. The system trigger associated with saved data is called the reference system trigger. The active system trigger is indicated by a yellow T; the reference system trigger is indicated by a gray T.
	Module trigger	The point at which the module triggered. Trigger marks cannot be moved.
	Begin data / end data	The start and end of a module's data record. These data marks cannot be moved.
1 2	Cursors 1 and 2	Moveable marks used for visual reference and for data measurements.
Checkbox	Lock Delta Time	Click this checkbox to lock the delta time value. When you lock delta time, the channel marks move across the data simultaneously, maintaining a fixed delta time.
	User mark	User-created marks. Use marks to make specific data more easy to identify and find.

Taking Cursor Measurements

Use the cursors to take time measurements. Take time measurements in the Listing window, as shown below.

1. In the Listing window, move Cursor 1 to the location that you want to measure.
2. Read the time from the C1 readout on the measurement bar. Cursor time is relative to the active system trigger.
3. Move Cursor 2 to another location that you want to measure.
4. Read the time from the C2 readout on the measurement bar.
5. Read the time difference between the two locations from the Delta readout on the measurement bar.
6. Click the Lock Delta Time checkbox to maintain the specified delta time, moving the C1 and C2 marks simultaneously across the data.

Jumping to Specific Data Locations

You can use the Go To dialog box to jump to a new position by selecting any current mark or waveform. To open the Go To dialog box, open a data window and click the Go To tool bar button as shown in Figure 3-86.

You can also use the Overview Mark bar (see Figure 3-87) to jump to another location. If you do not click on a mark, clicking in the Overview Mark bar scrolls to that location.

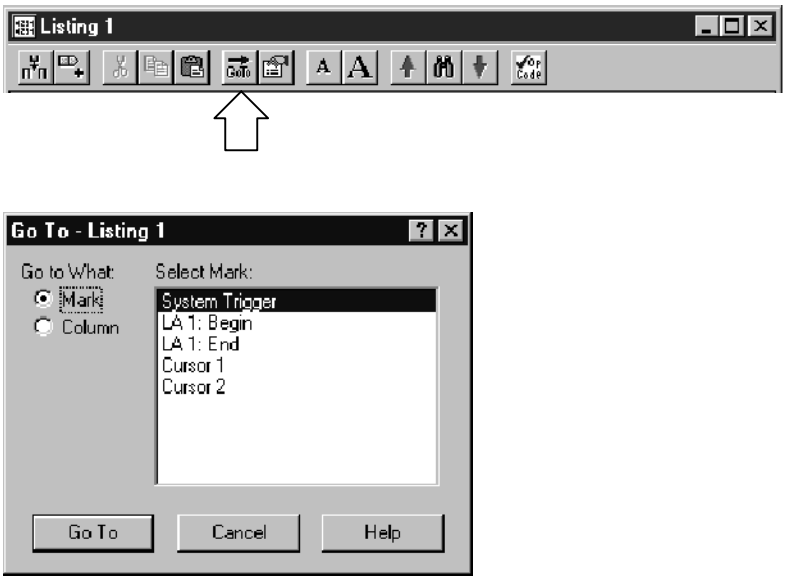


Figure 3-86: Using the Go To dialog box to jump to the system trigger

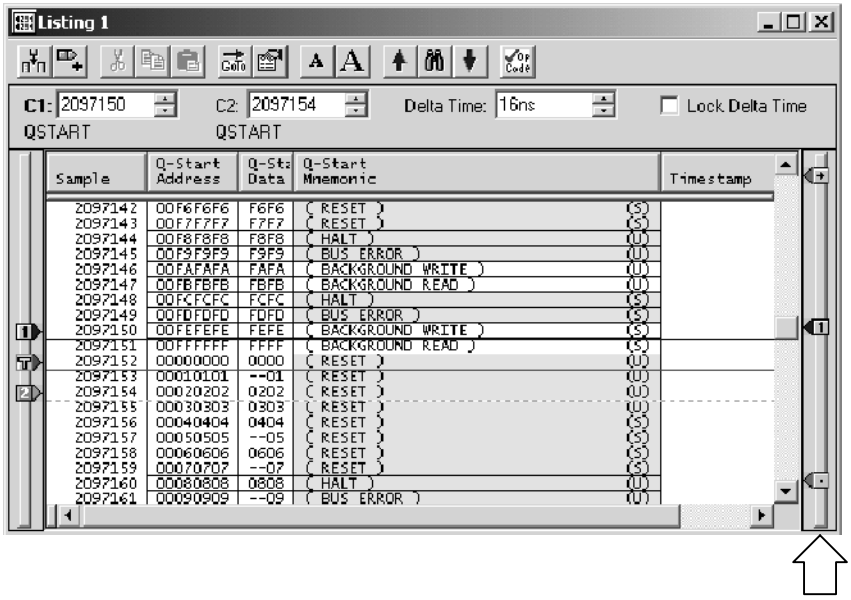
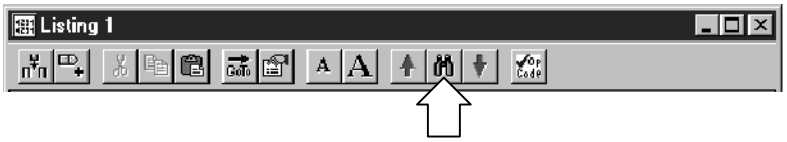


Figure 3-87: Using the Overview Mark bar to jump to a data location

Searching Data

Use the Define Search dialog box (see Figure 3-88) to search for specific data within the current Listing window. Searches are specific to the selected data source and begin from the active cursor.

Click the search icon to open the dialog box and then fill out the search conditions. The active cursor moves to the location of a successful search.



You can search any data source available to the current data window, but you can only search one data source at a time. For additional searches of the same event, click the Search Forward and Search Back arrow buttons in the tool bar.

Hidden data cannot be found by the search function. For example, if you turn off a column display in the Column properties page by deselecting Show Column, you cannot search for data in that column. Similarly, suppressed data cannot be found by the search function; suppressed data in the listing window can be identified by gaps in sequence numbers.

You can unsuppress data and then use the search function as long as the data is in memory. However, you cannot unsuppress data in setups that you save using the "Save only Unsuppressed Data" from the Save As dialog box.

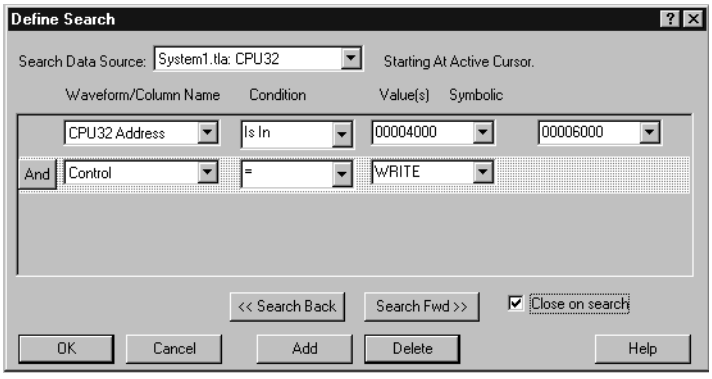


Figure 3-88: Defining search criteria

Locking Windows

Locking windows provides an easy method to compare data from two different windows. Use the Lock Windows dialog box, shown in Figure 3–89, to select how windows are locked together.

To open the Lock Windows dialog box, go the System window and click the button for the data window you want to open. Then from the View menu, click Lock Windows.

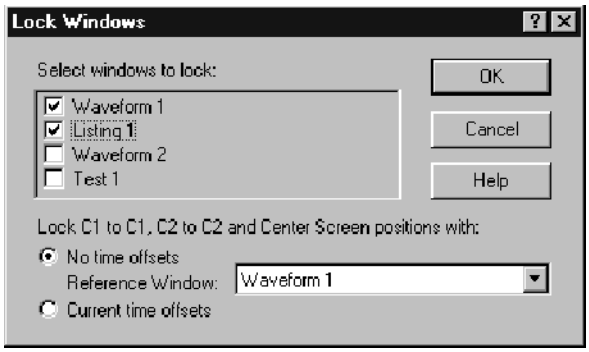


Figure 3- 89: Lock Windows dialog box

MagniVu Data

The LA modules have MagniVu data acquisition as a standard feature. MagniVu data acquisition for TLA7Lx/Mx/Nx/Px/Qx modules offers 500 picosecond, high-speed timing simultaneous with 200 MHz state on all channels through the same probe. MagniVu memory depth is set to a fixed 2K.

MagniVu data acquisition for TLA7Axx modules offers 125 ps, high-speed timing simultaneous with120 MHz, 235 MHz, or 450 MHz state on all channels through the same probe. MagniVu memory depth is set to a fixed 16K.

You can view MagniVu data in both Listing and Waveform windows. For more information on MagniVu data, refer to *MagniVu Data* beginning on page 3–106.

Comparing Listing Data

When comparing data to reference data, you can highlight data that is equal to or not equal to the reference data.

***NOTE**. Before you can display compare data, you must define the compare parameters in the Define Compare dialog box in the LA Setup window. Refer to* Data Compare *beginning on page 3–5 for information on setting up the compare parameters.*

The following steps describe how to display compare data in the Listing window.

1. Open a Listing window and click the Properties tool bar button, as shown.

2. Select the Listing Window tab.
3. Select Show Compare, and select one of the colors to indicate when data does not equal the reference data (Acq!=Ref). See Figure 3–90.
4. If you want to highlight data that does equal the reference data, select Acq=Ref and the appropriate color.

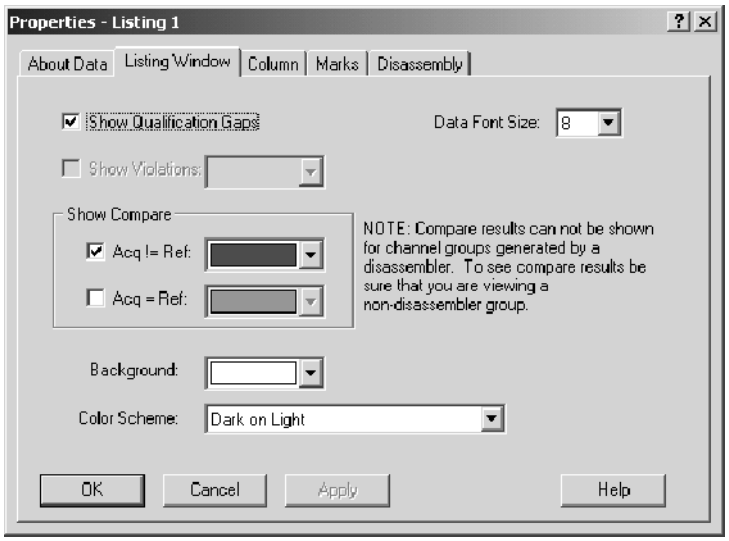


Figure 3-90: Selecting compare data colors in the Listing Window tab

5. Click OK.

The data differences or equalities will be highlighted in colors you specified, similar to Figure 3–91.

NOTE. *For more information on comparing data, refer to* Guidelines for Memoy Compare *on page 3–7.*

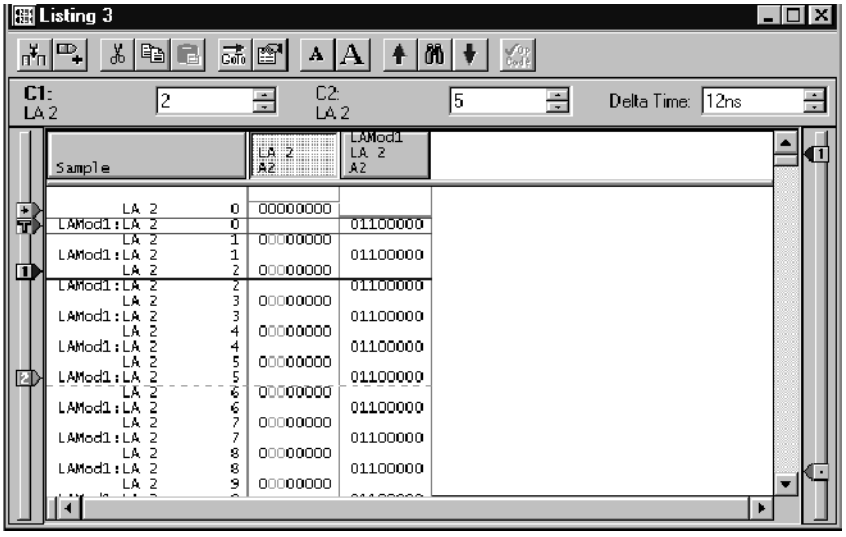


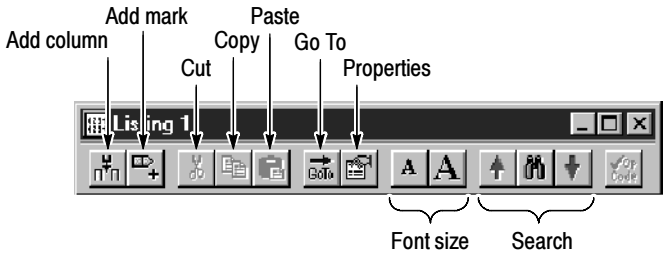
Figure 3-91: Viewing LA compare data in a Listing window

Adjusting the Listing Window

There are a number of actions you can perform in the Listing window to get the exact view of the data that you want.

Listing Window Tool Bar

The tool bar has shortcut buttons for common operations, as shown below.



Changing the Display Font Size

Click the Font Size tool bar buttons. Continue to click the tool bar buttons until the text reaches the desired size. You can also set the font to a specific size using the Listing Window properties.

Moving Columns

Select the column labels, and then drag them to their new location.

Adding a New Column or Data Source

Click the tool bar Add Column button to open the Add Column dialog box. Then select the data source and its associated group or channel to add it to the display. If the data source you want is not listed, click Add Source to find and select the source. The data source can be an installed module or a saved module file. See Figure 3–92.

New columns are added after (to the right of) the selected columns or after all columns if none are selected.

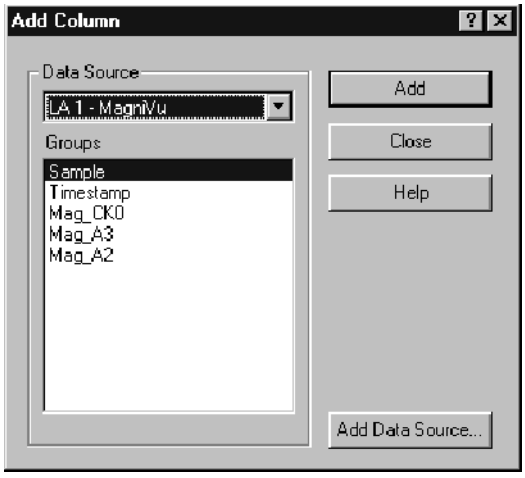


Figure 3- 92: Add Column dialog box

Deleting Columns

Select the column labels, and then click the Cut tool bar button.

Changing Column Width

Double-click the column label to display the Column tab. Enter a new value for the column width. If you have a portable mainframe, you can also change the column width by selecting the column label and using the front panel Scale control to set the width.

Cut, Copy, Paste

You can cut, copy, and paste columns and marks. You can also copy textual data from the listing to the clipboard. From there you can paste it to other areas, such as the Define Search dialog box or the Clause Definition dialog box in the Trigger window.

Changing Radixes

To change a column radix in the Listing window, double-click the column label to open the Column properties tab. Select a new radix. To use the Symbolic radix, select Symbolic from the list, click the Symbol File button, and then browse the file system for a symbol file. See *Symbol Support* beginning on page 2–48 for information about using symbols and symbol table files.

Viewing Qualification Gaps

Qualification gaps indicate that data samples were not stored due to storage qualification or Don't Store trigger actions.

Qualification gaps are indicated with a horizontal gray line above the first data after the gap. Turn qualification gaps on or off from the Listing Window property page.

Viewing Violations

Glitches and setup and hold violations are indicated in the display by highlighted text of the complete sample for all radixes except binary, octal, and hexadecimal. In those radixes, only the violation bits are highlighted. Turn violations on or off from the Listing Window properties tab. To view glitches, you must set clocking to Internal and select Glitches in the Acquire box of the Setup window before making an acquisition. To view setup and hold violations, you must set clocking to External and select Setup/Hold in the Acquire box of the Setup window before making an acquisition.

***NOTE**. To view glitches in a data window, you must enable Glitch storage in the Acquire box of the LA Setup window before acquiring data. To view setup and hold violations, you must enable Setup/Hold storage in the Acquire box of the LA Setup window before acquiring data.*

Naming Columns

Rename a column by returning to the LA Setup window and changing the channel group name.

Changing the Disassembly Format

For microprocessor support packages, you can change the disassembly format used in the Listing window. Use the Disassembly properties tab to select the display format of disassembly groups. You must have a support package loaded for this page to be active.

Splitting the Data Area

You can split the data area to compare columns that are far away from each other within the display. Drag the split box from the left end of the horizontal scroll bar.

Customizing the Listing Window Data Area

Use the Listing Properties dialog box to customize data in the Listing window. The related properties tabs control aspects of the listing display such as size, color, and in some cases, enabling or disabling whether an element is shown. Click the Properties tool bar button to display the Listing Window properties. Then select one of the properties tabs to change the data you are interested in.

Exporting Listing Data

Use the Export Data dialog box to export data from the current listing window to a text file or to a binary file. This is a way to print a copy of a complete or partial listing. Figure 3–93 shows the Export Data dialog box.

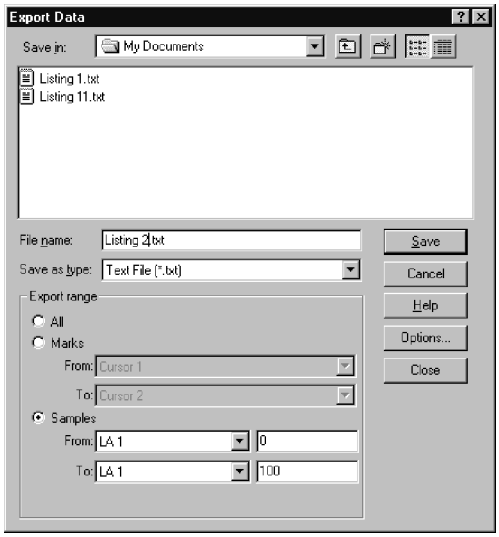


Figure 3- 93: Export Data dialog box

You can export the following listing data:

- All listing data from the acquisition
- Listing and DSO voltage measurement from a Listing window
- A range of listing data between two selected marks
- A range of listing data between two samples

Exporting Data to a Text File

If you want to export data to a text file, click Options to define the format of the data in the Export Data Options dialog box (see Figure 3–94). The data is saved in a text file with the .txt file name extension.

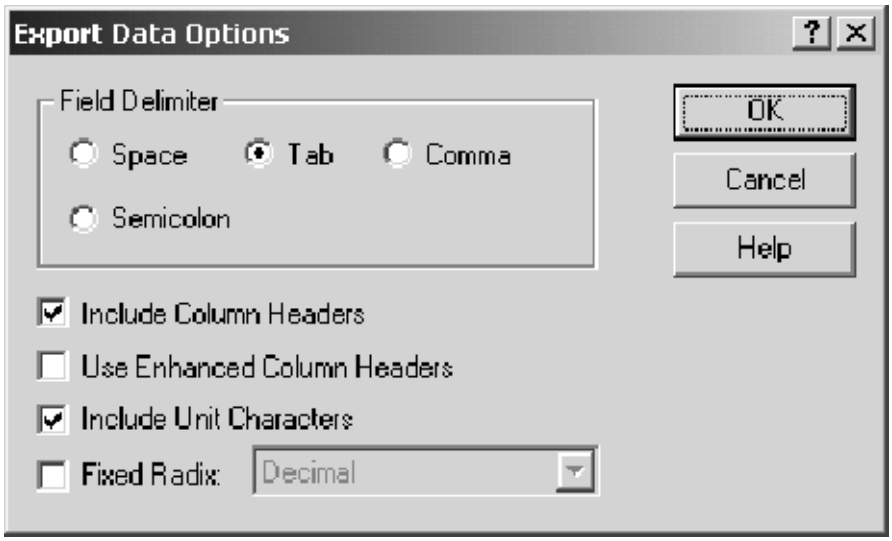


Figure 3-94: Export Data Options dialog box

Use the Export Data Options dialog box to customize the listing data for a text file. You can specify the field delimiter to separate the listing columns. You can also specify whether measurement units will be included with the data. If you export the data without unit characters, the time stamp values are in picoseconds and the DSO values are listed in volts.

To export listing data, follow these steps:

1. In the System window, select a Listing window.
2. From the File menu, click Export Data.
3. In the Export Data dialog box, select the folder to which you want to export data. Otherwise, leave the default of My Documents.
4. Click the Options button to specify any export options for the text data, and then click OK.
5. Enter a name for the exported file.
6. Specify the export range.
7. Click Save.

Exporting Data as a Binary File

You can also export the listing data as a binary file with a .tbf (TLA700 Binary Format) file name extension. This option is only available if the data window is from a single data source. You can export any data that appears in a Listing window, including DSO and MagniVu data. This option is useful when you write applications that require binary data. It is also faster than exporting an ASCII file and the file size is often smaller.

LA Module Binary Export File Format. The LA module binary data is exported as a stream of bytes with the following characteristics:

- The binary data uses big-endian fields (the most significant bit is the left-most bit).
- Each group column field is zero-padded on the most significant end to the nearest byte.
- Sample numbers and mnemonics groups are not exported.
- Time stamp data is seven bytes wide and represents the number of picoseconds since the start of the acquisition.
- The left-most column in the Listing window display corresponds to the first exported field of a sample.
- The first sample in the Listing window appears at the beginning of the exported file.
- MagniVu data follows the same guidelines as regular listing data.

DSO Module Binary Export File Format. The DSO module binary data (when used in a Listing window) is exported as a stream of bytes with the following characteristics:

- The binary data uses little-endian fields (the most significant bit is the right-most bit).
- Each channel field is a 16-bit value.
- Sample numbers, mnemonics groups, and time stamp values are not exported.
- The left-most column in the Listing window display corresponds to the first exported field of a sample.
- The first sample in the Listing window appears at the beginning of the exported file.
- DSO data values are in twos-compliment format.

- The formula used for converting a DSO channel field into a voltage is:

  ((Vertical range in volts / 64512) X channel field) + vertical offset in volts

The contents of the window will be sent to the printer or to the specified file.

Listing Window Shortcut Keys

You can use the general purpose shortcut keys listed in Table 3–21 to move data and cursors in the Listing window. You should also refer to the discussions of short cut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- CTRL + Arrow keys move the active cursor.
- The Shift key increases movement by a factor of 10.

Table 3-21: Listing window shortcut keys

Desired action	Key combination
Go to next trigger	CTRL + T
Display Go To dialog box	CTRL + G
Move Cursor 1 to the center of the window	CTRL + 1
Move Cursor 2 to the center of the window	CTRL + 2
Add a mark	CTRL + K
Add a column	CTRL + L
Scroll data up 10 samples	Shift + Up arrow
Scroll data down 10 samples	Shift + Down arrow
Move active cursor up one sample	CTRL + Up arrow
Move active cursor down one sample	CTRL + Down arrow
Move active cursor up 10 samples	CTRL + Shift + Up arrow
Move active cursor down 10 samples	CTRL + Shift + Down arrow

Source Window

Use the Source window to display the high-level language (HLL) source code as it is executed by your target system and acquired by the logic analyzer. The logic analyzer links the Source and Listing windows, and provides additional tools to help you view the tools and data. See Figure 3–95 for an example of a Source window.

The data area of the Source window lists the content of the source file including line numbers for each source code statement. The path name of the file displays immediately above the source data.

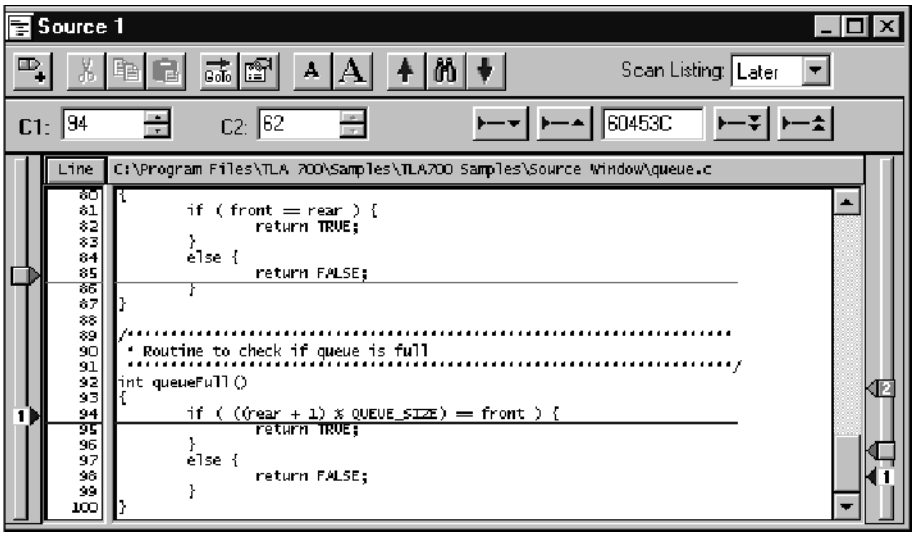


Figure 3-95: Source window

You can use controls to step through data, move between user-defined marks, and scroll through data. These controls directly affect the active cursor in the associated Listing window and indirectly affect the active cursor in the Source window.

Creating a Source Window

Before creating a Source window, load a microprocessor support package. You should also set up the Listing window you will use with the Source window.

Create a new Source window with the New Data Window wizard. You can access the New Data Window wizard from the tool bar in the System window. For help on using the New Data Window wizard, refer to the online help.

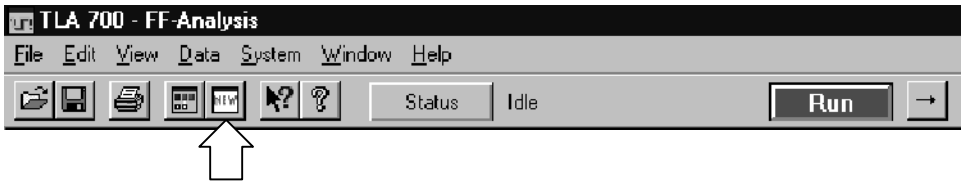


Figure 3-96: Accessing the New Data Window wizard

Reading the Source Window Indicators

Data marks, cursors, and other indicators help you navigate and identify the data. Figure 3–97 and Table 3–22 identify and describe data window marks.

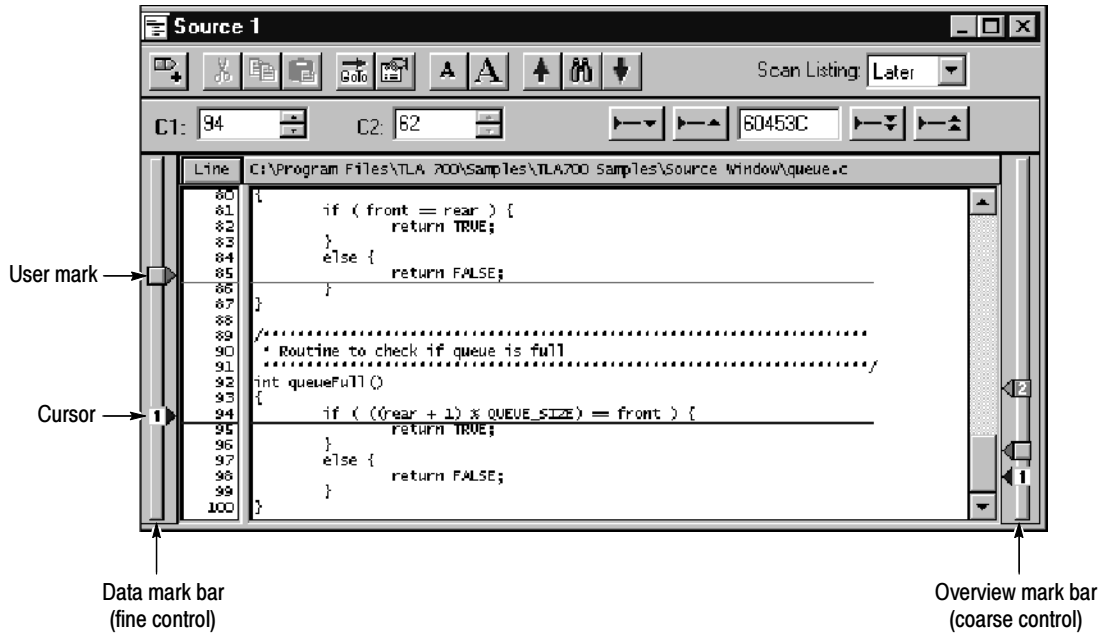


Figure 3-97: Source window cursors and marks

Table 3-22: Source window cursor and mark summary

Mark	Name	Description
1 2	Cursors 1 and 2	Moveable marks used for visual reference and for data measurements.
☐	User mark	User-created marks. Use marks to make specific data easier to identify and find.

Jumping to Specific Data Locations

You can use the Go To dialog box to jump to a new position by selecting any current mark or waveform. To open the Go To dialog box, open a data window, and click the Go To tool bar button, as shown in Figure 3-98.

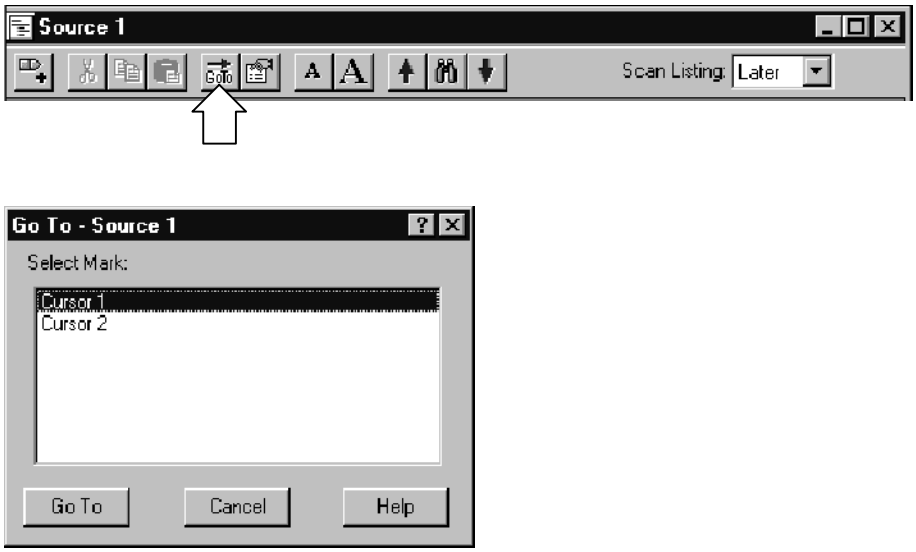


Figure 3-98: Using the Go To dialog box to jump to the cursor location

You can also use the Overview Mark bar to quickly jump to another location. If you do not click a mark, clicking in the Overview Mark bar scrolls to that location.

Moving the cursor between statements in the Source window does not necessarily move the cursor in the same direction in the Listing window. This can happen, for example, if the statement in the new location was executed both before and after the statement in the old location, such as when the statement is in a loop. The Scan Listing box sets the scan direction in a Listing window when you move the cursor in the Source window.

Moving Through Source Files

There are several ways of moving through the data in source files. You can move through source files from the Source window or from the Listing window. When you move a cursor in one window, the corresponding cursor in the other window also moves.

Use the Step Forward or Step Backward buttons (see Figure 3–99) to step through source statements in execution order in the Source window. You can also use the Next Mark or Previous Mark buttons to jump to the next or previous executed source statement that has a user-defined mark.

Use the cursor controls in either window to move the cursors. You can also move the cursors in either window by clicking and dragging the cursor handles or by adjusting the cursor spin box controls.

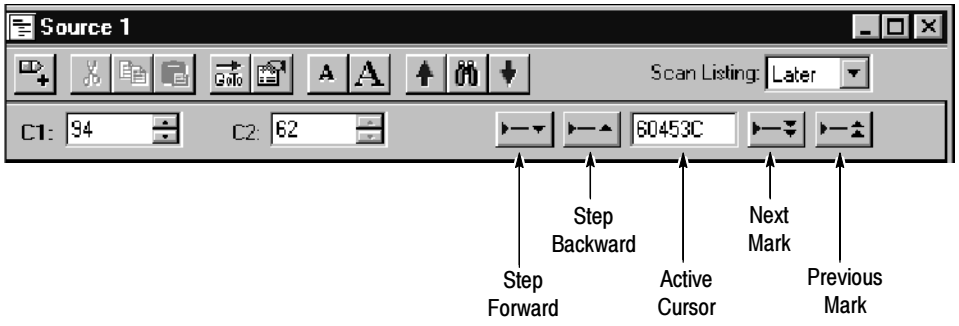


Figure 3- 99: Source window controls

Source-Relative Cursor Positioning

Source-relative cursor positioning refers to updating the Listing window cursor position as a result of changing the position of the active cursor in the Source window.

When you move the Source window cursor to a new statement, the Source window determines the address range of the source statement based on information from the loaded symbol file. The Source window uses the setting of the Scan Listing mode to determine the search direction in the Listing window. The Listing window searches the acquisition data for a matching address. When the matching address is found, the active cursor in the Listing window is moved to the matching sample.

If the Source window cursor is moved to a non-executable statement, such as a comment, the address of the next executable statement is used.

Listing-Relative Cursor Positioning

Listing-relative cursor positioning refers to updating the Source window cursor position as a result of changing the active cursor position in the Listing window.

When you move the Listing window cursor to a new sample, the active Source window cursor attempts to move to a corresponding source statement in the Source window. The Source window uses information from the loaded symbol file to convert the address of the Listing cursor position to a source file name and statement (line number) location. The Source window then updates the active Source window cursor position and displays the corresponding source statement.

Step Forward and Step Backward Buttons

Use the Step Forward and Step Backward buttons to trace the execution order of source statements. Click the Step Forward button to move to the next executed source statement. Click the Step Backward button to move to the previous executed source statement.

When you click the Step Forward or Step Backward buttons, the Source window causes the Listing window to search forward (or backward), beginning at the active Listing cursor, for the next (or previous) executed source statement. When a match is found, the Listing window positions the active Listing cursor to the matching sample. The Source window converts the address to a file name and line number, and then updates the active Source cursor position to the corresponding source statement. The statement may be located in a source file that is different than the original displayed file. In this case, the new file is displayed and the cursor is placed on the proper statement.

A single line in the Source window may consist of more than one statement, for example:

```
for ( i=0; i < NUM_STATES; i++)
```

The next executed statement in the Listing window may appear on the same line in the Source window as the current statement. However, the next executed statement may also appear on a different line (before or after the current statement), or in a different file. Click the Step Forward and Step Backward buttons to move the cursor between statements in execution order.

The ability of the Source window to discriminate between multiple statements on the same line depends on the amount of information provided by the code generation tools. If there is enough information to identify multiple statements per line, the Source window cursors will include character highlighting to identify individual statements on a line.

Next Mark and Previous Mark Buttons

Use the Next Mark and Previous Mark buttons to move the active cursor in the Source window to the next or previous executed user-defined mark position (if any marks have been defined). Next and previous refer to the execution sequence and not to the position of the mark in the window.

The Next Mark and Previous Mark buttons are similar to the Step Forward and Step Backward buttons. However, rather than stepping through every executed statement, you can define marks in the Source window as breakpoints and then step between marks in execution order to move though the source code.

When you click the Next Mark or Previous Mark buttons, the Source window tells the Listing window to search for addresses corresponding to the marked source statements. When a corresponding sample is found, the Listing window positions its active cursor to the matching sample. The Source window converts the address to a file name and line number. It then updates the active Source cursor position and displays the corresponding source statement.

If the code generation tools provide column information for symbol files, you can mark individual statements of multiple-statement lines in the source code. You can then use the Next Mark and Previous Mark buttons to step between the marks and highlight the individual statements.

The Next Mark and Previous Mark buttons are not active if there are no marks defined in the Source window.

Active Cursor Readout

The active cursor readout displays the address of the source statement at the active cursor. The address shown is the low address bound. The radix of the address is always hexadecimal. If you position the cursor on a non-executable statement, such as a comment or white space, the address of the next executable statement is displayed.

Use the active cursor readout to jump to a new location in the source file. Enter an address in this field and the active cursor moves to the corresponding statement. If you enter an address that does not correspond directly to the address of a source statement, the next statement will be used and the address is adjusted.

You can copy and paste the readout value into other locations such as in the event portion of the Clause Definition dialog in the LA Trigger window.

Uncorrelated State

Sometimes you can move the cursor in the Listing window to a location where there is no corresponding source statement. The cursor in the Source window remains at the current location and changes the color of the Source window to signify that an uncorrelated state exists between the Source and Listing windows. When this happens, you can click the Step Forward or the Step Backward buttons to search for an executable source line in the Listing window; this correlates the active cursors in both windows.

Clicking the buttons forces the Listing window to search for a data sample that corresponds to the next or previous line of executed source code. The line of executed code may be in a different source file. If this happens, the Source window displays the required file or prompts you for a path name. The ability to locate source files depends on the Search Path List and Suffix List defined in the Source Files properties tab.

Searching for Source Data

Use the Define Search dialog box to search for specific text patterns. You can search the current source file or search all of the source files identified by the loaded symbol file.

Click the search icon to open the dialog box, and then fill out the search conditions (see Figure 3–100). The active cursor marks the first occurrence of the data.

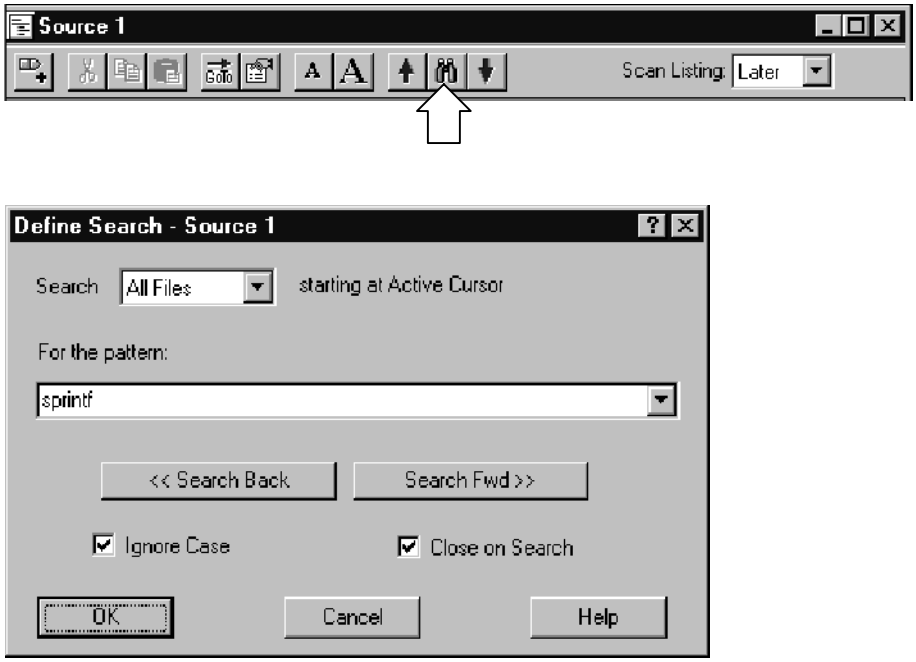


Figure 3-100: Defining source search criteria

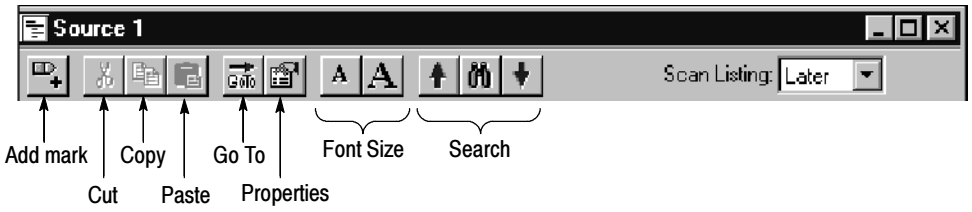
You can search for any text pattern including leading and embedded white space; trailing white space is ignored.

When searching for data in multiple files using the Displayed Source File list, the search operation follows the order of files listed in the Source Window properties tab. When you search for data in all files and one or more of the files cannot be found, the Source File Locator dialog box prompts you to specify the location of the file.

If the search is not completed in a set amount of time, the Search Progress dialog box shows the status of the search. You can let the search continue, or you can click Abort to stop the search.

Adjusting the Source Window

There are a number of actions you can perform in the Source window to get the exact view of the data that you want. You can access most of the shortcuts from the Source window tool bar.



Changing the Display Font Size

Click the Font Size tool bar buttons, shown in the previous figure. You can continue to click the tool bar buttons until the text reaches the desired size. You can also set the font to a specific size using Source window properties.

Cut, Copy, Paste

You can cut, copy, and paste columns and marks. You can also copy text data to the clipboard. From there you can paste it to other areas, such as the Define Search dialog box or the Clause Definition dialog box in the Trigger window.

Turning Line Numbers On or Off

Turn source line numbers on or off by clicking Line Number Column in the View menu.

Customizing the Source Window Data Area

Use the Source properties dialog box to customize data in the Source window. The related properties tabs control aspects of the source display such as source files, text size, colors, tab spacing, and source file locations. Click the Properties tool bar button to open the Source window properties. You can also click the label above the data area to display Source window properties. Then select one of the tabs to change the data you are interested in.

Locating Source Files

You can define the location of source files using the Source Files properties tab (see Figure 3–101). Use the Source Files tab to list the locations of source files as well as possible file suffixes that can be attached to the file names (used for compilers that do not include the file suffixes). A similar tab (System options Source Files tab) is used as a default list of locations of source files and suffixes. The logic analyzer uses this list every time you create a new Source window.

The Source window uses the file path and file suffix in combination to locate the correct source file. It searches for the file name in each directory indicated by the file path list in the order specified. If a file name does not have a suffix, then suffixes from the suffix list are tried until a match is found or all file path and suffix combinations are exhausted.

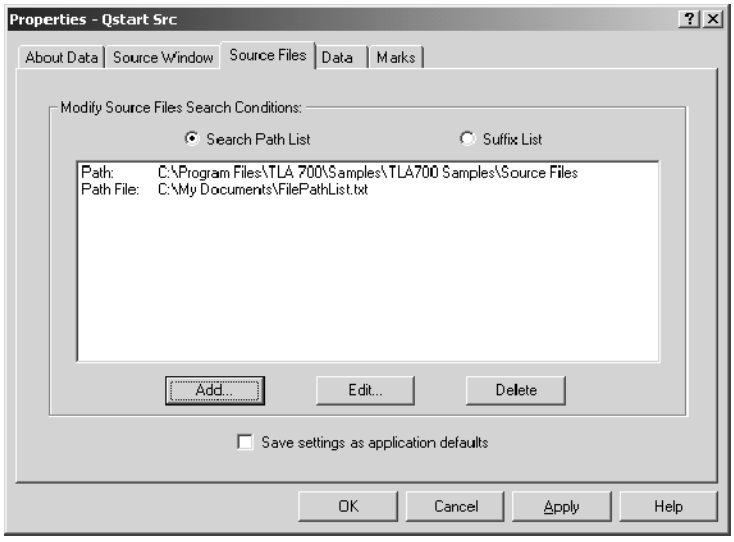


Figure 3-101: Source Files property page

The search path list can also contain a path to a file that lists search paths (path file). When you add a new entry to the search path list (by clicking the Add button), you can specify that the entry is a file that lists directory paths (see Figure 3–102). The path file must already exist when you add it to the list. The paths in the file will be interpreted just as if the paths were specified in the property page.

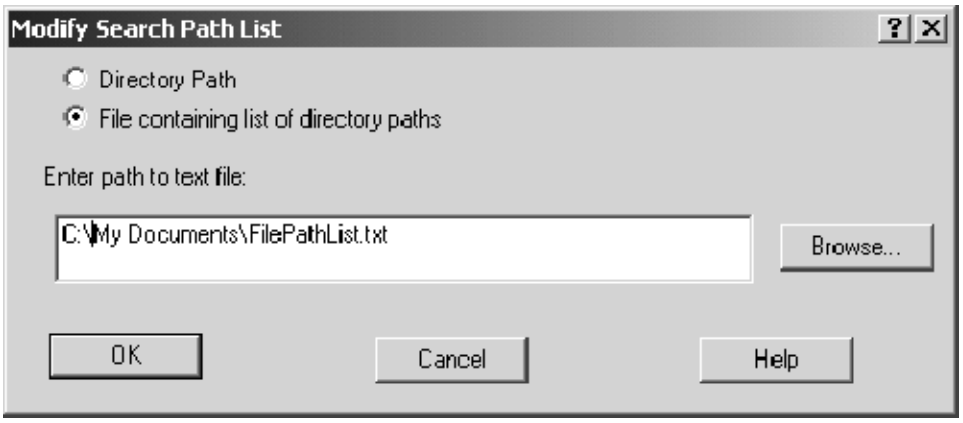


Figure 3-102: Modify Search Path list dialog box

You can intermix paths and path files in the property sheet. Each entry is prefixed with either Path: or Path File: to indicate the type of entry. The paths in a path file will be searched according to the position of the entry in the property page and in the order of the paths listed in the file. The search order is determined as if the entries in the property page were replaced with the contents of the path file.

When specifying the search path, you can use an asterisk (*) as the final component of a search path directory. For example, if you specify the following path, C:\MySources*, the MySources directory and all directories (one level deep) within MySources will be searched. However, you cannot use the asterisk as a general-purpose wild card character. For example, the use of an asterisk in C:\MySources** or C:\MySources\abc* is invalid.

You must specify the complete absolute (not relative) path name for the file in the Search Path List. Otherwise, the Source window will not locate the source file. Make sure that the source file you are looking for has a unique file name. When searching for source files, it is possible to load the wrong file if there is another file with the same name in the directories specified by the search path. The Source window always loads the first file that matches the search criteria.

Because some compilers do not include a source file suffix in the symbol file, you may also need to specify the correct file suffixes in the file suffix list (examples of correct file suffixes are: .c .cpp, and .s). The Source window will always load the first file that matches the criteria in the file suffix list.

The logic analyzer searches for files using both lists from top to bottom. Therefore, you should place the most likely search path or file suffix at the beginning of the lists.

The search path lists and the suffix lists in the Source Files properties tab are valid only for the current Source window. If you want to save the settings as defaults, click Save settings as application defaults near the bottom of the window (see Figure 3–101 on page 3–143). The settings will be saved to the System options Source Files tab and will be used each time you create a new Source window.

Source Window Shortcut Keys

You can use the general-purpose shortcut keys listed in Table 3–23 to move data and cursors in the Source window. You should also refer to the discussions of shortcut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- CTRL + Arrow keys move the active cursor.
- The Shift key increases movement by a factor of 10.

Table 3-23: Source window shortcut keys

Desired action	Key combination
Display Go To dialog box	CTRL + G
Move Cursor 1 to the center of the window	CTRL + 1
Move Cursor 2 to the center of the window	CTRL + 2
Add a mark	CTRL + K
Scroll data up 10 lines	Shift + Up arrow
Scroll data down 10 lines	Shift + Down arrow
Move active cursor up one line	CTRL + Up arrow
Move active cursor down one line	CTRL + Down arrow
Move active cursor up 10 lines	CTRL + Shift + Up arrow
Move active cursor down 10 lines	CTRL + Shift + Down arrow

Histogram Window

Use the Histogram window to set up, capture, and display performance analysis data from an LA module channel group, counter, or timer. You can use the Histogram window to determine the level of activity within various functions or subroutines, analyze how memory is used, or determine the relative execution time of subroutines or program modules.

Histogram data is presented as a list of ranges and corresponding histogram bars showing the distribution of the ranges. See Figure 3–103 for an example.

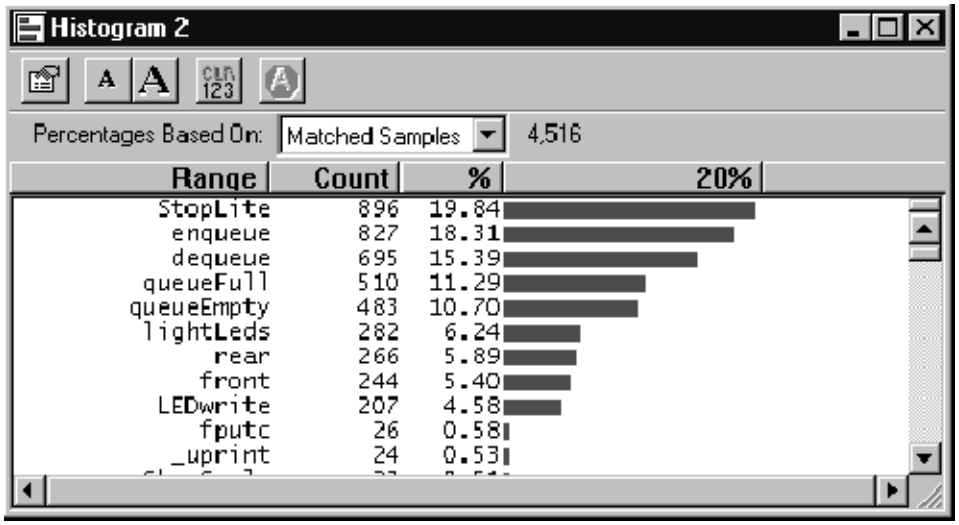


Figure 3-103: Histogram window

The histogram data is based on all acquisition data (All Samples) or on the data within a defined set of ranges (Matched Samples).

Measuring Histogram Data

There are two basic ways of using the Histogram window to analyze data. One is to provide a graphic overview of the address activity of software execution. The other is to use counters or timers to measure specific events.

If you want to use counters or timers to measure events, you must set up the counters or timers in the Trigger window. You can then select the data source in the New Data Window wizard when you create a Histogram window. You can also select the data source for an existing Histogram window from the Data Source properties tab as shown in Figure 3–104.

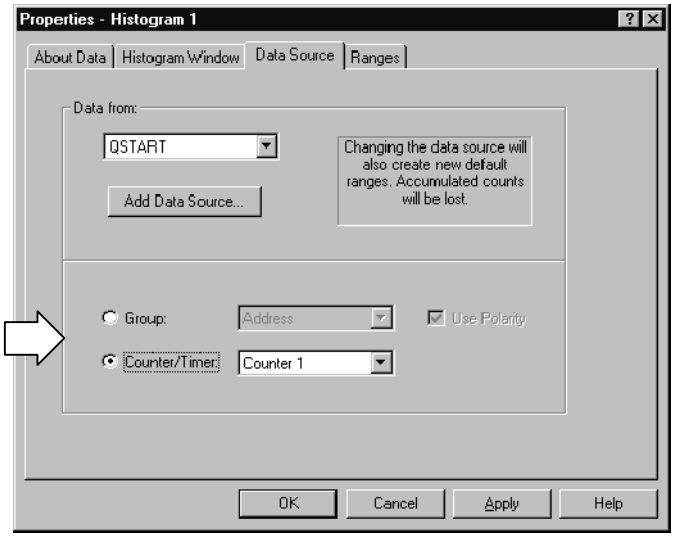


Figure 3- 104: Selecting the data source for the Histogram window

Viewing Address Activity for Channel Groups (Range Overview)

To provide an overview of the address activity of a software routine, you define a set of ranges (numeric, logarithmic, or symbolic). You can set up the Trigger window to look for data within the defined ranges. The data is processed and displayed in the Histogram window for the current acquisition. If you set up the logic analyzer to repetitively acquire data, the sampling errors will decrease over time as you acquire more data. The resultant data provides a stable display in the Histogram window where you can view the overall activity of the software.

You can use this method of analyzing data to determine which sections of code are being accessed or not accessed. You can also determine the time spent in a routine relative to other areas of code. Figure 3–103 is an example of viewing address activity in a software application using symbolic ranges.

Measuring Counter or Timer Events (Single Event)

To measure an event, you define a starting point, a target event, a counter or a timer, and a stopping point in the LA Trigger window. Use the Data Source properties tab to select the counter or timer as the data source for your analysis. When you acquire data, the Histogram window displays the minimum, maximum, and average value of the counter or timer data as shown in Figure 3-105.

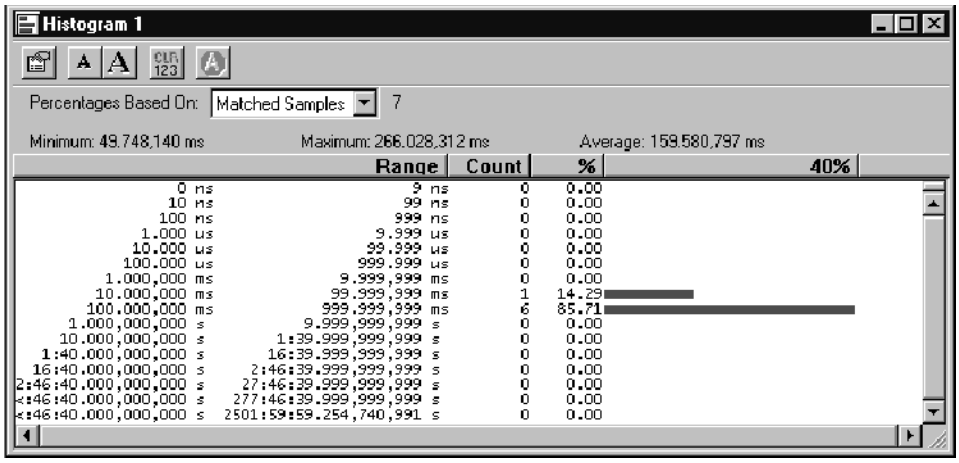
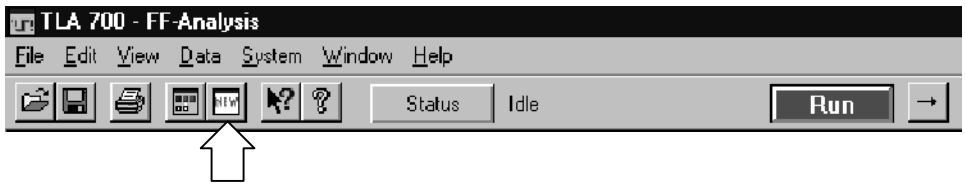


Figure 3-105: Measuring events with the Histogram window

Creating a Histogram Window

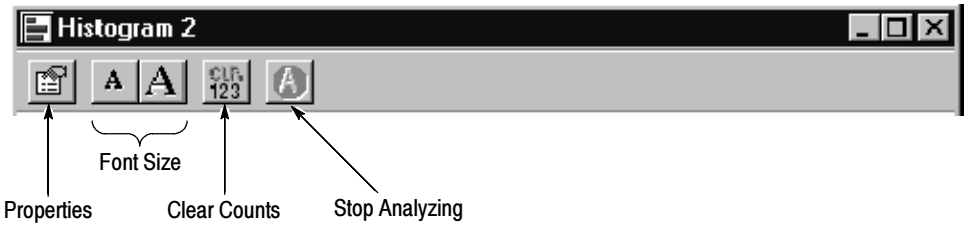
Before creating the Histogram window, define the channel setups and clocking in the Setup window. You should also define your trigger program in the Trigger window. If you want to measure an event, you should define the trigger events and set up the appropriate counter and timer actions. If you want to use symbols, make sure that you load the symbol file.

Create a new Histogram window with the New Data Window wizard. You can access the New Data Window wizard from the tool bar in the System window. For help on using the New Data Window wizard, refer to the online help.



Adjusting the Histogram Window

There are a number of actions you can perform in the Histogram window to get the exact view of the data that you want. Use the buttons in the tool bar to access short cuts to adjust the data.



Changing the Display Font Size

Click the Font Size tool bar buttons, shown in the previous figure. Continue to click the tool bar buttons until the text reaches the desired size. You can also set the font to a specific size using the Histogram Window properties tab.

Clearing Histogram Counts

Click the Clear Counts tool bar button to reset all ranges and percentages to zero.

Stopping Analysis

Click the Stop Analyzing tool bar button to stop analyzing the current acquisition. This button is inactive when there is no current acquisition in process.

Sizing Columns

Select the column label separator and drag it to change the width of a column.

Sorting Data within Columns

Sort ranges, counts, and percentages by clicking on the column labels. Click the column label to toggle the sort between increasing and decreasing values.

Changing Histogram Magnification

Click Scale from the View menu. Select a new magnification value from the list and click OK. You can also click on the percentage column label and select a magnification value.

Defining Histogram Ranges

Ranges displayed in the Histogram window are based on the values you select in the Ranges properties tab. You can define ranges as follows:

- Linear generation. The ranges are divided linearly between two bounds.
- Log generation. The ranges are divided logarithmically between two bounds.
- Symbols. The ranges are defined by the values in a loaded symbol file. You can use the same loaded symbol table as in other windows.

Splitting the Data Area

You can split the data area to compare ranges that are far away from each other within the display. Drag the split box from the top of the horizontal scroll bar.

Customizing the Histogram Window Data Area

Use properties to customize data in the Histogram window. The Histogram Properties dialog box controls aspects of the Histogram display such as ranges, bounds, font size, color, and data source information. Click the Properties toolbar button to open the Histogram Properties dialog box. Then select the specific tab you are interested in.

Here are some guidelines for using and customizing the Histogram window.

- Data is accumulated until you explicitly clear the data.
- There is no limit to the number of symbolic ranges for histogram data.
- You can analyze live LA data or saved LA data (reference data).
- You can use up to 32 bits of data in an address group.
- You can enable or disable channel group polarity.
- You can change colors for the foreground, background, and histogram bars as needed.
- You can change the data font size as necessary to view the data.

Exporting Histogram Data

Use the Export Histogram dialog box to export data from the current Histogram window to a text file. This is a way to print a copy of the histogram data. Figure 3–106 shows the Export Histogram dialog box.

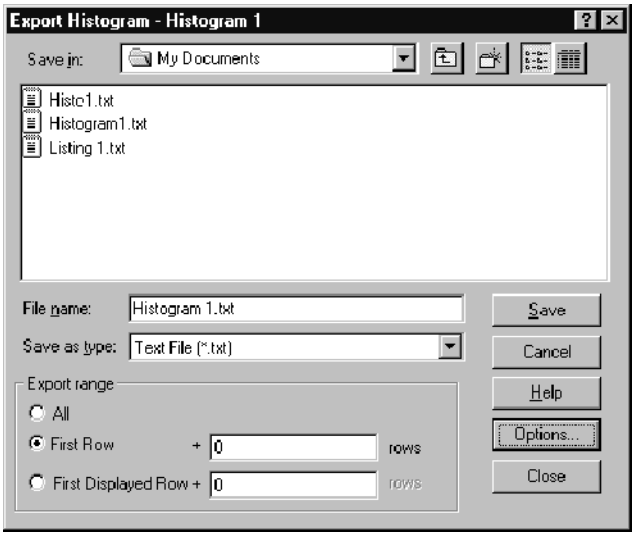


Figure 3- 106: Export Histogram dialog box

Click Options to define the format of the data in the Export Histogram Options dialog. The data is saved in a text file with the .txt file name extension.

Use the Export Data Options dialog to customize the data for a text file. You can specify the field delimiter to separate the columns. To export the bounds as a text string, select Label "00–FF." To export the bounds as two delimited numbers, select Numbers.

To export Histogram data, follow these steps:

1. In the System window, select a Histogram window.
2. From the File menu, click Export Histogram.
3. In the Export Histogram dialog box, select the folder to which you want to export data. Otherwise, leave the default of My Documents.
4. Click Options to specify any export options for the text data and then click OK.
5. Enter a name for the exported file.

6. Specify the export range.
7. Click Save.

Figure 3-107 shows an example of an exported histogram file.

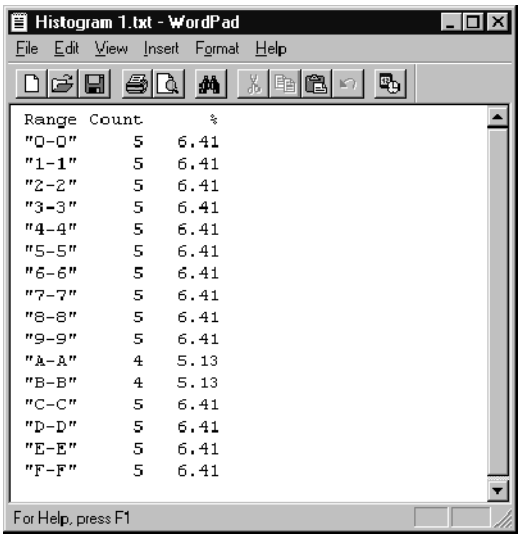


Figure 3-107: ASCII histogram data file

Histogram Window Shortcut Keys

You can use the general-purpose shortcut keys listed in Table 3-24 to move data and cursors in the Histogram window. You should also refer to the discussions of shortcut keys in the online help or under the section for the individual data windows.

The shortcut keys (also known as accelerator keys or hot keys) abide by the following rules:

- Arrow keys with no modifier keys scroll data.
- The Shift key increases movement by a factor of 10.

Table 3-24: Histogram window shortcut keys

Desired action	Key combination
Scroll data up 10 ranges	Shift + Up arrow
Scroll data down 10 ranges	Shift + Down arrow

Appendices

Appendix A: Specifications

This chapter lists the specifications for the Tektronix Logic Analyzer family and the associated modules.

Characteristic Tables

All specifications are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) in the *Tektronix Logic Analyzer Family Performance Verification and Adjustment Technical Reference Manual*.

For mainframes and modules, the performance limits in this specification are valid with these conditions:

- The logic analyzer must be in an environment with temperature, altitude, humidity, and vibration within the operating limits described in these specifications.
- The logic analyzer must have had a warm-up period of at least 30 minutes.

For modules, the performance limits in this specification are valid with these conditions:

- The modules must be installed in a Logic Analyzer Mainframe.
- The module must have been calibrated/adjusted at an ambient temperature between +20 °C and +30 °C.
- The DSO module must have had its signal-path-compensation routine (self calibration or self cal) last executed after at least a 30 minute warm-up period.
- After the warm-up period, the DSO module must have had its signal-path-compensation routine last executed at an ambient temperature within ±5 °C of the current ambient temperature.

For optimum performance using an external oscilloscope, please consult the documentation for any external oscilloscopes used with your Tektronix Logic Analyzer to determine the warm-up period and signal-path compensation requirements.

Atmospheric Characteristics for the Tektronix Logic Analyzer Family

Table A–1 lists the Atmospheric characteristics of all components in the Tektronix Logic Analyzer family.

Table A-1: Atmospheric characteristics

Characteristic	Description
Temperature: Operating and nonoperating	Operating (no media in floppy disk drive): +5 °C to +50 °C, 15 °C/hr maximum gradient, non-condensing (derated 1 °C per 1000 ft above 5000 foot altitude)[1] Nonoperating (no media in floppy disk drive or CD ROM drive): -20 °C to +60 °C, 15 °C/hr maximum gradient, non-condensing.
Relative Humidity: Operating and nonoperating	Operating (no media in floppy disk drive or CD ROM drive): 20% to 80% relative humidity, non-condensing. Maximum wet bulb temperature: +29 °C (derates relative humidity to approximately 22% at +50 °C).[2] Nonoperating (no media in floppy disk drive or CD ROM drive): 8% to 80% relative humidity, non-condensing. Maximum wet bulb temperature: +29 °C (derates relative humidity to approximately 22% at +50 °C).
Altitude: Operating and nonoperating	Operating: To 10,000 ft (3040 m), (derated 1 °C per 1000 ft (305 m) above 5000 ft (1524 m) altitude) Nonoperating: 40,000 ft (12190 m).

1 TLA7Axx series module operating temperature is+40 °C maximum.

2 TLA7Axx series module operating humidity is 45% at +40 °C.

Certifications and Compliances

Table A–2 lists the certifications and compliances of the Tektronix Logic Analyzer family. The certifications and compliances apply to all components of the Tektronix Logic Analyzer family unless noted otherwise.

Table A-2: Certifications and compliances

Category	Standards or description	
EC Declaration of Conformity - EMC	Meets intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:	
	EN 61326	EMC requirements for Class A electrical equipment for measurement, control and laboratory use.[1]
	IEC 61000-4-2	Electrostatic discharge immunity (Performance criterion B)
	IEC 61000-4-3	RF electromagnetic field immunity (Performance criterion A)
	IEC 61000-4-4	Electrical fast transient / burst immunity (Performance criterion B)
	IEC 61000-4-5	Power line surge immunity (Performance criterion B)
	IEC 61000-4-6	Conducted RF immunity (Performance criterion A)
	IEC 61000-4-11	Voltage dips and interruptions immunity (Performance criterion B)
	EN 61000-3-2	AC power line harmonic emissions
Australia / New Zealand Declaration of Conformity - EMC	Complies with EMC provision of Radiocommunications Act per the following standard(s):	
	AS/NZS 2064.1/2	Industrial, Scientific, and Medical Equipment: 1992
EC Declaration of Conformity - Low Voltage	Compliance was demonstrated to the following specification as listed in the Official Journal of the European Communities:	
	Low Voltage Directive 73/23/EEC, amended by 93/68/EEC	
	EN 61010-1/A2:1995	Safety requirements for electrical equipment for measurement control and laboratory use.
U.S. Nationally Recognized Testing Laboratory Listing	UL3111-1	Standard for electrical measuring and test equipment.
Canadian Certification	CAN/CSA C22.2 No. 1010.1	Safety requirements for electrical equipment for measurement, control, and laboratory use.
Additional Compliance	IEC61010-1/A2:1995	Safety requirements for electrical equipment for measurement, control, and laboratory use.
Installation (Overvoltage) Category	Terminals on this product may have different installation (overvoltage) category designations. The installation categories are:	
	CAT II	Local-level mains (wall sockets). Equipment at this level includes appliances, portable tools, and similar products. Equipment is usually cord-connected.

[1] **Emissions which exceed the levels required by this standard may occur when this equipment is connected to a test object.**

Table A-2: Certifications and compliances (Cont.)

Category	Standards or description	
Pollution Degree	A measure of the contaminates that could occur in the environment around and within a product. Typically the internal environment inside a product is considered to be the same as the external. Products should be used only in the environment for which they are rated.	
	Pollution Degree 2	Normally only dry, nonconductive pollution occurs. Occasionally a temporary conductivity that is caused by condensation must be expected. This location is a typical office/home environment. Temporary condensation occurs only when the product is out of service.
Safety Certification Compliance		
Equipment Type	Test and measuring	
Safety Class	Class 1 (as defined in IEC61010-1, Annex H) - grounded product	
Overvoltage Category	Overvoltage Category II (as defined in IEC61010-1, Annex J)	
Pollution Degree	Pollution Degree 2 (as defined in IEC61010-1). Note: Rated for indoor use only.	

TLA600 Series Logic Analyzer Specifications

Tables A–3 through A–17 list the specifications for the TLA600 series logic analyzer.

Table A-3: TLA600 input parameters with probes

Characteristic	Description
✓ Threshold Accuracy	±100 mV
Threshold range and step size	Settable from +5 V to -2 V in 50 mV steps
Threshold channel selection	16 threshold groups assigned to channels. P6417 and P6418 probes have two threshold settings, one for the clock/qualifier channel and one for the data channels. P6434 probes have four threshold settings, one for each of the clock/qualifier channels and two for the data channels (one per 16 data channels).
✓ Channel-to-channel skew	≤ 1.6 ns maximum
Channel-to-channel skew (Typical)	≤ 1.0 ns
Sample uncertainty	
Asynchronous:	Sample period
Synchronous:	500 ps
Probe input resistance (Typical)	20 kΩ
Probe input capacitance: P6417, P6434 (Typical)	2 pF
Probe input capacitance: P6418 (Typical)	1.4 pF data channels 2 pF CLK/Qual channels
Minimum slew rate (Typical)	0.2 V/ns
Maximum operating signal	6.5 V_{p-p} -3.5 V absolute input voltage minimum 6.5 V absolute input voltage maximum
Probe overdrive: P6417, P6418 P6434	 ±250 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±300 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±4 V maximum beyond threshold
Maximum nondestructive input signal to probe	±15 V
Minimum input pulse width signal (single channel) (Typical)	2 ns
Delay time from probe tip to input probe connector (Typical)	7.33 ns

Table A- 4: TLA600 timing latencies

Characteristic	Description
System Trigger and External Signal Input Latencies[1] (Typical)	
External System Trigger Input to LA Probe Tip[2]	-266 ns
External Signal Input to LA Probe Tip via Signal 3, 4[3]	-212 ns + Clk
External Signal Input to LA Probe Tip via Signal 1, 2[3, 4]	-208 ns + Clk
System Trigger and External Signal Output Latencies (Typical)	
LA Probe Tip to External System Trigger Out[5]	376 ns + SMPL
LA Probe Tip to External Signal Out via Signal 3, 4[5]	
OR function	366 ns + SMPL
AND function	379 ns + SMPL
LA Probe Tip to External Signal Out via Signal 1, 2[4, 5]	
normal function	364 ns + SMPL
inverted logic on backplane	364 ns + SMPL

1 **All system trigger and external signal input latencies are measured from a falling-edge transition (active true low) with signals measured in the wired-OR configuration.**

2 **In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.**

3 **"Clk" represents the time to the next master clock at the destination logic analyzer. In the asynchronous (or internal) clock mode, this represents the delta time to the next sample clock beyond the minimum asynchronous rate of 4 ns. In the synchronous (or external) clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied system under test clocks and qualification data.**

4 **Signals 1 and 2 (ECLTRG0, 1) are limited to a "broadcast" mode of operation, where only one source is allowed to drive the signal node at any one time. That single source may be utilized to drive any combination of destinations.**

5 **SMPL represents the time from the event at the probe tip inputs to the next valid data sample. In the Normal Internal clock mode, this represents the delta time to the next sample clock. In the MagniVu Internal clock mode, this represents 500 ps or less. In the External clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.**

Table A- 5: TLA600 external signal interface

Characteristic	Description
System Trigger Input	TTL compatible input via rear panel mounted BNC connectors
Input Levels V_{IH} V_{IL}	TTL compatible input ≥ 2.0 V ≤ 0.8 V
Input Mode	Falling edge sensitive, latched (active low)
Minimum Pulse Width	12 ns
Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods
Maximum Input Voltage	0 to +5 V peak
External Signal Input	TTL compatible input via rear panel mounted BNC connectors
Input Destination	Signal 1, 2, 3, 4
Input Levels V_{IH} V_{IL}	TTL compatible input ≥ 2.0 V ≤ 0.8 V
Input Mode	Active (true) low, level sensitive
Input Bandwidth[1] Signal 1, 2 Signal 3, 4	 50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Accepts signals during valid acquisition periods via real-time gating
Maximum Input Voltage	0 to +5 V peak
System Trigger Output	TTL compatible output via rear panel mounted BNC connectors
Source Mode	Active (true) low, falling edge latched
Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions
Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL-compatible output ≥4 V into open circuit ≥ 2 V into 50 Ω to ground ≤ 0.7 V sinking 10 mA
Output Protection	Short-circuit protected (to ground)
External Signal Output	TTL compatible outputs via rear panel mounted BNC connectors
Source Selection	Signal 1, 2, 3, 4, or 10 MHz clock
Output Modes Level Sensitive	User definable Active (true) low or active (true) high
Output Levels V_{OH} V_{OL}	50 Ohm back terminated TTL output ≥ 4 V into open circuit ≥ 2 V into 50 Ω to ground ≤ 0.7 V sinking 10 mA

Table A-5: TLA600 external signal interface (Cont.)

Characteristic	Description
Output Bandwidth[2] Signal 1, 2 Signal 3, 4	 50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions Outputs 10 MHz clock continuously
Output Protection	Short-circuit protected (to ground)

1 **The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.**

2 **The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.**

Table A-6: TLA600 channel width and depth

Characteristic	Description	
Number of channels	Product	Channels
	TLA601, TLA611, TLA621	32 data and 2 clock
	TLA602, TLA612, TLA622	64 data and 4 clock
	TLA603, TLA613, TLA623	96 data, 4 clock, and 2 qualifier
	TLA604, TLA614, TLA624	128 data, 4 clock, and 4 qualifier
Acquisition memory depth	Product	Memory depth
	TLA601, TLA602, TLA603, TLA604	64 K or 256 K samples[1]
	TLA611, TLA612, TLA613, TLA614	64 K or 256 K samples[1]
	TLA621, TLA622, TLA623, TLA624	1 M samples

1 **PowerFlex options**

Table A-7: TLA600 clocking

Characteristic	Description	
Asynchronous clocking		
✓ Internal sampling period[1]	4 ns to 50 ms in a 1-2-5 sequence 2 ns in 2x Clocking mode	
✓ Minimum recognizable word[2] (across all channels)	Channel-to-channel skew + sample uncertainty Example: for a P6417, P6418, or P6434 Probe and a 4 ns sample period = 1.6 ns + 4 ns = 5.6 ns	
Synchronous clocking		
Number of clock channels[3]	Product	Clock channels
	TLA601, TLA611, TLA621	2
	TLA602, TLA612, TLA622	4
	TLA603, TLA613, TLA623	4
	TLA604, TLA614, TLA624	4
Number of qualifier channels[5]	Product	Qualifier channels
	TLA601, TLA611, TLA621	0
	TLA602, TLA612, TLA622	0
	TLA603, TLA613, TLA623	2
	TLA604, TLA614, TLA624	4
✓ Setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 0.4 ns Maximum setup time = User interface setup time + 0.8 ns Maximum hold time = User interface hold time + 0.2 ns Examples: for a P6417 or a P6418 probe and user interface setup and hold of 2.0/0.0 typical: Maximum window size = 1.6 ns + (2 x 500 ps) + 0.4ns = 3.0 ns Maximum setup time = 2.0 ns + 0.8 ns = 2.8 ns Maximum hold time = 0.0 ns + 0.2 ns = 0.2ns	
Setup and hold window size (data and qualifiers) (Typical)	Channel-to-channel skew (*typical*) + (2 x sample uncertainty) Example: for P6417 or P6418 Probe = 1 ns + (2 x 500 ps) = 2 ns	
Setup and hold window range	The setup and hold window can be moved for each channel group from +8.5 ns (Ts) to -7.0 ns (Ts) in 0.5 ns steps (setup time). Hold time follows the setup time by the setup and hold window size.	
✓ Maximum synchronous clock rate[4]	200 MHz in full speed mode (5 ns minimum between active clock edges) 100 MHz (10 ns minimum between active clock edges)	
Demux clocking		
TLA603, TLA613, TLA623 TLA604, TLA614, TLA624	Channels multiplex as follows: A3(7:0) to D3(7:0) A2(7:0) to D2(7:0) A1(7:0) to D1(7:0) A0(7:0) to D0(7:0)	

Table A-7: TLA600 clocking (Cont.)

Characteristic	Description
TLA601, TLA611, TLA621 TLA602, TLA612, TLA622	Channels multiplex as follows: A3(7:0) to C3(7:0) A2(7:0) to C2(7:0) A1(7:0) to D1(7:0) TLA602, TLA612, TLA622 A0(7:0) to D0(7:0) TLA602, TLA612, TLA622
Time between DeMux clock edges[4] (Typical)	5 ns minimum between Demux clock edges in full-speed mode 10 ns minimum between Demux clock edges in half-speed mode
Time between DeMux store clock edges[4] (Typical)	10 ns minimum between Demux master clock edges in full-speed mode 20 ns minimum between Demux master clock edges in half-speed mode
Data Rate[4] (Typical)	400 MHz (200 MHz option required) half channel. (Requires channels to be multiplexed.) These multiplexed channels double the memory depth.
Clocking state machine	
Pipeline delays	Each channel group can be programmed with a pipeline delay of 0 through 3 active clock edges.

1 It is possible to use storage control and only store data when it has changed (transitional storage).

2 Applies to asynchronous clocking only. Setup and hold window specification applies to synchronous clocking only.

3 Any or all of the clock channels may be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as the active clock edges. The clock channels are stored.

4 Full and half speed modes are controlled by PowerFlex options and upgrade kits.

5 All qualifier channels are stored. For custom clocking there are an additional 4 qualifier channels on C2 3:0 regardless of channel width.

Table A-8: TLA600 trigger system

Characteristic	Description
Triggering Resources	
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available: 16 word recognizers 0 range recognizers 13 word recognizers 1 range recognizer 10 word recognizers 2 range recognizers 7 word recognizers 3 range recognizers 4 word recognizers 4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted.
Glitch detector[1,2]	Each channel group can be enabled to detect a glitch

Table A- 8: TLA600 trigger system (Cont.)

Characteristic	Description
Minimum detectable glitch pulse width (Typical)	2.0 ns (single channel with P6417, P6418, or a P6434 probe)
Setup and hold violation detector[1,3]	Each channel group can be enabled to detect a setup and hold violation. The range is from 8 ns before the clock edge to 8 ns after the clock edge. The range can be selected in 0.5 ns increments. The setup and hold violation of each window can be individually programmed.
Transition detector[1]	Each channel group can be enabled or disabled to detect a transition between the current valid data sample and the previous valid data sample. This mode can be used to create transitional storage selections where all channels are enabled.
Counter/Timers	2 counter/timers, 51 bits wide, can be clocked up to 250 MHz. Maximum count is 2^{51}. Maximum time is 9.007×10^6 seconds or 104 days. Counters and timers can be set, reset, or tested and have zero reset latency.
External Signal In[1]	A backplane input signal
External Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-by-one as External Signal In, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger States	16
✓ Trigger State sequence rate	Same rate as valid data samples received, 250 MHz maximum
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Trigger position is programmable to any data sample (4 ns boundaries)
MagniVu™ acquisition trigger	Triggering of MagniV memory is controlled by the main acquisition trigger
MagniVu™ trigger position	The MagniV trigger position is programmable within 4 ns boundaries and separate from the main acquisition memory trigger position.
Increment counter	Either of the two counter/timers used as counters can be increased.
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer is used as a timer and is reset, the timer continues from the started or stopped state that it was in prior to the reset.
Signal out	A signal sent to the backplane to be used by other instruments
Trigger out	A trigger out signal sent to the backplane to trigger other instruments

Table A-8: TLA600 trigger system (Cont.)

Characteristic	Description
Storage Control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage	When enabled, 31 samples are stored before and after the valid sample. Not allowed when glitch storage or setup and hold violation is enabled.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous clocking rate is reduced to 10 ns.
Setup and hold violation storage	The acquisition memory can be enabled to store setup and hold violation information with each data sample when synchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The maximum clock rate is reduced by half.

1 Each use of External Signal In, glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.

2 Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.5 ns.

3 Any setup value is subject to variation of up to 1.8 ns; any hold value is subject to variation of up to 1.2 ns.

Table A-9: TLA600 MagniVu™ feature

Characteristic	Description
MagniVu memory depth	2016 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 500 ps in a separate high resolution memory. There are no clocking options.

Table A-10: TLA600 Data handling

Characteristic	Description
Nonvolatile memory retention time (Typical)	Battery is integral to the NVRAM. Battery life is > 10 years.

Table A-11: TLA600 internal controller

Characteristic	Description
Operating System	Microsoft Windows
Microprocessor	Intel Celeron, 566 MHz
Main Memory	SDRAM
Style	168 pin DIMM, 2 Sockets
Speed	100 MHz
Installed Configurations	Minimum 256 MB loaded in one socket Maximum 512 MB with both sockets loaded
Real-Time Clock and CMOS Setups, Plug & Play NVRAM Retention Time	Battery life is typically > 3 years when the logic analyzer is not connected to line voltage. When connected to line voltage the life of the battery is extended. Lithium battery, CR3032
Hard Disk Drive	Standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on an EIDE interface.
Size	Minimum 10 GByte Maximum 30 GByte Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
CD-RW Drive	Standard PC compatible IDE (Integrated Device Electronics) 24x-10x-40x CD-RW drive residing on an EIDE interface. Continually subject to change due to the fast-moving PC component environment.
Floppy Disk Drive	Standard 3.5 inch 1.44-MB PC compatible high-density, double-sided floppy disk drive.

Table A-12: TLA600 display system

Characteristic	Description
Classification	Standard PC graphics accelerator technology (bitBLT-based); capable of supporting both internal color LCD display and external color SVGA/XGA monitor
Display Memory	DRAM-based frame-buffer memory
Size	2 MB
Display Selection	Both front panel and external displays can be used simultaneously, each with independent resolutions. Supports Windows dual-monitor capability.
External Display Drive	One SVGA/XGA-compatible analog output port
Display Size	Selected via Windows Plug and Play support for DDC1 and DDC2 A and B Resolution (Pixels) — Colors 640 x 480 — 256, 64 K, 16.8 M 800 x 600 — 256, 64 K, 16.8 M 1024 x 768 — 256, 64 K, 8 M 1280 x 1024 — 256, 64 K, 8 M
Internal Display	
Classification	Thin Film Transistor (TFT) 10.4 inch active-matrix color LCD display; CCFL backlight; intensity controllable via software
Resolution	800 x 600 pixels
Color Scale	262,144 colors (6-bit RGB)

Table A-13: TLA600 front-panel interface

Characteristic	Description
QWERTY Keypad	ASCII keypad to support naming of files, traces, and keyboard equivalents of pointing device inputs for menus
Special Function Knobs	Various functions

Table A-14: TLA600 rear-panel interface

Characteristic	Description
Parallel Interface Port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial Interface Port (COM 1)	9-pin male sub-D connector to support RS-232 serial port
Single USB Ports	One USB (Universal Serial Bus) compliant port
SVGA Output Port (SVGA OUT)	15-pin sub-D SVGA connector
Mouse Port	PS/2 compatible mouse port utilizing a mini DIN connector
Keyboard Port	PS/2 compatible keyboard port utilizing a mini DIN connector
Type I and II PC Card Port	Standard Type I and II PC-compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC-compatible PC card slot

Table A-15: TLA600 AC power source

Characteristic	Description
Source Voltage and Frequency	90-250 V_{RMS}, 45-66 Hz, continuous range CAT II 100-132 V_{RMS}, 360-440 Hz, continuous range CAT II
Fuse Rating	
90 V - 132 V Operation (2 required)	UL198/CSA C22.2 0.25 in × 1.25 in, Fast Blow, 8 A, 250 V
90 V - 250 V Operation (2 required)	IEC 127/Sheet 1 5 mm × 20 mm, Fast Blow, 6.3 A, 250 V
Maximum Power Consumption	600 Watts line power maximum
Steady-State Input Current	6 A_{RMS} maximum
Inrush Surge Current	70 A maximum
Power Factor Correction	Yes
On/Standby Switch and Indicator	Front Panel On/Standby switch, with indicator. The power cord provides main power disconnect.

Table A-16: TLA600 cooling

Characteristic	Description
Cooling System	Forced air circulation (negative pressurization) utilizing six fans operating in parallel
Cooling Clearance	2 in (51 mm), sides and rear; unit should be operated on a flat, unobstructed surface

Table A-17: TLA600 mechanical characteristics

Characteristic	Description
Overall Dimensions	See Figure A-1 for overall chassis dimensions
Weight	Includes empty accessory pouch and front cover
TLA614, TLA624, TLA613, and TLA623	18.1 Kg (40 lbs)
TLA612, TLA622, TLA611, and TLA621	18 Kg (39.75 lbs)
TLA604 and TLA603	17.6 Kg (38.75 lbs)
TLA602 and TLA601	17.5 Kg (38.5 lbs)

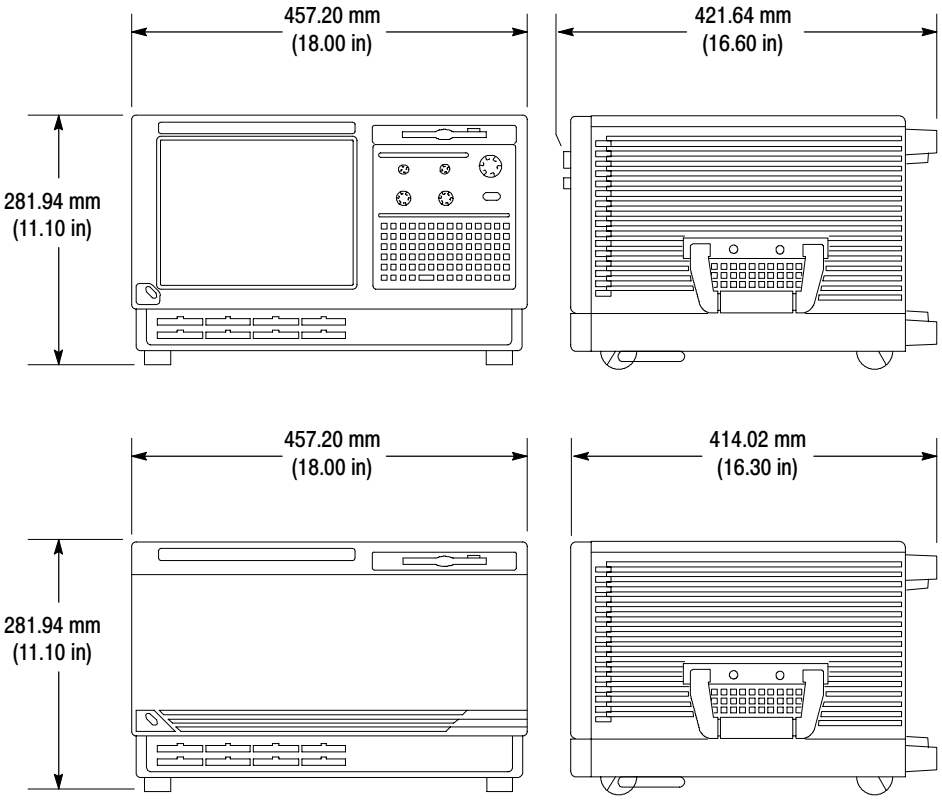


Figure A-1: Dimensions of the TLA600 series logic analyzer

TLA700 System Specifications

Tables A–18 through A–20 list the specifications common to the TLA715, TLA714, TLA720, and TLA721 logic analyzers. Detailed specifications for the individual logic analyzers begin on page A–23.

Table A- 18: TLA700 Backplane interface

Characteristic	Description
Slots	
Portable mainframe	4
Benchtop mainframe	10 (three slots taken up by the controller module)
Expansion mainframe	13
✓ CLK10 Frequency	10 MHz ±100 PPM
Relative Time Correlation Error[1,2] (Typical)	
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx “MagniVu” data	2 ns
TLA7Axx to TLA7Axx “MagniVu” data	2 ns
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx “MagniVu” data	-3 ns
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx “normal” data using an internal clock	1 TLA7Lx/Mx/Nx/Px/Qx sample - 0.5 ns
TLA7Axx to TLA7Axx “normal” data using an internal clock	1 TLA7Axx sample - 0.5 ns
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx “normal” data using an internal clock	1 TLA7Lx/Mx/Nx/Px/Qx sample - 0.5 ns
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx “normal” data using an external clock	2 ns
TLA7Axx to TLA7Axx “normal” data using an external clock	2 ns
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx “normal” data using an external clock	4 ns
TLA7Lx/Mx/Nx/Px/Qx “MagniVu” to DSO data	3 ns
TLA7Axx “MagniVu” to DSO data	2 ns
TLA7Lx/Mx/Nx/Px/Qx to DSO “normal” data using an internal clock[3]	1 TLA7Lx/Mx/Nx/Px/Qx sample + 2 ns
TLA7Axx to DSO “normal” data using an internal clock[3]	1 TLA7Axx sample + 2 ns
TLA7Lx/Mx/Nx/Px/Qx to DSO “normal” data using an external clock[3]	3 ns
TLA7Axx to DSO “normal” data using an external clock[3]	2 ns
DSO to DSO[3]	3 ns

1 Includes typical jitter, slot-to-slot skew, and probe-to-probe variations to provide a “typical” number for the measurement. Assumes standard accessory probes are utilized.

2 For time intervals longer than 1 μs between modules, add 0.01% of the difference between the absolute time measurements to the relative time correlation error to account for the inaccuracy of the CLK10 source.

3 The DSO module time correlation is measured at the maximum sample rate on one channel only.

Table A- 19: TLA700 Backplane latencies

Characteristic	Portable mainframe and benchtop mainframe	Expansion mainframe
System trigger and external signal input latencies[2] (Typical)		
External system trigger input to TLA7Lx/Mx/Nx/Px/Qx probe tip[4]	-266 ns	-230 ns
External system trigger input to TLA7Axx probe tip[4]	-653 ns	-617 ns
External signal input to TLA7Lx/Mx/Nx/Px/Qx probe tip via Signal 3, 4[5]	-212 ns + Clk	-176 ns + Clk
External signal input to TLA7Axx probe tip via Signal 3, 4[5]	-212 ns + Clk	-176 ns + Clk
External signal input to TLA7Lx/Mx/Nx/Px/Qx probe tip via Signal 1, 2[5, 6]	-634 ns + Clk	-596 ns + Clk
External signal input to TLA7Axx probe tip via Signal 1, 2[5, 6]	-636 ns + Clk	-615 ns + Clk
External system trigger input to DSO probe tip[4]	-25 ns	11 ns
System trigger and external signal output latencies[1] *(Typical)*		
TLA7Lx/Mx/Nx/Px/Qx probe tip to external system trigger out	376 ns + SMPL	412 ns + SMPL
TLA7Axx probe tip to external system trigger out	794 ns + SMPL	830 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx probe tip to external signal out via Signal 3, 4[3]		
OR function	366 ns + SMPL	402 ns + SMPL
AND function	379 ns + SMPL	415 ns + SMPL
TLA7Axx probe tip to external signal out via Signal 3, 4[3]		
OR function	792 ns + SMPL	828 ns + SMPL
AND function	800 ns + SMPL	836 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx probe tip to external signal out via Signal 1, 2[3,6]		
normal function	364 ns + SMPL	385 ns + SMPL
inverted logic on backplane	364 ns + SMPL	385 ns + SMPL
TLA7Axx probe tip to external signal out via Signal 1, 2[3,6]		
normal function	796 ns + SMPL	817 ns + SMPL
inverted logic on backplane	796 ns + SMPL	817 ns + SMPL

Table A- 19: TLA700 Backplane latencies (Cont.)

Characteristic	Portable mainframe and benchtop mainframe	Expansion mainframe
DSO probe tip to external system trigger out	68 ns	104 ns
DSO Probe tip to external signal out via Signal 3, 4[3]		
OR function	65 ns	101 ns
AND function	75 ns	111 ns
DSO probe tip to external signal out via Signal 1, 2[3,6]		
normal function	68 ns	89 ns
inverted logic on backplane	71 ns	92 ns
Inter-module latencies (Typical)		
TLA7Lx/Mx/Nx/Px/Qx to DSO inter-module system trigger[1,4]	358 ns + SMPL	394 ns + SMPL
TLA7Axx to DSO inter-module system trigger[1,4]	772 ns + SMPL	808 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module system trigger[1,4]	66 ns + SMPL	102 ns + SMPL
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx inter-module system trigger[1,4]	479 ns + SMPL	515 ns + SMPL
TLA7Axx to TLA7Axx inter-module system trigger[1,4]	116 ns + SMPL	152 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to DSO inter-module ARM[1]	360 ns + SMPL	396 ns + SMPL
TLA7Axx to DSO inter-module ARM[1]	779 ns + SMPL	815 ns + SMPL
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM[1,5]	108 ns + SMPL + Clk	144 ns + SMPL + Clk
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM[1,5]	479 ns + SMPL + Clk	533 ns + SMPL + Clk
TLA7Axx to TLA7Axx inter-module ARM[1,5]	111 ns + SMPL + Clk	147 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2[1,5,6]	116 ns + SMPL + Clk	137 ns + SMPL + Clk
TLA7Axx to TLA7Axx inter-module via Signal 1, 2[1,5,6]	113 ns + SMPL + Clk	134 ns + SMPL + Clk
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2[1,5,6]	534 ns + SMPL + Clk	555 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Q to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4[1,5]	116 ns + SMPL + Clk	152 ns + SMPL + Clk
TLA7Axx to TLA7Axx inter-module via Signal 3, 4[1,5]	124 ns + SMPL + Clk	160 ns + SMPL + Clk
TLA7Axx to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4[1,5]	545 ns + SMPL + Clk	581 ns + SMPL + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx inter-module System Trigger[1,4]	-287 ns + SMPL	-251 ns + SMPL

Table A- 19: TLA700 Backplane latencies (Cont.)

Characteristic	Portable mainframe and benchtop mainframe	Expansion mainframe
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module System Trigger[4]	-240 ns	-204 ns
DSO to TLA7Axx inter-module System Trigger[4]	-598 ns	-562 ns
DSO to DSO inter-module System Trigger[4]	50 ns	86 ns
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx inter-module ARM[1,5]	-300 ns + SMPL + Clk	-264 ns + SMPL + Clk
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module ARM[5]	-192 ns + Clk	-156 ns + Clk
DSO to TLA7Axx inter-module ARM[5]	-600 ns + Clk	-564 ns + Clk
DSO to DSO inter-module ARM	59 ns	95 ns
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 1, 2[5,6]	-179 ns + Clk	-158 ns + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx inter-module via Signal 1, 2[1,5,6]	-294 ns + SMPL + Clk	-273 ns + SMPL + Clk
DSO to TLA7Axx inter-module via Signal 1, 2[5,6]	-598ns + Clk	-577 ns + Clk
TLA7Lx/Mx/Nx/Px/Qx to TLA7Axx inter-module via Signal 3, 4[1,5]	-294 ns + SMPL + Clk	-258 ns + SMPL + Clk
DSO to TLA7Lx/Mx/Nx/Px/Qx inter-module via Signal 3, 4[5]	-184 ns + Clk	-148 ns + Clk
DSO to TLA7Axx inter-module via Signal 3, 4[5]	-598 ns + Clk	-562 ns + Clk

1 SMPL represents the time from the event at the probe tip inputs to the next valid data sample of the LA module. In the Normal Internal clock mode, this represents the delta time to the next sample clock. In the MagniVu Internal clock mode, this represents 500 ps or less. In the External clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine, the system-under-test supplied clocks, and the qualification data.

2 All system trigger and external signal input latencies are measured from a falling-edge transition (active true low) with signals measured in the wired-OR configuration.

3 All signal output latencies are validated to the rising edge of an active (true) high output.

4 In the Waveform window, triggers are always marked immediately except when delayed to the first sample. In the Listing window, triggers are always marked on the next sample period following their occurrence.

5 "Clk" represents the time to the next master clock at the destination logic analyzer. In the asynchronous (or internal) clock mode, this represents the delta time to the next sample clock beyond the minimum asynchronous rate of 4 ns. In the synchronous (or external) clock mode, this represents the time to the next master clock generated by the setup of the clocking state machine and the supplied system under test clocks and qualification data.

6 Signals 1 and 2 are limited to a "broadcast" mode of operation, where only one source is allowed to drive the signal node at any one time. That single source may be utilized to drive any combination of destinations.

Table A-20: TLA700 External signal interface

Characteristic	Description
System Trigger Input	TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Input Levels V_{IH} V_{IL}	TTL compatible input ≥ 2.0 V ≤ 0.8 V
Input destination	System trigger
Input Mode	Falling edge sensitive, latched (active low)
Minimum Pulse Width	12 ns
Active Period	Accepts system triggers during valid acquisition periods via real-time gating, resets system trigger input latch between valid acquisition periods
Maximum Input Voltage	0 to +5 V peak
External Signal Input	TTL compatible input via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Input Destination	Signal 1, 2 Signal 3, 4
Input Levels V_{IH} V_{IL}	TTL compatible input ≥ 2.0 V ≤ 0.8 V
Input Mode	Active (true) low, level sensitive
Input Bandwidth[1] Signal 1, 2 Signal 3, 4	 50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Accepts signals during valid acquisition periods via real-time gating
Maximum Input Voltage	0 to +5 V peak
System Trigger Output	TTL compatible output via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Source selection	System trigger
Source Mode	Active (true) low, falling edge latched
Active Period	Outputs system trigger state during valid acquisition period, resets system trigger output to false state between valid acquisitions
Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL-compatible output ≥4 V into open circuit ≥ 2 V into 50 Ω to ground ≤ 0.7 V sinking 10 ma
Output Protection	Short-circuit protected (to ground)

Table A- 20: TLA700 External signal interface (Cont.)

Characteristic	Description
External Signal Output	TTL compatible outputs via rear panel mounted BNC connectors (portable mainframe) or front panel mounted SMB connectors (benchtop mainframe)
Source Selection	Signal 1, 2 Signal 3, 4 10 MHz clock
Output Modes Level Sensitive	User definable Active (true) low or active (true) high
Output Levels V_{OH} V_{OL}	50 Ω back terminated TTL output ≥ 4 V into open circuit ≥ 2 V into 50 Ω to ground ≤ 0.7 V sinking 10 ma
Output Bandwidth[2] Signal 1, 2 Signal 3, 4	 50 MHz square wave minimum 10 MHz square wave minimum
Active Period	Outputs signals during valid acquisition periods, resets signals to false state between valid acquisitions Outputs 10 MHz clock continuously
Output Protection	Short-circuit protected (to ground)
Intermodule signal line bandwidth	Minimum bandwidth up to which the intermodule signals are specified to operate correctly
Signal 1, 2 Signal 3, 4	50 MHz square wave minimum 10 MHz square wave minimum

1 The Input Bandwidth specification only applies to signals to the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

2 The Output Bandwidth specification only applies to signals from the modules; it does not apply to signals applied to the External Signal Input and sent back to the External Signal Output.

TLA715 Dual Monitor Portable Mainframe Characteristics

Tables A–21 through A–28 describe the specifications for the TLA715 Dual Monitor Portable Mainframe.

Table A- 21: TLA715 Internal controller

Characteristic	Description
Operating system	Microsoft Windows 2000
Microprocessor	Intel Pentium PC-AT configuration with an Intel 815E chip-set and a 733 MHz Pentium III processor
Main memory	SDRAM
Style	144 pin SO DIMM, 2 sockets, gold plated, 1.25-inch (3.175 cm) maximum height
Speed	133 MHz
Available configurations	32, 64, 128, 256 MByte per SO DIMM
Installed configurations	Minimum 256 MB loaded in one socket Maximum 512 MB with both sockets loaded
Cache memory	256 KByte Level 2 (L2) write-back cache
Flash BIOS	256 KByte
Real-time clock and CMOS setups NVRAM	Real-time clock/calendar, standard and advanced PC CMOS setups; see BIOS specification
RTC, CMOS setup, & PNP NVRAM retention time (typical)	> 10 years battery life, lithium battery
Floppy disk drive	Standard 3.5 inch 1.44-MB PC compatible high-density, double-sided floppy disk drive, 500 Kbits/sec transfer rate
Bootable replaceable hard disk drive	Standard PC compatible IDE (Integrated Device Electronics) hard disk drive residing on an EIDE interface.
Size	Minimum 10 GB Maximum 30 GB Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
Interface	ATA -5/enhanced IDE (EIDE)
Average seek time	Read, 12 ms
Average latency	7/14 ms
I/O data transfer rate	33.3 MBytes/sec maximum (U-DMA mode 2)
Cache buffer	2 MBytes (30 GB) /512 KBytes (10GB)
CD-RW drive	Standard PC compatible IDE (Integrated device Electronics) 8x-8x-24x CD-RW drive residing on an IDE interface. Continually subject to change due to the fast-moving PC component environment.

Table A-22: TLA715 display system

Characteristic	Description
Classification	Standard PC graphics-accelerator technology capable of supporting both internal color LCD display and two external color VGA, SVGA, or XGA monitors
Display memory	4 MB SDRAM clocked up to 100 MHz, no external video memory
Display selection	Hardware sense of external SVGA monitor during BIOS boot sequence; defaults to internal color LCD display (indicated by two beeps); automatically switches to external SVGA monitor, if attached (indicated by one beep). Dual (simultaneous) display of external SVGA monitor and internal color LCD is possible via special CMOS "simulscan" setup, as long as internal and external displays operate at same resolution (limited to 800x600 on current LCD) and display rates (simulscan mode indicated by three beeps). Four beeps during the BIOS boot indicates a monochrome LCD was found (not supported). Five beeps indicates no recognizable LCD or external monitor was found. Dynamic Display Configuration 1 (DDC1) support for external SVGA monitor is provided.
External display drive	Two VGA, SVGA, or XGA-compatible analog output ports. Display size is selected via Win2000 display applet.
Display Size (Primary video port with Silicon motion chip)	Resolution (Pixels) / Colors / Refresh Rates 640 x 480 / 256, 64 K, 16.8 M / 60, 75, 85 800 x 600 / 265, 64 K, 16.8 M / 60, 75, 85 1024 x 768 / 256, 64 K, 16.8 M / 60, 75, 85 1280 x 1024 / 256, 64 K, 16.8 M / 60 1600 x 600 / 256, 64 K / 60 1600 x 1200 / 256, 64 K / 60
(Secondary video port with 815E chip set)	Resolution (Pixels) / Colors / Refresh Rates 640 x 480 / 256, 64 K, 16.8 M / 60, 75, 85 800 x 600 / 256, 64 K, 16.8 M / 60, 75, 85 1024 x 768 / 256, 64 K, 16.8 M / 60, 75, 85 1280 x 1024 / 256, 64 K, 16.8 M / 60, 75, 80 1600 x 1200 / 256 / 60, 75
Internal display	
Classification	TFT (Thin Film Transistor) 26 cm active-matrix color LCD display, CCFL backlight, intensity controllable via software
Resolution	800 X 600, 262, 144 colors with 211.2 mm (8.3 in) by 158.4 mm (6.2 in) of viewing area
Color scale	262, 144 colors (6-bit RGB) with a color gamut of 42% at center to NTSC

Table A- 23: TLA715 front-panel interface

Characteristic	Description
QWERTY keypad	31-key ASCII keypad to support naming of files, traces, and keyboard equivalents of pointing device inputs for menus
HEX keypad	25-key HEX keypad supporting standard DSO and LA entry functions
Special function knobs	
Multi-function knob	Various increment/decrement functions dependent on screen or window type
Vertical position	Scrolling and positioning dependent on display type
Vertical scale	Scales waveform displays only
Horizontal position	Scrolling and positioning dependent on display type
Horizontal scale	Scales waveform displays only
Integrated pointing device	Vertically mounted Trackball with two keypad control buttons (SELECT and MENU)
USB port	Front panel (lower left-hand side) dual USB connector
Mouse Port	PS/2 compatible pointing device port
Keyboard Port	PS/2 compatible keyboard port

Table A- 24: TLA715 rear-panel interface

Characteristic	Description
Parallel interface port	36-pin high-density connector supports Output only, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP) Complies with IEEE P1284-C/D2 for bi-directional Parallel Peripheral Interface for Personal Computers (draft) style 1284-C
Serial interface port	9-pin male sub-D connector to support RS-232 serial port
SVGA output Port 1 and Port 2	Two 15-pin sub-D SVGA connectors
PC CardBus32 port	Standard Type I, II, III PC-compatible, PC card slot Complies with PCMCIA 2.1 and JEIDA 4.1

Table A-25: TLA715 AC power source

Characteristic	Description
Source voltage and frequency	90 V_{RMS} to 250 V_{RMS}, 45 Hz to 66 Hz, continuous range CAT II; 100 V_{RMS} to 132 V_{RMS}, 360 Hz to 440 Hz, continuous range CAT II
Fuse rating	
90 V to 250 V operation (159-0046-00)	UL198/CSA C22.2 0.25 in × 1.25 in, Fast Blow, 8 A, 250 V
90 V to 250 V operation (159-0381-00)	IEC 127/Sheet 1 5 mm × 20 mm, Fast Blow, 6.3 A, 250 V
Maximum power consumption	600 W
Steady-state input current	6 A_{RMS} maximum at 90 VAC_{RMS}, 60 Hz or 100 VAC_{RMS}, 400 Hz
Inrush surge current	70 A maximum
Power factor correction	Yes
On/Sleep indicator	Green/yellow front panel LED located next to On/Standby switch provides visual feedback when the On/Off switch is actuated. When the LED is green, the instrument is powered and the processor is not sleeping. When the LED is yellow, the instrument is powered, but the processor is sleeping.
On/Standby switch and indicator	Front panel On/Standby switch. Users can push the switch to power down the instrument without going through the Windows shutdown process; the instrument normally powers down. The power cord provides main power disconnect.

Table A-26: TLA715 secondary power

Characteristic	Description			
⩘ DC Voltage Regulation	Voltage	Minimum	Nominal	Maximum
(Combined System, voltage available at each slot)	+24 V	23.28 V	24.24 V	25.20 V
	+12 V	11.64 V	12.12 V	12.60 V
	+5 V	4.875 V	5.063 V	5.250 V
	-2 V	-2.10 V	-2.00 V	-1.90 V
	-5.2 V	-5.460 V	-5.252 V	-5.044 V
	-12 V	-12.60 V	-12.12 V	-11.64 V
	-24 V	-25.20 V	-24.24 V	-23.28 V

Table A-27: TLA715 cooling

Characteristic	Description
Cooling system	Forced air circulation system with no removable filters using six fans operating in parallel
Pressurization	Negative pressurization system in all chambers including modules
Slot activation	Installing a module activates the cooling for the corresponding occupied slots by opening the airflow shutter mechanism. Optimizes cooling efficiency by only applying airflow to installed modules.
Air intake	Front sides and bottom
Air exhaust	Back rear
Cooling clearance	2 inches (51 mm) front, sides, top, and rear. Prevent blockage of airflow to bottom of instrument by placing on a solid, noncompressable surface; can be operated on rear feet.
Fan speed and operation	All fans operational at half their rated potential and speed (12 VDC)

Table A-28: TLA715 mechanical

Characteristic	Description
Overall dimensions	(See Figure A-3 for overall chassis dimensions) Dimensions are without front feet extended, front cover attached, pouch attached, nor power cord attached.
Height (with feet)	9.25 in (23.5 cm)
Width	17 in (43.18 cm)
Depth	17.5 in (44.45 cm)
Weight	30 lbs 12 oz (13.9 kg) with no modules installed, two dual-wide slot covers, and empty pouch
Shipping configuration	60 lbs 13 oz (27.58 kg) minimum configuration (no modules), with all standard accessories 86 lbs 9 oz (39.26 kg) full configuration, with two TLA 7P4 modules and standard accessories (including probes and clips)
Acoustic noise level (typical)	42.7 dBA weighted (operator) 37.0 dBA weighted (bystander)
Construction materials	Chassis parts are constructed of aluminum alloy; front panel and trim peaces are constructed of plastic; circuit boards are constructed of glass.
Finish type	Tektronix blue body and Tektronix silver-gray trim and front with black pouch, FDD feet, handle, and miscellaneous trim pieces

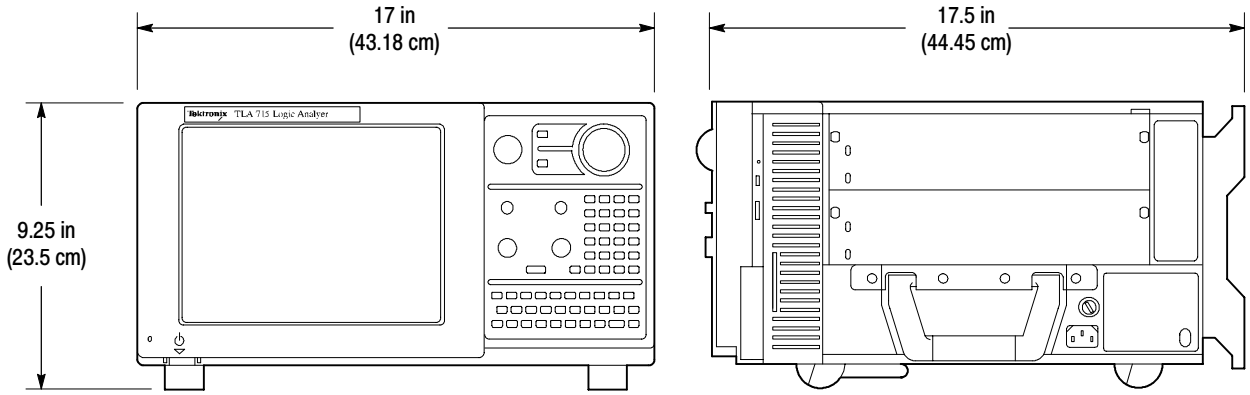


Figure A-2: Dimensions of TLA715 portable mainframe

TLA714 Portable Mainframe Characteristics

Tables A–29 through A–36 describe the specifications for the TLA714 Portable Mainframe.

Table A- 29: TLA714 Internal controller

Characteristic	Description
Operating System	Microsoft Windows
Microprocessor	Intel Pentium PC-AT configuration with a 266 MHz Intel Pentium MMX microprocessor
Main Memory	SDRAM
Style	144 pin SO DIMM, 2 Sockets
Speed	66 MHz
Installed Configurations	Minimum 64 MB loaded in one socket Maximum 128 MB with both sockets loaded
Cache Memory	512 KB Level 2 (L2) write-back cache
Flash BIOS	512 KB Provides PC plug-and-play services with and without Microsoft Windows operating system. Flash based BIOS field upgradable via a floppy disk.
Real-Time Clock and CMOS Setups NVRAM	Real-Time clock/calendar, with typical 10-year life. Standard and advanced PC CMOS setups.
Bootable Replaceable Hard Disk Drive	Standard PC compatible IDE (Integrated device Electronics) hard disk drive residing on an EIDE interface.
Size	Minimum 10 GByte Maximum 30 GByte Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
Interface	ATA 4/Enhanced IDE (EIDE)
Average seek time	Read 13 ms
I/O data-transfer rate	33.3 MB/s max (U-DMA mode 2) (ATA33)
CD-RW Drive	Standard PC compatible IDE (Integrated device Electronics) 8x-8x-24x CD-RW drive residing on an IDE interface Continually subject to change due to the fast-moving PC component environment
Floppy Disk Drive	Standard 3.5 inch 1.44-MB PC compatible high-density, double-sided floppy disk drive

Table A- 30: TLA714 display system

Characteristic	Description
Classification	Standard PC graphics accelerator technology (bitBLT-based); capable of supporting both internal color LCD display and external color SVGA/XGA monitor
Display Memory	DRAM-based frame-buffer memory
Size	2 MB
Display Selection	Hardware sense of external SVGA monitor during BIOS boot sequence; defaults to internal color LCD display; automatically switches to external SVGA monitor, if attached Dual (simultaneous) display of external SVGA monitor and internal color LCD is possible via special “simulscan” CMOS setup, as long as internal and external displays operate at same resolution (limited to 800x600 on current TFT LCD) and display rates Dynamic Display Configuration (DDC2 A and B) support for external SVGA monitor is provided.
External Display Drive	One SVGA/XGA-compatible analog output port
Display Size	User selected via Microsoft Windows Plug and Play support for DDC1 and DDC2 A and B Resolution (Pixels) — Colors 640 x 480 — 256 640 x 480 — 64,000 640 x 480 — 16,800,000 800 x 600 — 256 800 x 600 — 64,000 800 x 600 — 16,800,000 1024 x 768 — 256 1280 x 1024 — 256 1600 x 1200 — 256
Internal Display	
Classification	Thin Film Transistor (TFT) 10.4 inch active-matrix color LCD display; CCFL backlight; intensity controllable via software
Resolution	800 x 600 pixels
Color Scale	262,144 colors (6-bit RGB)

Table A-31: TLA714 front-panel interface

Characteristic	Description
QWERTY Keypad	ASCII keypad to support naming of files, traces, and keyboard equivalents of pointing device inputs for menus
HEX Keypad	HEX keypad supporting text entry functions
Special Function Knobs	Various functions
Integrated Pointing Device	GlidePoint touchpad
Dual USB Ports	Two USB (Universal Serial Bus) compliant ports
Mouse Port	PS/2 compatible mouse port utilizing a mini DIN connector
Keyboard Port	PS/2 compatible keyboard port utilizing a mini DIN connector

Table A-32: TLA714 rear-panel interface

Characteristic	Description
Parallel Interface Port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial Interface Port (COM A)	9-pin male sub-D connector to support RS-232 serial port
SVGA Output Port (SVGA OUT)	15-pin sub-D SVGA connector
Type I and II PC Card Port	Standard Type I and II PC-compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC-compatible PC card slot

Table A-33: TLA714 AC power source

Characteristic	Description
Source Voltage and Frequency	90-250 V_{RMS}, 45-66 Hz, continuous range CAT II 100-132 V_{RMS}, 360-440 Hz, continuous range CAT II
Fuse Rating	
90 V - 250 V Operation (159-0046-00)	UL198/CSA C22.2 0.25 in × 1.25 in, Fast Blow, 8 A, 250 V
90 V - 250 V Operation (159-0381-00)	IEC 127/Sheet 1 5 mm × 20 mm, Fast Blow, 6.3 A, 250 V
Maximum Power Consumption	600 W line power maximum
Steady-State Input Current	6 A_{RMS} maximum
Inrush Surge Current	70 A maximum

Table A-33: TLA714 AC power source (Cont.)

Characteristic	Description
Power Factor Correction	Yes
On/Standby Switch and Indicator	Front Panel On/Standby switch, with LED indicator located next to switch The power cord provides main power disconnect.

Table A-34: TLA714 secondary power

Characteristic	Description			
⩘ DC Voltage Regulation (Combined System, voltage available at each slot)	Voltage	Minimum	Nominal	Maximum
	+24 V	23.28 V	24.24 V	25.20 V
	+12 V	11.64 V	12.12 V	12.60 V
	+5 V	4.875 V	5.063 V	5.250 V
	-2 V	-2.10 V	-2.00 V	-1.90 V
	-5.2 V	-5.460 V	-5.252 V	-5.044 V
	-12 V	-12.60 V	-12.12 V	-11.64 V
	-24 V	-25.20 V	-24.24 V	-23.28 V

Table A-35: TLA714 cooling

Characteristic	Description
Cooling System	Forced air circulation (negative pressurization) utilizing six fans operating in parallel
Cooling Clearance	2 in (51 mm), sides and rear; unit should be operated on a flat, unobstructed surface
Slot Activation	Installing a module activates the cooling for the corresponding occupied slots by opening the air flow shutter mechanism. Optimizes cooling efficiency by only applying airflow to modules that are installed.

Table A-36: TLA714 mechanical

Characteristic	Description
Overall Dimensions	(See Figure A-3 for overall chassis dimensions.)
Height (with feet)	9.25 in (235 mm)
Width	17.0 in (432 mm)
Depth	17.5 in (445 mm)
Weight (Typical)	30 lbs 12 oz. (13.9 kg) with no modules installed, 2 dual-wide slot covers, and empty pouch
Shipping configuration (Typical)	88 lbs (26.3 kg) minimum configuration (no modules or probes), with all standard accessories 87 lb (39.5 kg) full configuration, with 2 TLA7P4 modules and standard accessories (including probes)

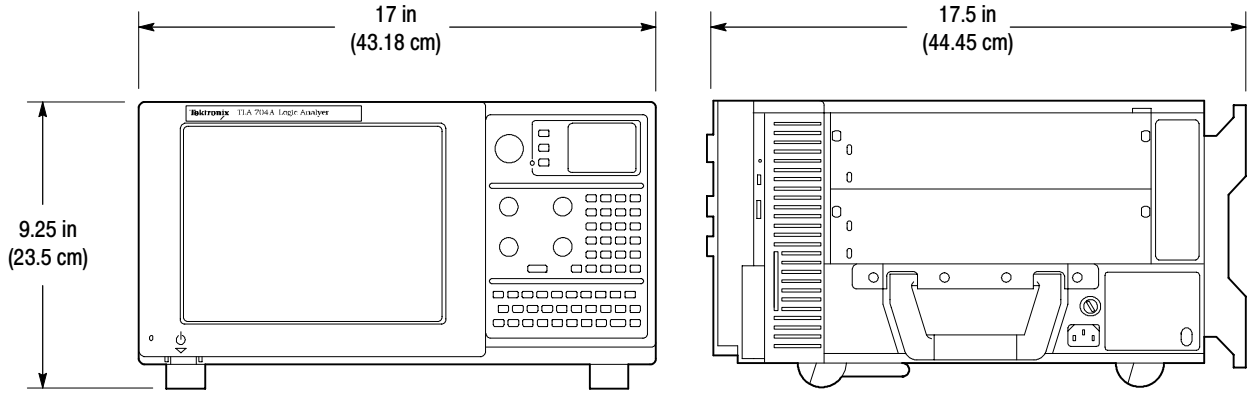


Figure A-3: Dimensions of TLA714 portable mainframe

Benchtop and Expansion Mainframe Characteristics

Tables A–37 through A–41 list the specifications for the TLA720/721 Benchtop mainframe and the TLA7XM expansion mainframe.

Table A-37: Benchtop and expansion mainframe AC power source

Characteristic	Description
Source Voltage	90–250 $V_{RMS,}$ 45–66 Hz, continuous range CAT II 100–132 $V_{RMS,}$ 360–440 Hz, continuous range CAT II
Maximum Power Consumption	1450 W line power (the maximum power consumed by a fully loaded 13-slot instrument)
Fuse Rating (Current and voltage ratings and type of fuse used to fuse the source line voltage)	
90 V - 132 VAC_{RMS} Operation High-power/Low Line (159-0379-00)	Safety: UL198G/CSA C22.2 Size: 0.25 in × 1.25 in Style: Slow acting Rating: 20 A/250 V
103 V - 250 VAC_{RMS} Operation (159-0256-00)	Safety: UL198G/CSA C22.2 Size: 0.25 in × 1.25 in Style: No. 59/Fast acting Rating: 15 A/250 V
207 V - 250 VAC_{RMS} Operation (159-0381-00)	Safety: IEC 127/Sheet 1 Size: 5 mm × 20 mm Style: Fast acting “F”, high-breaking capacity Rating: 6.3 A/250 V
Inrush Surge Current	70 A maximum
Steady State Input Current	16.5 A_{RMS} maximum at 90 VAC_{RMS} 6.3 A_{RMS} maximum at 207 VAC_{RMS}
Power Factor Correction (Typical)	0.99 at 60 Hz operation and 0.95 at 400 Hz operation
ON/Standby Switch and Indicator	Front Panel On/Standby switch with integral power indicator

Table A-38: Benchtop and expansion mainframe secondary power

Characteristic	Description			
⩗ DC Voltage Regulation	Voltage	Minimum	Nominal	Maximum
(Combined System, voltage available at each slot)	+24 V	23.28 V	24.24 V	25.20 V
	+12 V	11.64 V	12.12 V	12.60 V
	+5 V	4.875 V	5.063 V	5.250 V
	-2 V	-2.10 V	-2.00 V	-1.90 V
	-5.2 V	-5.460 V	-5.252 V	-5.044 V
	-12 V	-12.60 V	-12.12 V	-11.64 V
	-24 V	-25.20 V	-24.24 V	-23.28 V

Table A-39: Benchtop and expansion mainframe cooling

Characteristic	Description
Cooling system	Forced air circulation system (positive pressurization) using a single low-noise centripetal (squirrel cage) fan configuration with no filters for the power supply and 13 module slots.
Fan speed control	Rear panel switch selects between full speed and variable speed. Slot exhaust temperature and ambient air temperature are monitored such that a constant delta temperature is maintained.
Slot activation	Installing a module activates the cooling for the corresponding occupied slots by opening the air flow shutter mechanism. Optimizes cooling efficiency by only applying airflow to modules that are installed.
Pressurization	Positive pressurization system, all chambers including modules
Slot airflow direction	P2 to P1, bottom of module to top of module
Mainframe air intake	Lower fan-pack rear face and bottom
Mainframe air exhaust	Top-sides and top-rear back. Top rear-back exhaust redirected to the sides by the fan pack housing to minimize reentry into the intake.
Δ Temperature readout sensitivity	100 mV/ °C with 0 °C corresponding to 0 V output
Temperature sense range	-10 °C to +90 °C, delta temperature ≤ 50 °C
Clearance	2 in (51 mm), rear, top, and sides
Fan speed readout	RPM = 20 × (Tach frequency) or 10 ÷ (+Pulse Width) where (+Pulse Width) is the positive width of the TACH1 fan output signal measured in seconds
Fan speed range	650 to 2250 RPM

Table A-40: Enhanced monitor

Characteristic	Description
Voltage readout	+24 V, -24 V, +12 V, -12 V, +5 V, -5.2 V, -2 V, +5 $V_{Standby}$ if present, and +5 $V_{External}$ via RS232
Voltage readout accuracy (Typical)	±3% maximum
Current readout	Readout of the present current on the +24 V, -24 V, +12 V, -12 V, +5 V, -2 V, -5.2 V rails via RS232
Current readout accuracy (Typical)	±5% of maximum power supply I_{mp}
Rear panel connector levels	±25 VDC maximum, 1 A maximum per pin (Provides access for RS-232 host to enhanced monitor)

Table A-41: Benchtop and expansion mainframe mechanical

Characteristic	Description
Overall Dimensions	(See Figures A-4 and A-5 for overall dimensions.)
Standard	
Height (with feet)	13.7 in (346.7 mm) including feet
Width	16.7 in (424.2 mm)
Depth	26.5 in (673.1 mm)
Rackmount	
Height	13.25 in (336.6 mm)
Width	18.9 in (480.1 mm)
Depth	28.9 in to 33.9 in (734.1 mm to 861.1 mm) in 0.5 in increments, user selectable
Benchtop controller dimensions	
Height	10.32 in (262.1 mm)
Width	2.39 in (60.7 mm)
Depth	14.75 in (373.4 mm)
Expansion module dimensions	
Height	10.32 in (262.1 mm)
Width	1.25 in (31.75 mm)
Depth	14.75 in (373.4 mm)
Weight	
Mainframe with benchtop controller and slot fillers (Typical)	58 lbs 11 oz. (26.7 kg)

Table A- 41: Benchtop and expansion mainframe mechanical (Cont.)

Characteristic	Description
Shipping configuration (Typical)	60 lbs 11 oz. (26.7 kg) minimum configuration with controller (only) and all standard accessories (two manuals, five dual-wide and one single-wide slot filler panels, power cord, empty pouch, front cover, keyboard, software, and cables) 187 lbs (85 kg) fully configured, same as above with the addition of five LA modules (four TLA7P4 modules, one TLA7N4 module) and all module standard accessories (probes and clips)
Benchtop controller	6 lbs 10 oz. (3.0 kg)
Expansion module	3 lbs (1.4 kg)
Maximum per slot	5 lbs (2.27 kg)
Rackmount kit adder	20 lbs (9.1 kg)
Size	
Benchtop controller	Three slots wide
Expansion module	Single slot wide
Acoustic noise level (*Typical*)	
Variable fan speed (at 860 RPM)	43.2 dBA weighted (front) 43.8 dBA weighted (back)
Full speed fan (switched at rear)	66.2 dBA weighted (front) 66.2 dBA weighted (back)
Construction materials	Chassis parts, aluminum alloy Front panel and trim pieces, plastic Circuit boards, glass laminate
Finish type	Mainframes are Tektronix silver gray with dark gray trim on fan pack and bottom feet support rails. Benchtop controllers are Tektronix silver gray on front lexan and injector/ejector assemblies with a black FDD and PC card ejector buttons.

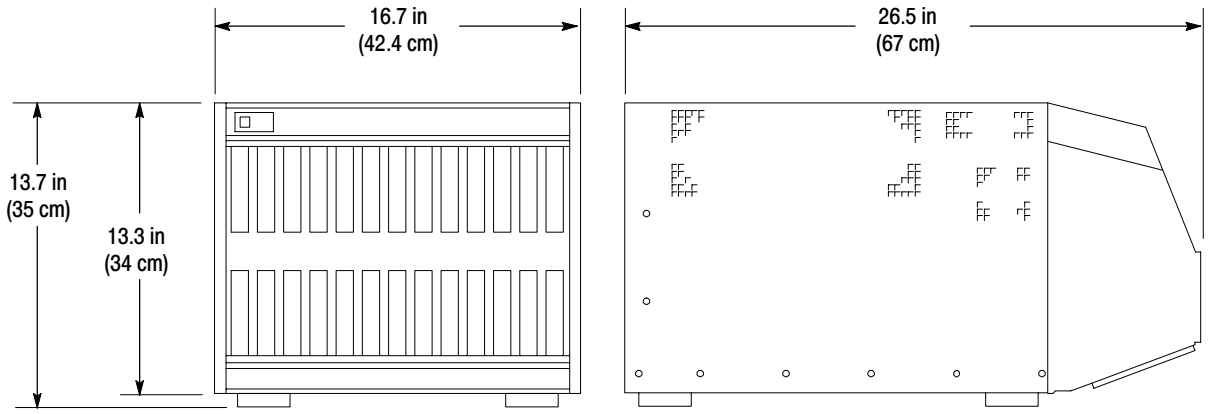


Figure A-4: Dimensions of the benchtop and expansion mainframe

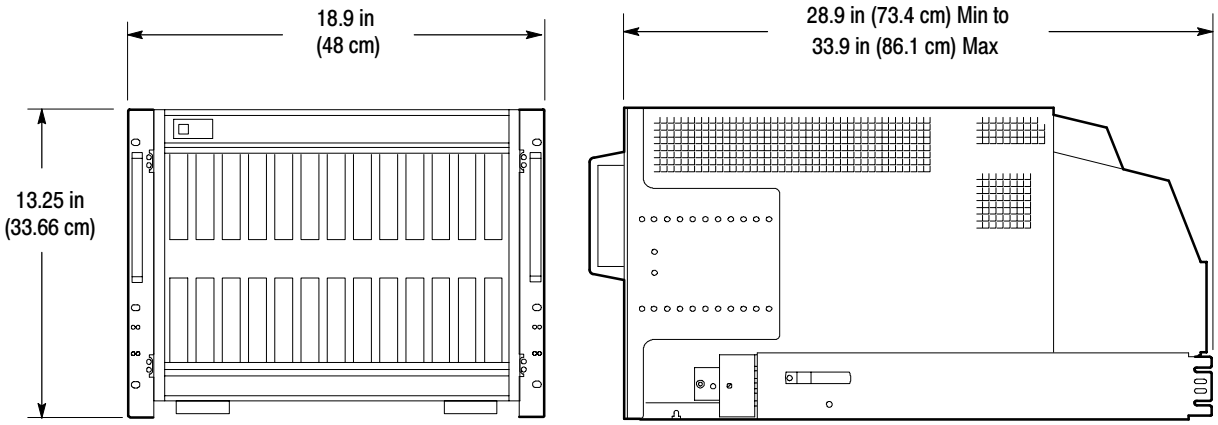


Figure A-5: Dimensions of the benchtop and expansion mainframe with rackmount option

TLA721 Dual Monitor Benchtop Controller Characteristics

Tables A–42 and A–43 lists the specifications for the TLA721 Dual Monitor Benchtop Controller.

Table A–42: TLA721 benchtop controller characteristics

Characteristic	Description
Operating system	Microsoft Windows 2000
Microprocessor	Intel 733 MHz Pentium III configuration with an Intel 815E chip-set
Main memory	Two 144 pin SODIMM sockets support one or two SDRAM modules.
Available configurations	16, 32, 64, 256 MB per SODIMM
Installed configuration	512 MB maximum configuration
Speed	133 MHz
CAS latency	2, 3
RAS to CAS delay	2, 3
RAS precharge	2, 3
DRAM cycle time	5/7 or 7/9
Cache memory	512 KB, level 2 (L2) write-back cache
Flash BIOS	512 KB Provides PC plug-and-play services with and without Microsoft Windows operating system. Flash based BIOS field upgradable via a floppy disk Forced recovery jumper is provided
Real-time clock and CMOS setups NVRAM	Real-time clock/calendar. Standard and advanced PC CMOS setups: see BIOS specifications
RTC, CMOS setup, & PnP NVRAM retention time (Typical)	Battery life is typically > 7 years
Floppy disk drive	Standard 3.5 inch, 1.44 MB, high-density, double-sided, PC-compatible high-density floppy disk drive
Transfer rate	500 Kbits per second
Access time (ave.)	194 ms
Bootable replaceable hard disk drive	Standard PC compatible IDE (Integrated device Electronics) hard disk drive residing on an EIDE interface
Size	Maximum 30 GByte Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
Interface	ATA-5/Enhanced IDE (EIDE)

Table A-42: TLA721 benchtop controller characteristics (Cont.)

Characteristic	Description
Average seek time	Read 12 ms
I/O data-transfer rate	33.3 MB/s maximum (U-DMA mode 2)
Average latency	7/14 ms
Cache buffer	512 KB
CD-RW Drive	Standard PC compatible IDE (Integrated device Electronics) 8x-8x-24x CD-RW drive residing on an IDE interface. Continually subject to change due to the fast-moving PC component environment.
Applicable formats	CD-DA; CE-ROM Mode 1, Mode 2; CD-ROM XA Mode 2 (Form 1, Form 2); Photo CD (single/multi session); Enhanced CD
Interface	IDE (ATAPI)
Average access time	130 ms
Data-transfer rate (burst sustained)	16.7 MB per second maximum, 1290–3000 KB per second
Display classification	Standard PC graphics accelerator technology (bitBLT based) residing on the Peripheral Component Interconnect (PCI) bus capable of supporting external color VGA, SVGA, or XGA monitors
Display configuration	Hardware automatically senses a missing flat panel LCD in the benchtop mainframe and defaults to the external SVGA monitor output during the BIOS boot sequence (no internal TFT LCD display exists). This is indicated by a single beep during the boot sequence. Dynamic Display Configuration 1 (DDC1) support for the external monitor is provided.
Display memory	4 MB SDRAM is on board the video controller; no external video memory
Display drive Display size	Two VGA, SVGA, or XGA compatible analog output ports User selected via Microsoft Windows Plug and Play support for DDC1 and DDC2 A and B (Primary video port with Silicon Motion Chip) Resolution (Pixels) / Colors / Refresh Rates 640 x 480 / 256, 64 K, 16.8 M / 60, 75, 85 800 x 600 / 256, 64 K, 16.8 M / 60, 75, 85 1024 x768 / 256, 64 K, 16.8 M / 60, 75, 85 1280 x 1024 / 256, 64 K, 16.8 M / 60 1600 x 600 / 256, 64 K / 60 1600 x 1200 / 256, 64 K / 60 (Secondary video port with 815E Chip set) Resolution (Pixels) / Colors / Refresh Rates 640 x 480 / 256, 64 K, 16.8 M / 60, 75, 85 800 x 600 / 256, 64 K, 16.8 M / 60, 75, 85 1024 x768 / 256, 64 K, 16.8 M / 60, 75, 85 1280 x 1024 / 256, 64 K, 16.8 M / 60, 75, 85 1600 x 1200 / 256 / 60, 75

Table A-43: Front panel characteristics

Characteristic	Description
SVGA output port (SVGA)	Two 15-pin sub-D SVGA connectors
Dual USB ports	Two USB (Universal Serial Bus) compliant ports
Mouse port	Front panel mounted PS2 compatible mouse port utilizing a mini DIN connector
Keyboard port	Front panel mounted PS2 compatible keyboard port utilizing a mini DIN connector
Parallel interface port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial interface port (COM)	9-pin male sub-D connector to support an RS232 serial port
PC CardBus32 port	Standard Type I and II PC compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC compatible PC card slot

TLA720 Benchtop Controller Characteristics

Tables A–44 through A–45 list the specifications for the TLA720 Benchtop Controller.

Table A–44: TLA720 benchtop controller characteristics

Characteristic	Description
Operating System	Microsoft Windows
Microprocessor	Intel Pentium 266 MHz PC-AT configuration with an Intel chip-set
Main Memory	SDRAM
Style	Two 144 pin SODIMM sockets support one or two SDRAM modules.
Installed Configuration	128 MB Two 64 MB SDRAM modules installed
Speed	60 ns
Cache Memory	256 K, level 2 (L2) write-back cache
Flash BIOS	512 KB Provides PC plug-and-play services with and without Microsoft Windows operating system. Flash based BIOS field upgradable via a floppy disk
Real-Time Clock and CMOS Setups NVRAM (Typical)	Real-time clock/calendar, with typical 7-year life. Standard and advanced PC CMOS setups: see BIOS specification.
Floppy Disk Drive	Standard 3.5 inch, 1.44 MB, double-sided, PC-compatible high-density floppy disk drive
Bootable Replaceable Hard Disk Drive	Standard PC compatible IDE (Integrated device Electronics) hard disk drive residing on an EIDE interface
Size	Maximum 30 GByte Continually subject to change due to the fast-moving PC component environment. These storage capacities valid at product introduction.
Interface	ATA-4/Enhanced IDE (EIDE)
Average seek time	Read 13 ms
I/O data-transfer rate	33.3 MB/s maximum (U-DMA mode 2)
CD-RW Drive	Standard PC compatible IDE (Integrated device Electronics) 8x-8x-24x CD-RW drive residing on an IDE interface. Continually subject to change due to the fast-moving PC component environment.

Table A-44: TLA720 benchtop controller characteristics (Cont.)

Characteristic	Description
Display Classification	Standard PC graphics accelerator technology (bitBLT based) capable of driving external color VGA, SVGA, or XGA monitors
Display Memory	DRAM based frame-buffer memory
Size	2 MB
Display Drive	One VGA, SVGA, or XGA compatible analog output port
Display Size	User selected via Microsoft Windows Plug and Play support for DDC1 and DDC2 A and B Resolution (Pixels) — Colors 640 x 480 — 256 640 x 480 — 64,000 640 x 480 — 16,800,000 800 x 600 — 256 800 x 600 — 64,000 800 x 600 — 16,800,000 1024 x768 — 256 1280 x 1024 — 256 1600 x 1200 — 256
SVGA Output Port (SVGA)	The SVGA port utilizing a 15-pin sub-D SVGA connector
Dual USB Ports	Two USB (Universal Serial Bus) compliant ports
Mouse Port	Front panel mounted PS2 compatible mouse port utilizing a mini DIN connector
Keyboard Port	Front panel mounted PS2 compatible keyboard port utilizing a mini DIN connector
Parallel Interface Port (LPT)	36-pin high-density connector supports standard Centronics mode, Enhanced Parallel Port (EPP), or Microsoft high-speed mode (ECP)
Serial Interface Port (COM)	9-pin male sub-D connector to support an RS232 serial port
Type I and II PC Card Port	Standard Type I and II PC compatible PC card slot
Type I, II, and III PC Card Port	Standard Type I, II, and III PC compatible PC card slot

Table A-45: TLA720 benchtop controller mechanical characteristics

Characteristic	Description
Weight (*Typical*)	6 lb. 10 oz. (2.9 kg)
Size	Three slots wide
Overall dimensions	
Height	10.32 in (262 mm)
Width	3.6 in (83 mm)
Depth	14.7 in (373 mm)

TLA7Axx Series Logic Analyzer Module Characteristics

Tables A–46 though A–54 list the specifications of the TLA7Axx Series Logic Analyzer modules.

Table A-46: TLA7Axx input parameters (with probes)

Characteristic	Description
✓ Threshold accuracy (Certifiable parameter)	± (25 mV + 1% of the threshold voltage setting)
Threshold range and step size	Setable from +4.5 V to -2.0 V in 5 mV steps
Threshold channel selection	16 threshold groups assigned to channels. Each probe has four threshold settings, one for each of the clock/qualifier channels and one per group of 16 data channels.
✓ Channel to channel skew	≤ 400 ps
Channel to channel skew (Typical)	≤ 300 ps
Sample uncertainty	
Asynchronous	Sample period
Synchronous	125 ps
Minimum slew rate (Typical)	0.2 V/ns
Input voltage range	-2.5 V to +5 V
Maximum operating voltage swing	6.0 V peak-to-peak
Probe overdrive	
Single ended probes	± 150 mV or ± 25% of signal swing minimum required beyond threshold, whichever one is greater
Differential probes	V_{pos}-V_{neg} is ≥ 150mV_{p-p}
Maximum nondestructive input signal to probe	± 15 V
Minimum input pulse width (single channel) (Typical)	
P6860 and P6880 probes	500 ps
P6810 probes	750 ps
Delay time from probe tip to input probe connector (*Typical*)	For P6880 High Density Probe: 7.7 ns ± 60 ps

Table A-47: Analog output

Characteristic	Description
Number of outputs	Four analog outputs regardless of the module channel width. Any four of the module's channels can be mapped to the four analog outputs.
Attenuation	10X mode for normal operation 5X mode for small signals (-1.5 V to +2.5 V)
Bandwidth (Typical)	2 GHz
Accuracy (gain and offset) (Typical)	± (50 mV + 2% of signal amplitude)

Table A-48: Channel width and depth

Characteristic	Description
Number of channels	
TLA7AA4, TLA7AB4	128 data, 8 clock/qualifier
TLA7AA3	96 data, 6 clock/qualifier
TLA7AA2, TLA7AB2	64 data, 4 clock/qualifier
TLA7AA1	32 data, 2 clock/qualifier
Acquisition memory depth	
TLA7AAx series	32 M per channel
TLA7ABx series	64 M per channel

Table A-49: Clocking

Characteristic	Description
Asynchronous clocking	
✓ Internal sampling period	500 ps to 50 ms in a 1-2-5 sequence. Storage control can be used to only store data when it has changed (transitional storage) 2 ns minimum for all channels 1 ns minimum for half channels (using 2:1 Demultiplex mode) 0.5 ns minimum for quarter channels (using 4:1 Demultiplex mode)
✓ Minimum recognizable word[1] (across all channels)	Channel-to-channel skew + sample uncertainty Example for a P6860 high-density probe and a 2 ns sample period: 400 ps + 2 ns = 2.4 ns

Table A-49: Clocking (Cont.)

Characteristic	Description	
Synchronous clocking		
Master clock channels[2]	Product	Clock channels
(Unused clock channels can be used as qualifier channels.)	32+2 module	2
	64+4 module	4
	96+6 module	4
	128+8 module	4
Merged slave clock channels[2]	Product	Clock channels
(64+4 channel modules and 32+2 channel modules cannot be merged.)	96+6 module	4
	128+8 module	4
Qualifier channels[3]	Product	Qualifier channels
	32+2 module	0
	64+4 module	0
	96+6 module	2
	128+8 module	4
✓ Setup and hold window size (data and qualifiers)	P6860 high density probe = 750 ps	
Setup and hold window size (data and qualifiers) (Typical)	P6860 high density probe = 625 ps	
Setup and hold window range	The setup and hold window can be moved for each channel group from +8.0 ns (T_S typical) to -8.0 ns (T_S typical) in 0.125 ns steps (setup time). The setup and hold window can be shifted toward the setup region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same setup and hold window. Setup times are specified as typical figures. Hold time follows the setup time by the setup and hold window size.	
Sample point selection window range	The setup and hold window can be moved for each channel group from +8.0 ns to -8.0 ns in 0.125 ns steps. This window can be shifted toward the positive region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same setup and hold window.	
✓ Maximum synchronous clock rate	450 MHz in full-speed mode (2.2 ns minimum between active clock edges) 235 MHz in half-speed mode (4.25 ns minimum between active clock edges) 120 MHz in quarter-speed mode (8.3 ns minimum between active clock edges) 800 MHz on half channels[4] Software controls the selection between full-speed and half-speed modes.	

Table A- 49: Clocking (Cont.)

Characteristic	Description
Demultiplex clocking (two clock edges required)	
Demultiplex channels (2:1) TLA7AA3, TLA7AA4, TLA7AB4 modules	Any individual channel can be demultiplexed with its partner channel. If multiplexing is enabled, all of the A and D channels are multiplexed; there is no individual selection. Channels demultiplex as follows: A3(7:0) to/from D3(7:0) A2(7:0) to/from D2(7:0) A1(7:0) to/from D1(7:0) A0(7:0) to/from D0(7:0)
TLA7AA1, TLA7AA2, TLA7AB2 modules	Any individual channel can be demultiplexed with its partner channel. If multiplexing is enabled, all of the A and D channels are multiplexed; there is no individual selection. Channels demultiplex as follows: A3(7:0) to/from C3(7:0) A2(7:0) to/from C2(7:0) A1(7:0) to/from D1(7:0) 64+4 modules only A0(7:0) to/from D0(7:0) 64+4 modules only
Demultiplex channels (4:1) TLA7AA3, TLA7AA4, TLA7AB4 modules	Unlike the 2:1 Demultiplex, the channels within a group of four cannot arbitrarily drive the others. E3(7:0) to E2(7:0), E1(7:0), E0(7:0) 128+8 modules only A3(7:0) to A2(7:0), D3(7:0), D2(7:0) A1(7:0) to A0(7:0), D1(7:0), D0(7:0) C3(7:0) to C2(7:0), C1(7:0), C0(7:0) CK3 to CK2, Q3, Q2 128+8 modules only CK1 to CK0, Q1, Q0
TLA7AA1, TLA7AA2, TLA7AB2 modules	Unlike the 2:1 Demultiplex, the channels within a group of four cannot arbitrarily drive the others. A1(7:0) to A0(7:0), D1(7:0), D0(7:0) 64+4 modules only C3(7:0) to C2(7:0), A3(7:0), A2(7:0)
Time between Demultiplex clock edges (Typical)	Same limitations as normal synchronous acquisition

Table A-49: Clocking (Cont.)

Characteristic	Description
Source synchronous clocking	
Clocks per module	Four
Clocks with merged modules	When merged, the slave modules have two clocks available from the master module. Including the local clocks, the total is six clocks.
Clock groups	Four for a single module and for a merged system
Size of clock group valid FIFO	Four stages; this allows four (source synchronous or other) clocks to occur before the clock that completes the Clock Group Valid signal for that group
Source synchronous clock alignment window	Channel-to-channel skew only
Source synchronous clock reset	The Clock Group Valid FIFO can be reset in one of the two ways: 1. By the overflow of a presettable (1–255) 8-bit counter that counts one of the following clocks: 2 ns Clock or the master "heartbeat" clock (synchronous or asynchronous). An active edge places the reset count to its preset value. An active clock edge will clear the Clock Group Valid reset before the clock gets to the FIFO so that no data is lost. 2. By enabling an external reset. In this mode, one of the clock channels must be traded on the master module to act as a level-sensitive reset input. Any one of the clocks can be selected. A polarity selection is available. This mode affects all Clock Group Complete circuits. Neither one of the above modes can be intermixed; one or the other must be selected.
Clocking state machine	
Pipeline delays	Channel groups can be programmed with a pipeline delay of 0 through 7 active clock changes.

[1] Specification only applies with asynchronous (internal) clocking. With synchronous clocking, the setup and hold window size applies.

[2] Any or all clock channels can be enabled. For an enabled clock channel, either the rising, falling, or both edges can be selected as active clock edges. Clock channels are stored.

[3] Qualifier channels are stored.

[4] This is a special mode and has some limitations such as the clocking state machine and trigger state machine only running at 500 MHz.

Table A- 50: TLA7Axx module trigger system

Characteristic	Description
Trigger resources	
Word recognizers and range recognizers	16, word recognizers can be combined to form full width, double bounded range recognizers. The following selections are available: 16 word recognizers — 0 range recognizers 13 word recognizers — 1 range recognizer 10 word recognizers — 2 range recognizers 7 word recognizers — 3 range recognizers 4 word recognizers — 4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 Ck1 CK0 Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across the modules. The master module contains the most-significant groups.
Glitch detector (normal asynchronous clock mode)	Channel groups can be enabled to detect glitches. Glitches are subject to pulse width variations of up to $\pm$125 ps
Minimum detectable glitch pulse width (Typical)	Minimum input pulse width (single channel) P6860 high density probe: 500 ps P6880 differential probe: 500 ps P6810 general purpose probe: 750 ps
Setup and hold violation detector (normal asynchronous clock mode)	Any channel group can be enabled to detect a setup or hold violation. The range is from 8.0 ns before the clock edge to 8.0 ns after the clock edge in 0.125 ns steps. The channel setup and hold violation size can be individually programmed. The range can be shifted towards the positive region by 0 ns, 4 ns, or 8 ns. With a 0 ns shift, the range is +8 ns to -8 ns; with a 4 ns shift, the range is +12 ns to -4 ns; with an 8 ns shift, the range is +16 ns to 0 ns. The sample point selection region is the same as the setup and hold window. Any setup value is subject to variation of up to the channel skew specification. Any hold value is subject to variation of up to the channel skew specification.
Transition detector	16 transition detectors. Any channel group can be enabled or disabled to detect a rising transition, a falling transition, or both rising and falling transitions between the current valid data sample and the previous valid data sample.
Counter/timers	2 counter/timers, 51 bits wide, can be clocked up to 500 MHz Maximum count is 2^{51} Maximum time is 4.5×10^6 seconds or 52 days Counters can be used as setable, resettable, and testable flags. Counters can be reset, do nothing, increased, or decreased. Timers can be reset, started, stopped, or not changed. Counters and timers have zero reset latency and one clock terminal count latency.
Signal In 1	A backplane input signal.

Table A-50: TLA7Axx module trigger system (Cont.)

Characteristic	Description
Signal In 2	A backplane input signal.
Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered.
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-for-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger states	16
✓ Trigger state sequence rate	Same rate as valid data samples received. 500 MHz maximum.
Trigger machine actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Programmable to any data sample (2 ns boundaries)
MagniVu trigger	Main acquisition machine controls the triggering of the MagniVu memory
MagniVu trigger position	Programmable within 2 ns boundaries and separate from the main acquisition memory trigger position
Increment/decrement counter	Counter/timers used as counters can be incremented or decremented.
Start/stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer used as a timer is reset, the timer continues in the started or stopped state that it was prior to the reset.
Reloadable word recognizer (snapshot)	Loads the current acquired data sample into the reference value of the word recognizer via a trigger machine action. All data channels are loaded into their respective word recognizer reference register on a one-to-one manner.
Reloadable word recognizer latency	378 ns
Signal Out	A signal sent to the backplane to be used by other modules
Trigger Out	A signal sent to the backplane to trigger other modules
Storage control	
Storage	Storage is allowed only if a specific condition is met. The condition can use any of the trigger resources except for counter/timers. Storage commands defined in the current trigger state will override the global storage control. Storage can be used to start the acquisition with storage initially turned on (default setting) or off.
By event	Storage can be turned on or off; only the current sample can be stored. Event storage control overrides any global storage commands.
Block storage (store stretch)	When enabled, 31 samples are stored before and after the valid sample. This allows the storage of a group of samples around a valid data sample when storage control is being used. This only has meaning when storage control is used. Block storage is disallowed when glitch storage or setup and hold violation storage is enabled.

Table A-50: TLA7Axx module trigger system (Cont.)

Characteristic	Description
Glitch violation storage	Glitch violation information can be stored to acquisition memory with each data sample when asynchronous clocking is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds violation information). The fastest asynchronous clock rate is reduced to 4 ns.
Setup and hold violation storage	Setup and hold violation information can be stored to acquisition memory with each data sample when synchronous clocking is used. The acquisition data storage size is reduced by half when this mode is enabled (the other half holds violation information). The maximum synchronous clock rate in this mode is 235 MHz.

Table A-51: MagniVu acquisition

Characteristic	Description
MagniVu sampling period	Data is asynchronously sampled and stored every 125 ps in a separate MagniVu (high-resolution) memory. The storage speed can be changed by software to 250 ps, 500 ps, or 1000 ps with no loss in memory depth so that the high resolution memory covers more time at a higher resolution.
MagniVu memory depth	Approximately 16 K per channel. The MagniVu memory is separate from the main acquisition memory.

Table A-52: Merged modules

Characteristic	Description
Number of merged modules	2, 3, 4, or 5 adjacent modules can be merged. Only 102-channel modules or 136-channel modules can be merged. Merged modules can have unequal channel widths and channel depths.
Number of channels after merging	The sum of all channels available on each of the merged modules including clocks and qualifiers. No channels are lost when modules are merged.
Merged system acquisition depth	Channel depth is equal to that of the shallowest module.
Number of clock and qualifier channels after merging	The qualifier channels on the slave modules can only be used as data channels. They cannot influence the actual clocking function of the logic analyzer (for example, log strobe generation). The clock channels on the slave TLA7Axx modules can capture data on those modules for source-synchronous applications. Each slave module contributes four additional clock channels to the merged set. All clock and qualifier channels are stored to acquisition memory.
Merged system trigger resources	The same as a single module except for word recognizer width, setup and hold violation detector width, glitch detector width, and transition detector width has increased to equal that of the merged channel width. Range recognizers will increase to the merged channel width up to three modules; range recognition is not supported on the two outside slave modules.
Merged range significance	Most significant Master, Slave 1, Slave 2

Table A-53: Data handling

Characteristic	Description
Nonvolatile memory retention time (*Typical*)	The battery life is integral to the NVRAM; battery life is > 10 years.

Table A- 54: Mechanical

Characteristic	Description
Material	Chassis parts are constructed of aluminum alloy. The front panel is constructed of plastic laminated to steel front panel. Circuit boards are constructed of glass laminate.
Weight	
136-channel module	5 lb 6 oz. (2.438 kg)
102-channel module	5 lb 4 oz. (2.381 kg)
68-channel module	5 lb 0.5 oz. (2.282 kg)
34-channel module	4 lb 15.5 oz. (2.254 kg)
Shipping weight	7 lb 12 oz. (3.515 kg) for 136-channel module when packaged for domestic shipment
Overall dimensions	
Height	10.32 in (262 mm)
Width	2.39 in (61 mm) with merge connector in the recessed position Width increases by 0.41 in (10.41 mm) with merge connector in the extended position
Length	14.7 in (373 mm)
Mainframe interlock	1.4 ECL keying is implemented

TLA7Lx/Mx/Nx/Px/Qx Module Characteristics

Tables A–55 through A–61 list the specifications of the TLALx/Mx/Nx/Px/Qx logic analyzer modules.

Table A-55: LA module channel width and depth

Characteristic	Description	
Number of channels	Product	Channels
	TLA7N1, TLA7L1, TLA7M1	32 data and 2 clock
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2	64 data and 4 clock
	TLA7N3, TLA7L3, TLA7M3	96 data, 4 clock, and 2 qualifier
	TLA7N4, TLA7P4, TLA7Q4, TLA7L4, TLA7M4	128 data, 4 clock, and 4 qualifier
Acquisition memory depth	Product	Memory depth
	TLA7L1, TLA7L2, TLA7L3, TLA7L4	32 K or 128 K samples[1]
	TLA7M1, TLA7M2, TLA7M3, TLA7M4	512 K samples
	TLA7N1, TLA7N2, TLA7N3, TLA7N4	64 K or 256 K or 1 M or 4 M samples[1]
	TLA7P2, TLA7P4	16 M samples
	TLA7Q2, TLAQP4	64 M samples

[1] **PowerFlex options**

Table A-56: LA module clocking

Characteristic	Description	
Asynchronous clocking		
✓ Internal sampling period[1]	4 ns to 50 ms in a 1-2-5 sequence 2 ns in 2x Clocking mode	
✓ Minimum recognizable word[2] (across all channels)	Channel-to-channel skew + sample uncertainty Example: for a P6417 or a P6418 Probe and a 4 ns sample period = 1.6 ns + 4 ns = 5.6 ns	
Synchronous clocking		
Number of clock channels[3]	Product	Clock channels
	TLA7N1, TLA7L1, TLA7M1	2
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2	4
	TLA7N3, TLA7L3, TLA7M3	4
	TLA7N4, TLA7P4, TLA7Q4, TLA7L4, TLA7M4	4

Table A- 56: LA module clocking (Cont.)

Characteristic	Description	
Number of qualifier channels	Product	Qualifier channels
	TLA7N1, TLA7L1, TLA7M1	0
	TLA7N2, TLA7P2, TLA7Q2, TLA7L2, TLA7M2	0
	TLA7N3, TLA7L3, TLA7M3	2
	TLA7N4, TLA7P4, TLA7Q4, TLA7L4, TLA7M4	4
✓ Setup and hold window size (data and qualifiers)	Maximum window size = Maximum channel-to-channel skew + (2 x sample uncertainty) + 0.4 ns Maximum setup time = User interface setup time + 0.8 ns Maximum hold time = User interface hold time + 0.2 ns Maximum setup time for slave module of merged pair = User Interface setup time + 0.8 ns Maximum hold time for slave module of merged pair = User Interface hold time + 0.7 ns Examples: for a P6417, P6418, or P6434 probe and user interface setup and hold of 2.0/0.0 typical: Maximum window size = 1.6 ns + (2 x 500 ps) + 0.4ns = 3.0 ns Maximum setup time = 2.0 ns + 0.8 ns = 2.8 ns Maximum hold time = 0.0 ns + 0.2 ns = 0.2ns	
Setup and hold window size (data and qualifiers) (Typical)	Channel-to-channel skew (*typical*) + (2 x sample uncertainty) Example: for P6417 or P6418 Probe = 1 ns + (2 x 500 ps) = 2 ns	
Setup and hold window range	The setup and hold window can be moved for each channel group from +8.5 ns (Ts) to -7.0 ns (Ts) in 0.5 ns steps (setup time). Hold time follows the setup time by the setup and hold window size.	
✓ Maximum synchronous clock rate[4]	200 MHz in full speed mode (5 ns minimum between active clock edges) 100 MHz in half speed mode (10 ns minimum between active clock edges)	
Demux clocking		
Demux Channels TLA7N3, TLA7N4, TLA7P4, TLA7Q4, TLA 7L3, TLA 7L4, TLA 7M3, TLA 7M4	Channels multiplex as follows: A3(7:0) to D3(7:0) A2(7:0) to D2(7:0) A1(7:0) to D1(7:0) A0(7:0) to D0(7:0)	
TLA7N1, TLA7N2, TLA7P2, TLA7Q2, TLA 7L1, TLA 7L2, TLA 7M1, TLA 7M2	Channels multiplex as follows: A3(7:0) to C3(7:0) A2(7:0) to C2(7:0) A1(7:0) to D1(7:0) TLA7N2, TLA7P2, TLA7Q2, TLA 7L2, TLA 7M2 only A0(7:0) to D0(7:0) TLA7N2, TLA7P2, TLA7Q2, TLA 7L2, TLA 7M2 only	
Time between DeMux clock edges[4] (Typical)	5 ns minimum between DeMux clock edges in full-speed mode 10 ns minimum between DeMux clock edges in half-speed mode	
Time between DeMux store clock edges[4] (Typical)	10 ns minimum between DeMux master clock edges in full-speed mode 20 ns minimum between DeMux master clock edges in half-speed mode	

Table A-56: LA module clocking (Cont.)

Characteristic	Description
Data Rate (Typical) TLA7N1, TLA7N2, TLA7P2, TLA7Q2, TLA7N3, TLA7N4, TLA7P4, TLA7Q4,	400 MHz (200 MHz option required) half channel. (Requires channels to be multiplexed.) These multiplexed channels double the memory depth.
Clocking state machine	
Pipeline delays	Each channel group can be programmed with a pipeline delay of 0 through 3 active clock edges.

1 It is possible to use storage control and only store data when it has changed (transitional storage).

2 Applies to asynchronous clocking only. Setup and hold window specification applies to synchronous clocking only.

3 Any or all of the clock channels may be enabled. For an enabled clock channel, the rising edge, falling edge, or both edges can be selected as the active clock edges. The clock channels are stored.

4 Full and half speed modes are controlled by PowerFlex options and upgrade kits.

Table A-57: LA module trigger system

Characteristic	Description
Triggering Resources	
Word/Range recognizers	16 word recognizers. The word recognizers can be combined to form full width, double bounded, range recognizers. The following selections are available: 16 word recognizers — 0 range recognizers 13 word recognizers — 1 range recognizer 10 word recognizers — 2 range recognizers 7 word recognizers — 3 range recognizers 4 word recognizers — 4 range recognizers
Range recognizer channel order	From most-significant probe group to least-significant probe group: C3 C2 C1 C0 E3 E2 E1 E0 A3 A2 D3 D2 A1 A0 D1 D0 Q3 Q2 Q1 Q0 CK3 CK2 CK1 CK0 Missing channels for modules with fewer than 136 channels are omitted. When merged, the range recognition extends across all the modules; the master module contains the most-significant groups. The master module is to the left (lower-numbered slot) of a merged pair. The master module is in the center when three modules are merged. Slave module 1 is located to the right of the master module, and slave module 2 is located to the left of the master module.
Glitch detector[1,2]	Each channel group can be enabled to detect a glitch
Minimum detectable glitch pulse width (Typical)	2.0 ns (single channel with a P6417, P6418, or P6434 probe)

Table A- 57: LA module trigger system (Cont.)

Characteristic	Description
Setup and hold violation detector[1,3]	Each channel group can be enabled to detect a setup and hold violation. The range is from 8 ns before the clock edge to 8 ns after the clock edge. The range can be selected in 0.5 ns increments. The setup and hold violation of each window can be individually programmed.
Transition detector[1, 4]	Each channel group can be enabled or disabled to detect a transition between the current valid data sample and the previous valid data sample.
Counter/Timers	2 counter/timers, 51 bits wide, can be clocked up to 250 MHz. Maximum count is 2^{51}. Maximum time is 9.007×10^6 seconds or 104 days. Counters and timers can be set, reset, or tested and have zero reset latency.
Signal In 1	A backplane input signal
Signal In 2	A backplane input signal
Trigger In	A backplane input signal that causes the main acquisition and the MagniVu acquisition to trigger if they are not already triggered
Active trigger resources	16 maximum (excluding counter/timers) Word recognizers are traded off one-by-one as Signal In 1, Signal In 2, glitch detection, setup and hold detection, or transition detection resources are added.
Trigger States	16
✓ Trigger State sequence rate	Same rate as valid data samples received, 250 MHz maximum
Trigger Machine Actions	
Main acquisition trigger	Triggers the main acquisition memory
Main trigger position	Trigger position is programmable to any data sample (4 ns boundaries)
Increment counter	Either of the two counter/timers used as counters can be increased.
Start/Stop timer	Either of the two counter/timers used as timers can be started or stopped.
Reset counter/timer	Either of the two counter/timers can be reset. When a counter/timer is used as a timer and is reset, the timer continues in the started or stopped state that it was in prior to the reset.
Signal out	A signal sent to the backplane to be used by other modules
Trigger out	A trigger out signal sent to the backplane to trigger other modules

Table A-57: LA module trigger system (Cont.)

Characteristic	Description
Storage Control	
Global storage	Storage is allowed only when a specific condition is met. This condition can use any of the trigger machine resources except for the counter/timers. Storage commands defined in the current trigger state will override the global storage control. Global storage can be used to start the acquisition with storage initially turned on (default) or turned off.
By event	Storage can be turned on or off; only the current sample can be stored. The event storage control overrides any global storage commands.
Block storage	When enabled, 31 samples are stored before and after the valid sample. Block storage is disallowed when glitch storage or setup and hold violation is enabled.
Glitch violation storage	The acquisition memory can be enabled to store glitch violation information with each data sample when asynchronous clocking is used. The probe data storage size is reduced by one half (the other half holds the violation information). The fastest asynchronous clocking rate is reduced to 10 ns.

1 **Each use of a glitch detector, setup and hold violation detector, or transition detector requires a trade-off of one word recognizer resource.**

2 **Any glitch is subject to pulse width variation of up to the channel-to-channel skew specification + 0.5 ns.**

3 **For TLA7N1, TLA7N2, TLA7N3, TLA7N4, TLA7P2, TLA7P4, TLA7Q2, and TLA7Q4 Logic Analyzer modules, any setup value is subject to variation of up to 1.8 ns; any hold value is subject to variation of up to 1.2 ns. For TLA7L1, TLA7L2, TLA7L3, TLA7L4, TLA7M1, TLA7M2, TLA7M3, and TLA7M4 Logic Analyzer modules, any setup value is subject to variation of up to 1.6 ns; any hold value is subject to variation of up to 1.4 ns.**

4 **This mode can be used to create transitional storage selections where all channels are enabled.**

Table A-58: LA module MagniVu feature

Characteristic	Description
MagniVu memory depth	2016 samples per channel
MagniVu sampling period	Data is asynchronously sampled and stored every 500 ps in a separate high resolution memory.

Table A-59: LA module data handling

Characteristic	Description
Nonvolatile memory retention time (Typical)	Battery is integral to the NVRAM. Battery life is > 10 years.

Table A-60: LA module input parameters with probes

Characteristic	Description
✓ Threshold Accuracy	±100 mV
Threshold range and step size	Settable from +5 V to -2 V in 50 mV steps
Threshold channel selection	16 threshold groups assigned to channels. P6417 and P6418 probes have two threshold settings, one for the clock/qualifier channel and one for the data channels. P6434 probes have four threshold settings, one for each of the clock/qualifier channels and two for the data channels (one per 16 data channels).
✓ Channel-to-channel skew	≤ 1.6 ns maximum (When merged, add 0.5 ns for the slave module.)
Channel-to-channel skew (Typical)	≤ 1.0 ns typical (When merged, add 0.3 ns for the slave module.)
Sample uncertainty	
Asynchronous:	Sample period
Synchronous:	500 ps
Probe input resistance (Typical)	20 kΩ
Probe input capacitance: P6417, P6434 (Typical)	2 pF
Probe input capacitance: P6418 (Typical)	1.4 pF data channels 2 pF CLK/Qual channels
Minimum slew rate (Typical)	0.2 V/ns
Maximum operating signal	6.5 V_{p-p} -3.5 V absolute input voltage minimum 6.5 V absolute input voltage maximum
Probe overdrive: P6417, P6418 P6434	 ±250 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±300 mV or ±25% of signal swing minimum required beyond threshold, whichever is greater ±4 V maximum beyond threshold
Maximum nondestructive input signal to probe	±15 V
Minimum input pulse width signal (single channel) (Typical)	2 ns
Delay time from probe tip to input probe connector (Typical)	7.33 ns

Table A-61: LA module mechanical

Characteristic	Description
Slot width	Requires 2 mainframe slots
Weight (Typical)	5 lbs 10 oz. (2.55 kg) for TLA7N4 and TLA7P4 8 lbs (3.63 kg) for TLA7N4 and TLA7P4 packaged for domestic shipping
Overall dimensions	
Height	262 mm (10.32 in)
Width	61 mm (2.39 in)
Depth	373 mm (14.7 in)
Probe cables	
P6417 length	1.8 m (6 ft)
P6418 length	1.93 m (6 ft 4 in)
P6434 length	1.6 m (5 ft 2 in)
Mainframe interlock	1.4 ECL keying is implemented

DSO Module Characteristics

Tables A-62 through A-66 list the specifications for the DSO Module.

Table A-62: DSO module signal acquisition system

Characteristic	Description		
✓ Accuracy, DC gain	±1.5% for full scale ranges from 20 mV to 100 V ±2.0% for full scale ranges <19.9 mV		
✓ Accuracy, internal offset[1]	*Full scale range setting*	*Offset accuracy*	
	10 mV - 1 V	±[(0.2% × | offset |) + 1.5 mV + (6% × full scale range)]	
	1.01 V - 10 V	±[(0.25% × | offset |) + 15 mV + (6% × full scale range)]	
	10.1 V - 100 V	±[(0.25% × | offset |) + 150 mV + (6% × full scale range)]	
✓ Analog bandwidth, DC-50 Ω coupled	*Full scale range setting*	*Bandwidth[2]*	
	10.1 V - 100 V	DC - 500 MHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
	100 mV - 10 V	DC - 1 GHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
	50 mV - 99.5 mV	DC - 750 MHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
	20 mV - 49.8 mV	DC - 600 MHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
	10 mV - 19.9 mV	DC - 500 MHz (TLA7E1 and TLA7E2) DC - 500 MHz (TLA7D1 and TLA7D2)	
Bandwidth, analog, selections	20 MHz, 250 MHz, and FULL on each channel		
Calculated rise time (Typical)[3]	*Full scale range setting*	*TLA7E1 and TLA7E2*	*TLA7D1 and TLA7D2*
Typical full-bandwidth rise times are shown in the chart to the right	10.1 V - 100 V	900 ps	900 ps
	100 mV - 10 V	450 ps	900 ps
	50 mV - 99.5 mV	600 ps	900 ps
	20 mV - 49.8 mV	750 ps	900 ps
	10 mV - 19.9 mV	900 ps	900 ps
Crosstalk (channel isolation)	≥300:1 at 100 MHz and ≥100:1 at the rated bandwidth for the channel's sensitivity (Full Scale Range) setting, for any two channels having equal sensitivity settings		
Digitized bits	8		

Table A-62: DSO module signal acquisition system (Cont.)

Characteristic	Description		
Effective bits, real time sampling (Typical)	*Input frequency*	*TLA7E1 and TLA7E2 5 GS/s (each channel)*	*TLA7D1 and TLA7D2 2.5 GS/s (each channel)*
	10.2 MHz	6.2 bits	6.2 bits
	98 MHz	6.1 bits	6.1 bits
	245 MHz	6.0 bits	6.0 bits
	490 MHz	5.7 bits	5.7 bits
	990 MHz	5.2 bits	N/A
Frequency limit, upper, 20 MHz bandwidth limited (Typical)	20 MHz		
Frequency limit, upper, 250 MHz bandwidth limited (Typical)	250 MHz		
Input channels	*Product*	*Channels*	
	TLA7E2	Four	
	TLA7D2	Four	
	TLA7E1	Two	
	TLA7D1	Two	
Input coupling	DC, AC, or GND[4]		
Input impedance, DC-1 MΩ coupled	1 MΩ ±0.5% in parallel with 10 pF ±3 pF		
Input impedance selections	1 MΩ or 50 Ω		
Input resistance, DC-50 Ω coupled	50 Ω ±1%		
Input VSWR, DC-50 Ω coupled	≤1.3:1 from DC - 500 MHz, ≤1.5:1 from 500 MHz - 1 GHz		
Input voltage, maximum, DC-1 MΩ, AC-1 MΩ, or GND coupled	300 V_{RMS} but no greater than ±420 V peak, Installation category II, derated at 20 dB/decade above 1 MHz		
Input voltage, maximum, DC-50 Ω or AC-50 Ω Coupled	5 V_{RMS}, with peaks ≤ ±25 V		
Lower frequency limit, AC coupled (Typical)	≤10 Hz when AC-1 MΩ Coupled; ≤200 kHz when AC-50 Ω Coupled[5]		
⩗ Random noise	*Bandwidth selection*	*RMS noise*	
	Full	≤(350 μV + 0.5% of the full scale Setting)	
	250 MHz	≤(165 μV + 0.5% of the full scale Setting)	
	20 MHz	≤(75 μV + 0.5% of the full scale Setting)	

Table A-62: DSO module signal acquisition system (Cont.)

Characteristic	Description				
Range, internal offset	*Full scale range setting*	*Offset range*			
	10 mV - 1 V	±1 V			
	1.01 V - 10 V	±10 V			
	10.1 V - 100 V	±100 V			
Range, sensitivity (full scale range), all channels	10 mV to 100 V[6]				
Step response settling errors (Typical)[7, 8]	*Full scale range setting*	*± Step response*	*Maximum settling error (%) at 20 ns*	*100 ns*	*20 ms*
	10 mV - 1 V	≤2 V	0.5%	0.2%	0.1%
	1.01 V - 10 V	≤20 V	1.0%	0.5%	0.2%
	10.1 V - 100 V	≤200 V	1.0%	0.5%	0.2%

1 Net offset is the nominal voltage level at the digitizing oscilloscope input that corresponds to the center of the A/D Converter dynamic range. Offset accuracy is the accuracy of this voltage level.

2 The limits given are for the ambient temperature range of 0 °C to +30 °C. Reduce the upper bandwidth frequencies by 5 MHz for each °C above +30 °C. The bandwidth must be set to FULL.

3 Rise time (rounded to the nearest 50 ps) is calculated from the bandwidth when Full Bandwidth is selected. It is defined by the following formula:

Rise Time (ns) = 450 ÷ BW (MHz)

4 GND input coupling disconnects the input connector from the attenuator and connects a ground reference to the input of the attenuator.

5 The AC Coupled Lower Frequency Limits are reduced by a factor of 10 when 10X passive probes are used.

6 The sensitivity ranges from 10 mV to 100 V full scale in a 1-2-5 sequence of coarse settings. Between coarse settings, you can adjust the sensitivity with a resolution equal to 1% of the more sensitive coarse setting. For example, between the 500 mV and 1 V ranges, the sensitivity can be set with 5 mV resolution.

7 The Full Bandwidth settling errors are typically less than the percentages from the table.

8 The maximum absolute difference between the value at the end of a specified time interval after the mid-level crossing of the step, and the value one second after the mid-level crossing of the step, expressed as a percentage of the step amplitude. See IEEE std. 1057, Section 4.8.1, *Settling Time Parameters*.

Table A-63: DSO module timebase system

Characteristic	Description	
Range, Extended Realtime Sampling Rate	5 S/s to 10 MS/s in a 1-2.5-5 sequence	
Range, Realtime Sampling Rate	*Products*	*Limits*
	TLA7E1 and TLA7E2	25 MS/s to 5 GS/s on all channels simultaneously in a 1-2.5-5 sequence
	TLA7D1 and TLA7D2	25 MS/s to 2.5 GS/s on all channels simultaneously in a 1-2.5-5 sequence
Record Length	512, 1024, 2048, 4096, 8192, and 15000	
✓ Long Term Sample Rate	±100 ppm over any ≥ 1 ms interval	

Table A-64: DSO module trigger system

Characteristic	Description	
✓ Accuracy (Time) for Pulse Glitch or Pulse Width Triggering	*Time Range*	*Accuracy*
	2 ns to 500 ns	±(20% of Setting + 0.5 ns)
	520 ns to 1 s	±(104.5 ns + 0.01% of Setting)
✓ Accuracy (DC) for Edge Trigger Level, DC Coupled	±((2% × | Setting) |) + 0.03 of Full Scale Range + Offset Accuracy) for signals having rise and fall times ≥20 ns	
Range (Time) for Pulse Glitch and Pulse Width Triggering	2 ns to 1 s	
Range, Trigger Level	*Source*	*Range*
	Any Channel	±100% of full scale range
Range, Trigger Point Position	Minimum: 0% Maximum: 100%	
Resolution, Trigger Level	0.2% of full scale for any Channel source	
Resolution, Trigger Position	One Sample Interval at any Sample Rate	
Sensitivities, Pulse-Type Runt Trigger *(Typical)*	10% of full scale, from DC to 500 MHz, for vertical settings >100 mV full scale and ≤10 V full scale at the BNC input	
Sensitivities, Pulse-Type Trigger Width and Glitch *(Typical)*	10% of full scale for vertical settings >100 mV full scale and ≤10 V full scale at the BNC input	

Table A- 64: DSO module trigger system (Cont.)

Characteristic	Description		
✓ Sensitivity, Edge-Type Trigger, DC Coupled	The minimum signal levels required for stable edge triggering of an acquisition when the trigger source is DC-coupled		
	Products	*Trigger Source*	*Sensitivity*
	TLA7E1 and TLA7E2	Any Channel	3.5% of Full Scale Range from DC to 50 MHz, increasing to 10% of Full Scale Range at 1 GHz
	TLA7D1 and TLA7D2	Any Channel	3.5% of Full Scale Range from DC to 50 MHz, increasing to 10% of Full Scale Range at 500 MHz
Sensitivity, Edge-Type Trigger, Not DC Coupled (Typical)	*Trigger Coupling*	*Typical Signal Level for Stable Triggering*	
	AC	Same as the DC-coupled limits for frequencies above 60 Hz; attenuates signals below 60 Hz	
	High Frequency Reject	One and one-half times the DC-coupled limits from DC to 30 kHz; attenuates signals above 30 kHz	
	Low Frequency Reject	One and one-half times the DC-coupled limits for frequencies above 80 kHz; attenuates signals below 80 kHz	
	Noise Reject	Three times the DC-coupled limits	
Time, Minimum Pulse or Rearm, and Minimum Transition Time, for Pulse-Type Triggering (Typical)	For vertical settings >100 mV and ≤10 V at the BNC input		
	Pulse Class	*Minimum Pulse Width*	*Minimum Rearm Width*
	Glitch	1 ns	2 ns + 5% of Glitch Width Setting
	Width	1 ns	2 ns + 5% of Width Upper Limit Setting
Trigger Position Error, Edge Triggering (Typical)	*Acquisition Mode*	*Trigger Position Error*[1]	
	Sample	±(1 Sample Interval + 1 ns)	

[1] **The trigger position errors are typically less than the values given here. These values are for triggering signals having a slew rate at the trigger point of ≥5% of full scale/ns.**

Table A-65: DSO module front-panel connectors

Characteristic	Description
⌐ Probe Compensator, Output Voltage The Probe Compensator output voltage in peak-to-peak Volts	0.5 V (base-top) ± 1% into a ≥ 50 Ω load

Table A-66: DSO module mechanical

Characteristic	Description	
Slot width	Requires 2 mainframe slots	
Weight (Typical)	*Products*	*Weight*
	TLA7D1 and TLA7E1	2.44 kg (5.38 lbs)
	TLA7D2 and TLA7E2	2.55 kg (5.63 lbs)
Shipping Weight (Typical)	*Products*	*Weight*
	TLA7D1 and TLA7E1	6.35 kg (14 lbs)
	TLA7D2 and TLA7E2	7.71 kg (17 lbs)
Overall Dimensions	Height: 262.05 mm (10.32 in) Width: 60.66 mm (2.39 in) Depth: 373.38 mm (14.70 in)	

TLA7PG2 Pattern Generator Module Characteristics

Tables A–67 through A–72 list the specifications for the pattern generator module. For information on the individual pattern generator probes, refer to TLA7PG2 *Pattern Generator Probe Instruction Manual*.

Table A-67: PG module electrical specification, operational mode

Characteristic	Description	
Operational mode		
Normal	Pattern data output is synchronized by the internal/external clock input	
Step	Pattern data output is synchronized by the software command	
Output pattern		
✓ Maximum Operating Clock Frequency	134 MHz in Full Channel Mode 268 MHz in Half Channel Mode	
Pattern length	40 to 262,140 (2^{18} - 4) in Full Channel Mode (standard) 80 to 524,280 (2^{19} - 8) in Half Channel Mode (standard) 40 to 1,048,572 (2^{20} - 4) in Full Channel Mode (option 1M or PowerFlex upgrade) 80 to 2,097,144 (2^{21} - 8) in Half Channel Mode (option1M or PowerFlex upgrade)	
Number of channels	64 channels in Full Channel Mode 32 channels in Half Channel Mode The pattern memory for the following data channel will be shared with strobe control/internal inhibit control	
	Probe D data output channel	*Control*
	D0:0	STRB0
	D0:1	STRB1
	D0:2	STRB2
	D0:3	STRB3
	D0:4	Inhibit probe A
	D0:5	Inhibit probe B
	D0:6	Inhibit probe C
	D0:7	Inhibit probe D
Sequences	Maximum 4,000	
Number of blocks	Maximum 4,000	
Number of subsequences	Maximum 50	
Subsequences	Maximum 256 steps	
Repeat count	1 to 65,536 or infinite	

Table A-68: PG module clocking

Characteristic	Description
Internal clock	
Clock Period	2.0000000 s to 7.462865 ns in Full Channel Mode 1.0000000 s to 3.7313432 ns in Half Channel Mode
Period Resolution	8 digits
Frequency Accuracy	± 100 PPM
External clock input	
Clock Rate	DC to 134 MHz in Full Channel Mode DC to 267 MHz in Half Channel Mode
Polarity	Normal or Invert
Threshold	
Range	-2.56 V to +2.54 V
Resolution	20 mV
Input Impedance	1 kΩ terminated to GND
Sensitivity	500 mV_{p-p}

Table A-69: PG module event processing

Characteristic	Description
Event Action	Advance, Jump and Inhibit
Number of Event Inputs	8 External Event Inputs (2 per each probe)
Number of Event Definitions	8 (A maximum of 256 event input patterns can be OR'd to define an event)
Event Mode	
for Advance	Edge or Level
for Jump	Edge or Level
Event Filter	None or 50 ns

Table A-70: PG module inter-module interactions

Characteristic	Description
Signal Input	Input from backplane Selectable from Signal 1, 2, 3, and 4 Used to define the Event
Signal Output	Output to backplane Selectable from Signal 1, 2, 3, and 4 Specified as High or Low in each Sequence line

Table A-71: PG module merged PG modules

Characteristic	Description
Number of modules that can be merged together	Five
External Event Input for merged module	For Jump and Advance, only the External Event Input of the leftmost module is used. For Inhibit, each module uses its own External Event Input as a source

Table A-72: PG module mechanical

Characteristic	Description
Slot width	Requires two mainframe slots
Weight (Typical)	2.5 kg (5 lbs. 4 oz.)
Overall dimensions (excluding connectors)	
Height	10.32 in (262 mm)
Width	2.39 in (61 mm)
Depth	14.7 in (373 mm)
Mainframe interlock	1.4 ECI keying is implemented

External Oscilloscope (iView) Characteristics

Table A–73 list the characteristics for iView (Integrated View) and for the Tektronix logic analyzer when connected to an external oscilloscope. For detailed information on the individual specifications of the external oscilloscope, refer to the documentation that accompanies the oscilloscope.

Table A-73: External oscilloscope (Integrated View or iView) characteristics

Characteristic	Description
Supported Tektronix logic analyzer instruments	TLA600 series, TLA714, TLA715 TLA720, TLA721
TLA application software version	V4.2 or greater
Minimum recommended TLA controller DRAM[1]	256 MB
Supported external oscilloscopes *(for the latest list of supported external oscilloscopes, visit our website at www.tektronix.com/la)*	TDS3012, TDS3014, TDS3032, TDS3034, TDS3052, TDS3054 (TDS3GM GPIB/RS232 communication module required) TDS3012B, TDS3014B, TDS3032B, TDS3034B, TDS3052B, TDS3054B TDS5052, TDS5054, TDS5104 TDS654C, TDS684C, TDS694C TDS6604 TDS724D, TDS754C, TDS754D, TDS784C, TDS784D, TDS794D TDS7054, TDS7104, TDS7154, TDS7254, TDS7404 CSA7154, CSA7404
External oscilloscope software or firmware version number	
TDS684C, TDS694C	Any version
TDS3000 series	Any version
TDS5000 series	Any version
TDS6000 series	Any version
TDS7000, CSA7000 series	Version 1.2 or greater
Maximum number of external oscilloscopes	One per Tektronix logic analyzer
iView cable length	6.56 ft (2 m)

Table A- 73: External oscilloscope (Integrated View or iView) characteristics (Cont.)

Characteristic	Description
Time correlation uncertainty[2] (*Typical at system trigger)*	
Logic analyzer triggers external oscilloscope (2 ns + logic analyzer sample period + external oscilloscope sample period)	3 ns
External oscilloscope triggers logic analyzer (4 ns + logic analyzer sample period + external oscilloscope sample period)	5 ns

[1] **If DRAM is less than 256 MB, the record length of the external oscilloscope may be limited to 1 M.**

[2] **Includes sampling uncertainty, typical jitter, slot-to-slot skew, and probe-to-probe variations to provide a *typical* number for the measurement.**

Appendix B: TLA Symbol File Format

The logic analyzer can extract range symbol information directly from object files. The following are some of the formats. Check with your Tektronix representative for a complete listing of available formats.

OMF51, OMF86, OMF166, OMF286, OMF386, IEEE695, COFF, ELF/DWARF1 and DWARF2, and ELF/STABS

Users whose code generation tools do not generate these file formats can use TLA Symbol File (TSF) format (a text format). The TSF format is used by the logic analyzer when it exports symbol files. The logic analyzer can also read files in this format.

TLA symbol files consist of alphanumeric symbol names and associated data values. The files contain a header line and lines defining the symbol names and values. Fields on a line are separated with white space (blank spaces or tabs). The formats for the pattern symbol files and the various range symbol files differ; if you need to use pattern symbols and range symbols, use separate files.

Both TLA range and pattern symbol files have a .tsf file name extension (filename.tsf).

The first few lines of a TSF symbol file are typically comment lines describing when and how the file was generated.

```
#  TLA Symbol File
#  Created on Friday, May 29, 1998 at 09:52:03
#  From file: "c:\quickstart\tla7qs.x"
```

All lines in a TSF file that begin with a number sign (#) character are treated as comments, unless the very next character is a plus sign (+). The plus sign signifies a file reader directive. (An example of a file reader directive “#+” can be seen in the TSF header definition on the next page.) The number sign character can also initiate a comment on the end of a symbol definition or other uncommented lines. All text between the number sign and the end of the line is treated as a comment and ignored.

TSF Headers

A TSF header identifies the file format version to potential file readers. It specifies whether the file contains pattern or range symbols, the radix used to specify symbol values, and an optional offset amount to be added to each symbol value (for range symbol files).

The TSF Header is a file directive, which means that the following information begins with the special character combination of a number sign character followed immediately by a plus sign (#+). This is not a comment line. The special character sequence is used to mark instructions to the file reader; these instructions are called file directives.

The following examples show sample file headers for a pattern symbol file and a range symbol file. The first two lines are comments included for readability; they are not required as part of the file header.

```
#     TSF Format     Type    Display Radix  File Radix
#  ===============  =======  =============  ==========
#+ Version 2.1.0    PATTERN       HEX           HEX

#     TSF Format    Type   Display Radix  File Radix   Offset
#  ===============  =====  =============  ==========  ========
#+ Version 2.1.0    RANGE       HEX           HEX     00000000
```

The File Format Version number contains three fields. The first two fields are the format major and minor version numbers. The logic analyzer will only read TSF files where the major and minor version number of the file is less than or equal to that of the TLA TSF symbol file reader. The third field is used to denote minor format changes, which do not impact the file reader.

The File Format Version number is followed by a key word, PATTERN or RANGE, which signifies the type of symbols to be found in the file. TSF files can contain either type of symbols, but no single file can contain both. The header specifies the type for all symbols in the file.

The Display Radix field sets the default radix that will be used to display the numeric symbol value. For range symbol files this field must be one of the key words: HEX, DEC, OCT, or BIN. For pattern symbol files, only the key words: HEX, OCT, or BIN are allowed.

The File Radix field specifies the radix used by the symbol values in this file. Like the Display Radix field, the File Radix field must be one of the key words: HEX, DEC, OCT, or BIN for range symbol files, or HEX, OCT, or BIN for pattern symbol files.

The Offset field specifies an offset value and is applicable only to range symbol files. The offset value is specified in the radix indicated by the File Radix field. This offset value will be added to the lower and upper bounds of each range symbol that is read from the file. The offset is a 32-bit value, so it can have any value between 0x00000000 and 0xFFFFFFFF. If the sum of the offset and a range symbol bound value exceeds the 32-bit limit of 0xFFFFFFFF, the overflow bit is discarded. Negative offsets are specified by using a twos complement value for the offset.

TSF Pattern Symbols

Each pattern symbol in a TSF pattern file consists of two fields. The first field is the symbol name, and the second is the symbol pattern. The symbol name is a sequence of ASCII characters of up to 220 characters in length, although it is impractical to display symbol values much longer than 32 characters. Symbol names longer than 220 characters will be truncated during loading. The characters in a symbol name can be any character with an ASCII value between 0x21 (the exclamation point character, !) and 0x7E (the tilde character, ~). You can use symbol names with embedded spaces by enclosing the Symbol Name in double quotes.

```
# Symbol     Symbol     Optional Foreground
# Name       Pattern    and Background Color
# ======     ========   ====================
  NUL        XOOOOOOO
  SOH        XOOOOOO1   @red   @yellow
  STX        XOOOOO1O
 "ETX 0x03"  XOOOOO11
```

The symbol pattern consists of numerals in the radix specified by the File Radix field in the header, and Xs signifying “don’t-care” values. The number of bits represented by each character position in the pattern depends on the selected radix. For a radix of HEX, each character represents 4 bits. For an OCT radix, each character represents 3 bits; for a BIN radix, each character represents one bit.

Symbol order in a TSF pattern file is important. When selecting the symbol to display for a particular value, the logic analyzer scans the list of pattern symbols from top to bottom. It selects the first symbol for which all non-don’t-care bits of the symbol match the corresponding bits of the target symbol.

TSF Range Symbols

There are four different types of range symbols:

- Function
- Variable
- Source
- Color

Each of these types define a range of 32-bit addresses associated with some entity.

Function range symbols define the beginning and ending addresses where instructions that implement a function are located in memory.

Variable range symbols define the beginning and ending addresses where the value of a variable is located in memory.

Source range symbols are similar to function range symbols, except that the address range for a source symbol describes the location of the instructions that implement just one source statement. (Source symbols also contain file name, line number, and an optional column range that define the location of the source code associated with the symbol.)

Color range symbols define a display color for any value that falls within a range.

Each of the types of range symbols appear in a separate section of the file. Each section begins with a file directive indicating the type of symbols that follow. The sections may appear in any order, and can be broken up and separated by other sections if necessary.

The first section might be variables, followed by functions, then followed by another variable section. Each section is also optional, however some logic analyzer applications are unable to use the symbol file if the appropriate type of symbols are not present. For example, the source window is only able to correlate with a listing window if the symbol file contains source symbols.

Range symbol names follow the same rules as pattern symbol names. The symbol name is a sequence of ASCII characters of up to 220 characters in length, even though it is impractical to display symbol values much longer than 32 characters.

Symbol names longer than 220 characters will be truncated during loading. The characters in a symbol name can be any character with an ASCII value between 0x21 (the exclamation point character, !) and 0x7E (the tilde character, ~). You can use symbol names with embedded spaces by enclosing the Symbol Name in double quotes.

Range symbol address ranges can overlap. This overlap sometimes produces unexpected results. When overlaps occur, and the logic analyzer needs to convert a numeric value to a symbol, it must choose between the overlapping symbols. When choosing between overlapping symbols, the logic analyzer assigns a precedence order to the symbol types. Function symbols have the highest precedence, followed by variable symbols, and then source symbols.

TSF Function Symbols

The file directive "#+ Function" introduces the function symbol section of a TSF Range file. The file directive tells the file reader that the following symbols represent functions, as opposed to variables or source statements. If no symbol type file directive is given, the function symbol type is assumed.

```
#+ Function
#          Symbol Name              Low      High
# ============================== ======== ========
displayBanner                    006035ba 00603675
buildMenus                       00603676 006036e5
displayLCDmenu                   006036e6 0060372f
```

Function symbols consist of three fields: the symbol name, the lower bound, and the upper bound.

The lower and upper bound values are each 32-bit values, defined by numerals in the radix specified by the File Radix field in the file header. These values define the lower and upper limits of the range of addresses occupied by the instructions which implement a function. Both values are inclusive, which means that the specified range includes both of the bound values, as well as all of the addresses between them.

TSF Variable Symbols

The file directive "#+ Variable" introduces the variable symbol section of a TSF Range file. The file directive tells the file reader that the following symbols represent variables, as opposed to functions or source statements. If no symbol type file directive is given, the function symbol type is assumed.

```
#+ Variable
#          Symbol Name              Low      High
# ============================== ======== ========
menu                             00000100 00000102
userMenu1                        000004c0 000004c2
binBits                          000004d4 000004d6
```

Variable symbols consist of three fields: the symbol name, the lower bound, and the upper bound. Variable symbols are just like function symbols except that they define the address range occupied by a variable, instead of function. The lower and upper bound values of a variable symbol are inclusive, meaning that they are themselves a part of the range. For variables occupying only a single byte in memory, the lower and upper bound values are equal.

TSF Source Symbols

The file directive "#+ Source" introduces the source symbol section of a TSF range file. The file directive tells the file reader that the following symbols represent source statements, as opposed to functions or variables. The source file directive must be followed by a file name, which specifies the name of the source file containing the following source statements. Each new set of symbols for a unique source file must be introduced with an additional source file directive to specify the file name for those symbols. If no symbol type file directive is given, the function symbol type is assumed.

```
#+ Source stoplite
# Line   Low      High   Beg End  Symbol Name
# ==== ======== ======== === ===  ===========
    27 006043ec 006043ef   0  25  # stoplite_27_25
    35 006043f0 006043f5   0  23  # stoplite_35_23
    47 006043f6 006043ff   0  30  # stoplite_47_30
    48 00604400 00604409   0  30  # stoplite_48_30
    49 0060440a 00604413   0  30  # stoplite_49_30
    50 00604414 0060441d   0  30  # stoplite_50_30
    51 0060441e 00604427   0  30  # stoplite_51_30
    52 00604428 00604431   0  30  # stoplite_52_30
    56 00604432 00604437   0  17  # stoplite_56_17
    59 00604438 00604439   0  18  # stoplite_59_18
    60 0060443a 00604445   0  37  # stoplite_60_37
    61 00604446 0060444d   0  33  # stoplite_61_33
    59 0060444e 0060444f  35  39  # stoplite_59_35
    59 00604450 00604455  19  34  # stoplite_59_19
    71 00604456 00604457   0  37  # stoplite_71_37
    74 00604458 0060445f   0  35  # stoplite_74_35
    77 00604460 00604467   0  36  # stoplite_77_36
    80 00604468 0060446f   0  36  # stoplite_80_36
    83 00604470 0060447b   0  43  # stoplite_83_43
    87 0060447c 00604483   0  34  # stoplite_87_34
    71 00604484 0060448d   0  37  # stoplite_71_37
    84 0060448e 00604490   0  29  # stoplite_84_29
```

The source symbols section consists of five fields for each source statement: line number, lower address bound, upper address bound, beginning column value, and ending column value.

Source symbols do not have a name in the same sense as function or variable symbols, because there is no name associated with each of the executable statements in a source file. Instead, a source symbol has a file name, specified in the source directive, and a line number. The line number specifies the line of the source file that contains the source statement. Line numbers are always in decimal regardless of the file radix in the header.

The lower and upper bound values for a source symbol are similar to those of function and variable symbols. For source symbols, these bounds represent the range of addresses occupied by the instructions that implement a single source statement.

The bound values are defined in the file radix specified in the header and can range in value from 0x00000000 to 0xFFFFFFFF. The lower and upper bound addresses are inclusive, just like other symbols. A source symbol for an instruction occupying a single memory location has matching lower and upper bound values.

The beginning and ending column fields of a source statement are optional. When present, and non-zero, they define the beginning and ending column position for the source statement.

The beginning and ending column values define the location of the statement in the line. This is especially useful when there are multiple statements on a single line, because it makes it possible to define a separate symbol for each statement. When the column information is not present, or is set to zero, the symbol is assumed to correspond to the entire line.

Only a few compilers generate column information, but when the information is present in the symbol file, the logic analyzer uses the column information to provide highly accurate source code correlation. The example source symbols on the previous page show typical column values.

In most cases only one of the column values is non-zero. This is because those lines contain only one statement, and the compiler specified only the column at which the statement ended. Some compilers specify only the beginning column position for such lines, in which case the beginning value would be non-zero and the ending value zero.

Note that there are three symbols corresponding to line 59 of the file. Line 59 of the original source file contains the following statement:

for (i = 0; i < NUM_STATES; i++)

This one line contains three separate statements. The first statement is the initialization (i = 0), the second statement is the test (i < NUM_STATES), and the third statement is the increment (i++).

Although all three statements appear on the same line, each generates a separate set of instructions, and the symbols in the example define unique address ranges for each. This enables the Source window to accurately indicate which of the three statements on the line is associated with any given address.

Each of the source symbols in the example includes a comment at the end of the line showing a symbol name. Since this is a comment, it is ignored by the symbol file reader, and is optional. When symbol files are exported by the logic analyzer, they contain comments that show the derived symbol name created by the logic analyzer itself. The name is a concatenation of the symbol file name, line number, and column number (if present). This is the symbol value that the logic analyzer will display for addresses that fall within the lower and upper bounds of a source symbol.

TSF Color Symbols

Color range symbols define the beginning and ending group values where a color is displayed. Any group value in the acquisition falling within this range will be shown in the defined color. The value range of a color symbol can overlap with the set of ranges defined by one or more Function, Variable, or Source symbols. In many instances a Color symbol will use exactly the same range bounds as a Function or Variable symbol.

A partial range file with colors is shown below:

```
#+ Color
#          Color                      Low      High
# ============================== ======== ========
@magenta                         006035ba 00603640
@yellow @navy                    00603541 00603675
@default @green                  006036e6 0060372f
```

The first line tells the file reader that the following symbols represent colors. The next two lines are comments used as headers. The first color name specifies the foreground color, and the second optional color name specifies the background color. The available color names (keywords) are:

> @black, @blue, @cyan, @lime, @magenta, @red, @yellow, @white, @navy, @teal, @green, @purple, @maroon, @olive, @gray, and @silver.

The special color name @default gives the default text coloring specified by choosing a color in the Column tab of the Listing Window Property Sheet or the Waveform tab of the Waveform Window Property Sheet.

The Low and High columns describe the lower and upper bounds. The bounds are expressed as 32-bit values; the radix is specified in the header. The bounds are inclusive; the specified range includes both bound values, as well as all values between the bounds.

There is a different TSF symbol file syntax for adding color to range and pattern symbol files. For pattern symbol files, color is an attribute of existing pattern symbols. It is placed on the same line as the rest of the symbol, and to the right of the pattern definition. For range symbol files, color symbols are added in a separate section of the symbol file, just like Function, Variable, and Source

symbols. This allows the color information to be independent of the other defined range symbols.

A partial TSF Pattern Symbols file is shown below:

```
#  Symbol Name      Pattern    Color
# ==============   =========   ============
NUL                XOOO OOOO
SOH                XOOO OOO1   @blue
STX                XOOO OO1O   @white @red
SBZ                XOOO O1OO   @default @teal
```

Each Pattern symbol in a TSF Pattern file consists of three fields. The first field is the Symbol Name, the second is the Symbol Pattern, and the third is Symbol Color.

The Symbol Color specification may contain zero, one, or two color keywords. If only one color is given, it specifies the foreground color of the data. If two colors are given, they specify the foreground color followed by the background color.

To supply a background color, you must give a foreground color. If you want to use the group's defined color from the Column or Waveform Property Page, you can use @default as the foreground color.

Appendix C: Pattern Generator Physical-Logical Conversion

The logic analyzer and DSO modules handle signals 1, 2, 3, and 4 with a logical expression (True/False). However, the pattern generator module handles these signals with a physical expression (High/Low). Select whether to use the signals as AND or OR from the TLA application's Signals property page of the System Configuration window. Use Tables C–1 and C–2 to convert physical expressions to logical expressions or vice versa.

Table C-1: For Signal 1, 2, and 3, 4, (logical function AND)

LA/DSO expression	Logical true	Logical false
Pattern generator signal output	High	Low
Pattern generator event definition	1	0

Table C-2: For Signal 3, 4 (logical function OR)

LA/DSO expression	Logical true	Logical false
Pattern generator signal output	Low	High
Pattern generator event definition	0	1

Only one module in the system can drive Signal 1. Only one module in the system can drive signal 2. When used with an expansion mainframe, all modules that drive Signal 3 should be in the same mainframe, and all modules that drive Signal 4 should be in the same mainframe.

Appendix D: TLA700 Module Installation

This section describes the steps to install modules in your TLA700 Series Logic Analyzer for the first time. It is written from the perspective that you purchased most of the items uninstalled and you intend to install all of the different items.

CAUTION. *To avoid damaging the instrument, do not install or remove any modules while the instrument is powered on.*

Always power down the instrument before removing or inserting modules.

Setting the Logical Address

Every module in the instrument must have a unique logical address; no two modules can have the same address. Two rotary switches on the rear panel select the logical address. Although Figure D–1 shows an LA module, the address switches are identical for all TLA modules. Read the following descriptions before changing the logical address.

NOTE*. Do not set any module to logical address 00. Logical address 00 is reserved exclusively for the controller.*

Dynamic Logical Address Auto Configuration

The factory default switch setting is FF (Dynamic Auto Configuration). With dynamic logical address auto configuration selected, the instrument automatically sets the address to an unused value. For example, if there are modules set to addresses 01 and 02 already in your system, the resource manager will automatically assign the module an address other than 01 or 02. This allows you to freely move the modules around without reconfiguring the logical address.

Static Logical Address

Static logical address selections set the address to a fixed static logical address value. You can select any static addresses between 01 and FE hexadecimal (1 to 254 decimal). If you set the logical address switches to any other setting than FF, you must verify that no two modules (or devices) share the same address.

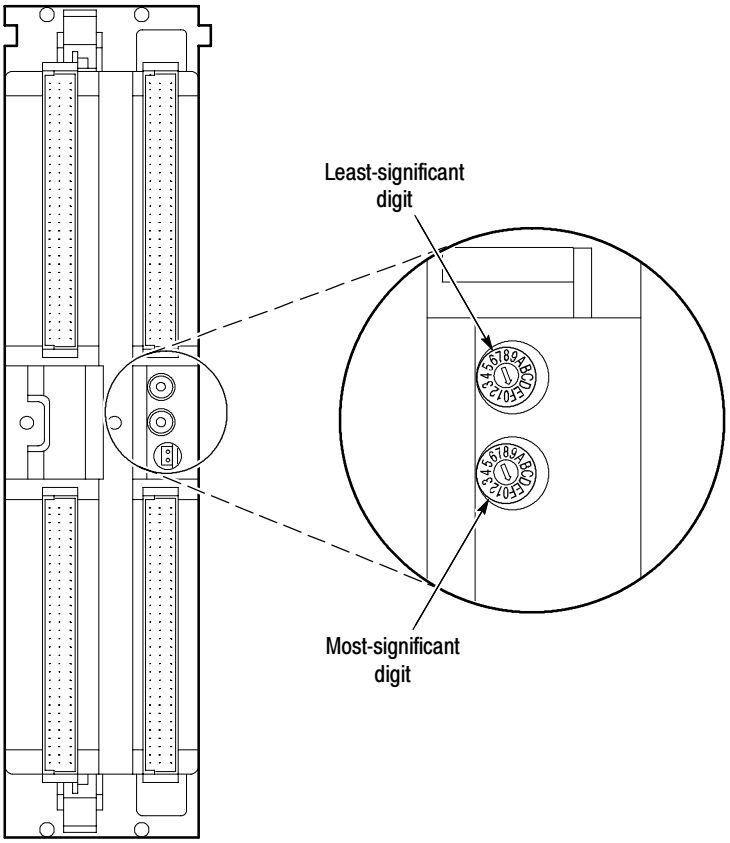


Figure D-1: Logical address switches

Module Address Problems

All modules are shipped with the logical address switch set to FF. This includes the the enhanced monitor board (located in the benchtop mainframe), which also requires a unique logical address.

If two modules (including the fan controller board) are set to the same address, the system will not work properly. The most common symptom of conflicting logical addresses is that a module will not show up in the system window.

Merging Modules

You can merge individual logic analyzer and pattern generator modules to create wider modules. Logic analyzer modules must be physically merged together by a merge cable and through software. Refer to *Appendix E: Merging Modules* for more information on merging modules.

Installing Modules in the Portable Mainframe

You can install any of the modules in any slot that the module key will allow; see Figure D–3. If you intend to merge the modules, disregard the following suggestions and refer to the merging modules rules on page E–1. If you are not merging the modules, and for air flow considerations, you should follow these guidelines:

- If a single LA module is to be installed, install it in slots 3–4. Place a double width slot cover over slots 1–2.
- Install TLA7Lx/Mx/Nx/Px/Qx modules, DSO modules, or pattern generator modules before you install TLA7Axx modules.
- If an LA module is to be installed with a DSO module, install the DSO module in slots 1–2, and the LA module in slots 3–4.
- If two LA modules are to be installed, install the module with the highest channel count in slots 1–2. Install the module with the lower channel count in slots 3–4.
- If two LA modules are to be installed, install the module with the largest memory in slots 3–4. Install the module with the lower memory in slots 1–2.

Use a screwdriver to tighten the retaining screws to 2.5 in-lbs after seating the modules in place. See Figure D–2.

Installing Modules in the Benchtop or Expansion Mainframes

You must install the benchtop controller in the benchtop mainframe in slots 0–2 (the TLA7XM Expansion Module must be located in slot 0). You can install any of the modules in any slot that the module key will allow; see Figure D–3.

If you intend to merge the modules, disregard the following suggestions and refer to the merging modules rules on page E–1. If you are not merging the modules, and for air flow considerations, you should follow these guidelines:

- If a single LA module is to be installed, install it in slots 3–4. Place a double width slot cover over slots 5–6, 7–8, 9–10 and 11–12.
- If an LA module is to be installed with a DSO module, install the LA module in slots 3–4, and the DSO module in slots 5–6. Place double width slot covers over slots 7–8, 9–10 and 11–12.
- Install TLA7Lx/Mx/Nx/Px/Qx modules, DSO modules, or pattern generator modules before you install TLA7Axx modules.

- If two or more LA modules are to be installed, install the module with the highest channel count in slots 3–4. Install the module with the lower channel count in slots 5–6. Place double width slot covers over slots 7–8, 9–10 and 11–12.
- If two or more LA modules are to be installed, install the module with the largest memory in slots 3–4. Install the module with the lower memory in slots 5–6. Place double width slot covers over slots 7–8, 9–10 and 11–12.

Use a screwdriver to tighten the retaining screws to 2.5 in-lbs after seating the modules in place. See Figure D–2.

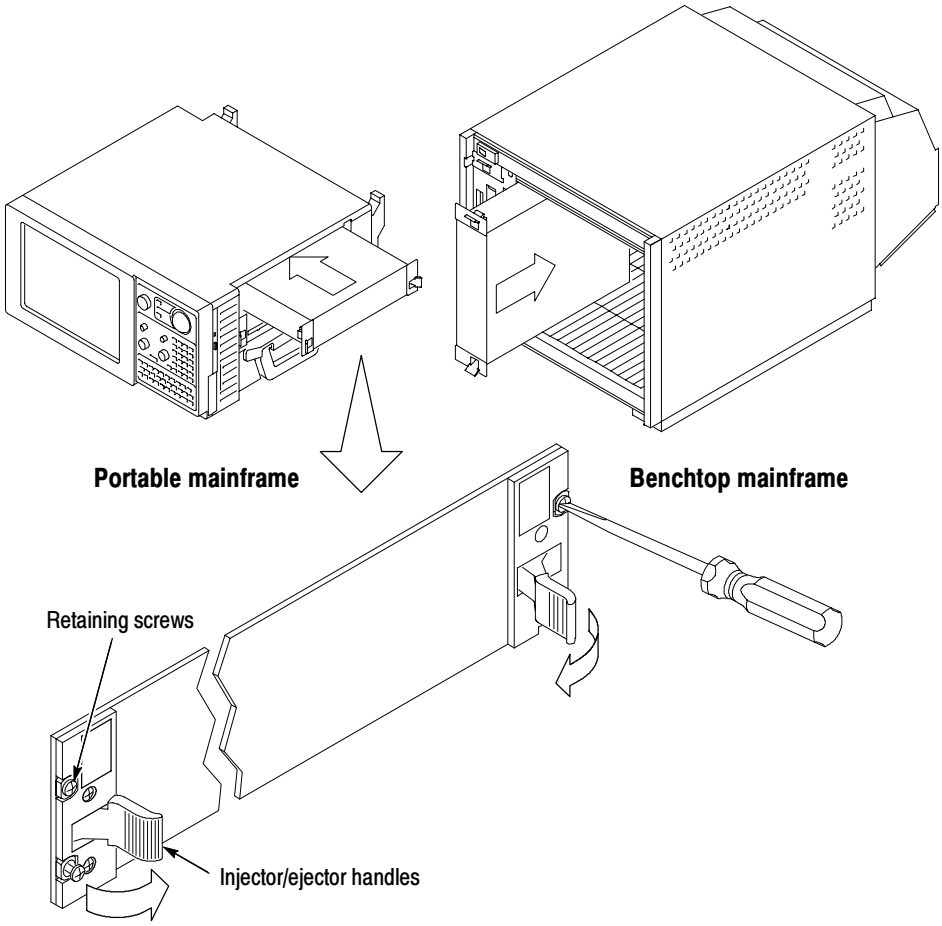


Figure D-2: Installing modules

Module Keying

Each module has a key that only allows certain modules to be installed next to other modules. For example, you can install a TLA7Dx DSO module to the left of a TLA7XM Expansion module, but you can not install a TLA7Nx LA module to the immediate left of a TLA7XM Expansion module. See Figure D–3.

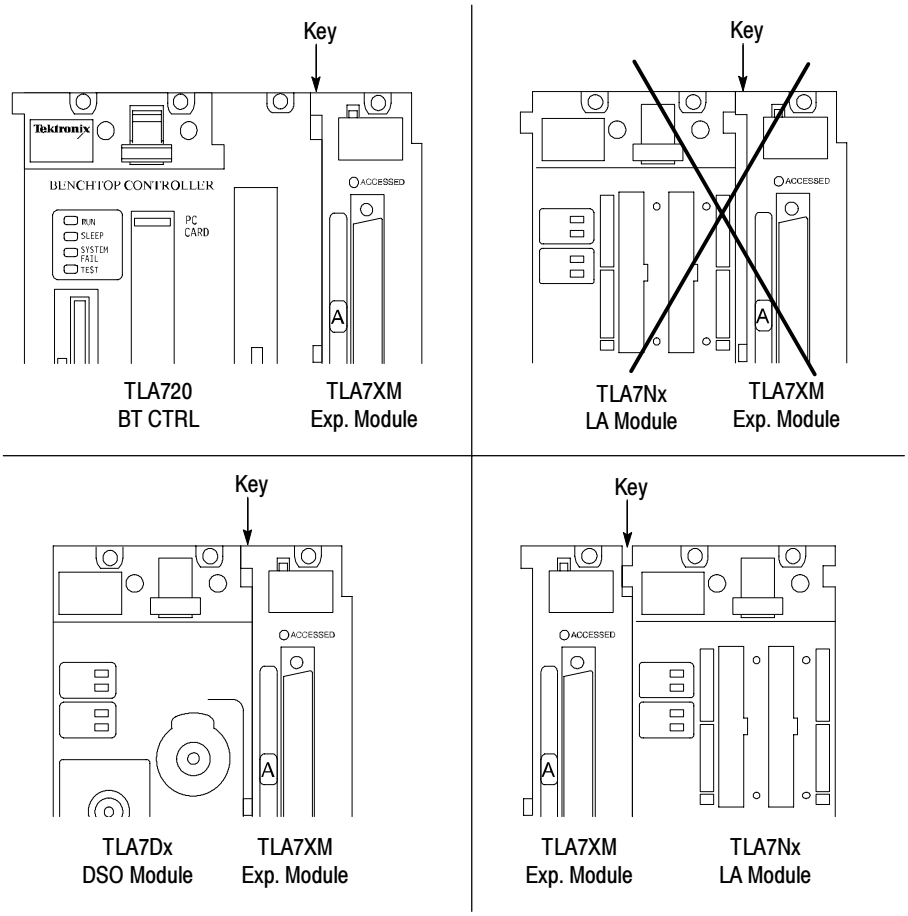


Figure D-3: Module keying

Covering Empty Slots

If you have any unused (empty) slots in your mainframe, you must install blank slot panel covers to meet EMC specifications. Install a blank slot panel cover for each empty slot as shown in Figure D–4 or D–5.

Make sure that the EMI shielding is in contact with the adjacent panel or module cover, and that the airflow shutter activation arms protrude through the holes in the blank shield.

CAUTION. *Use only Tektronix TLA slot panel covers on the benchtop mainframe. Otherwise, the mainframe may not meet cooling and EMC requirements.*

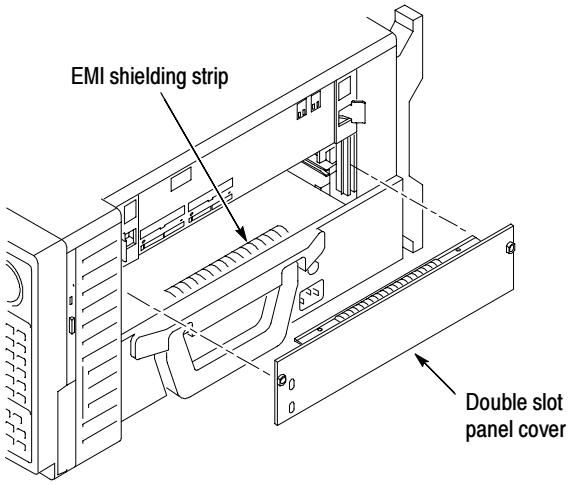


Figure D-4: Installing panel covers on the portable mainframe

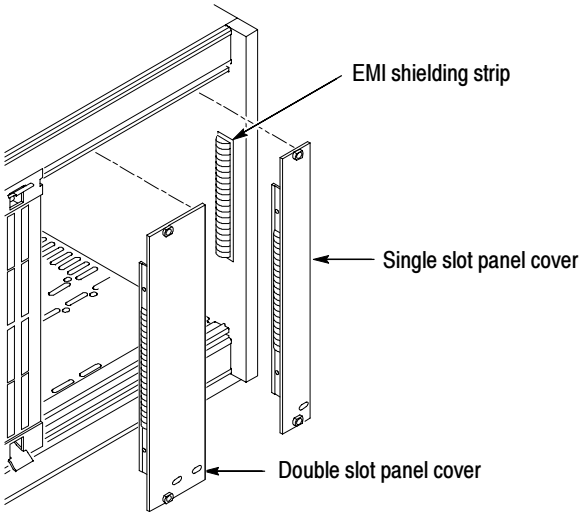


Figure D-5: Installing panel covers on the benchtop mainframes

Appendix E: Merging Modules

This appendix describes how to merge TLA700 series logic analyzer and pattern generator modules to form wider modules.

A merged logic analyzer module set consists of a master logic analyzer module and up to four slave logic analyzer modules that are physically connected together by a merge cable and are merged in software. Review the guidelines under *Logic Analyzer Module Merging Rules* and then follow the steps to physically connect the modules together before installing the modules in the mainframe.

A merged pattern generator module set consists of a master pattern generator module and up to four slave pattern generator modules merged in software. Review the guidelines under *Pattern Generator Module Merging Rules* on page E–3 before installing the modules in the mainframe.

Logic Analyzer Module Merging Rules

The following logic analyzer module merging rules must be followed:

- Only modules with 102 channels or more can be merged.
- Logic analyzer modules must be in adjacent slots and physically connected.
- Logic analyzer modules cannot be merged across mainframes (between the benchtop mainframe and one or more expansion mainframes), because the modules must be physically adjacent and physically connected.
- Logic analyzer modules with unequal synchronous clock rates cannot be merged.
- Merging logic analyzer modules with unequal memory depths will result in the merged modules assuming the depth of the shallowest module.
- When merging logic analyzer modules of unequal channel widths, use the logic analyzer module with the higher number of channels as the master module. If there is a second slave module, the first slave must have greater than or equal the number of channels as the second slave module. Slave 3 cannot have more channels than the master, slave 1 or slave 2. Slave 4 cannot have more channels than the master, slave 1, slave 2, or slave 3.
- The logic analyzer modules must have the same firmware version.
- The maximum merged combinations are two TLA7Lx and TLA7Mx logic analyzer modules; three TLA7Nx, TLA7Px, or TLA7Qx logic analyzer modules; and five TLA7Axx logic analyzer modules.

- TLA7Nx, TLA7Px, and TLA7Qx Logic analyzer modules cannot be merged with TLA7Lx and TLA7Mx Logic analyzer modules (even if they are connected together).
- TLA7Axx modules cannot be merged with TLA7Nx, TLA7Px, TLA7Qx, TLA7Lx or TLA7Mx modules.
- To merge a logic analyzer module to an established merged set, the established merged set must first be unmerged through software. Unmerged modules are the only potential candidates to add to a merged configuration.

Merge Procedure

Complete the following steps to create a merged module from two or more individual modules. You must complete these steps prior to installing the modules in a mainframe.

CAUTION. *To avoid damaging the mainframe or any modules, always power off the mainframe before removing or installing modules.*

1. Determine which modules will reside in the higher-numbered slots in a single mainframe.
2. Place the merge connector of these modules in the extended position. The module in the lowest-numbered slot must have the merge connector in the recessed position.

   Use Figure E–1 as a guide for determining the location of the master module with the merged module set. Even though Figure E–1 shows a five module set, you can still use the illustration to position the master module with respect to the slave module. For example, if you have a two module set, the master module is located in the lower-numbered slot, and the slave module is in the higher-numbered slot.

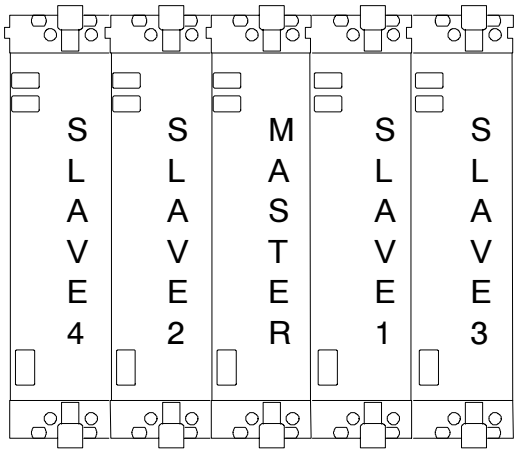


Figure E- 1: Location of modules in a merged system

Pattern Generator Module Merging Rules

The following pattern generator module merging rules must be followed:

- Pattern generator modules are merged through software.
- Pattern generator modules must be physically adjacent.
- Pattern generator modules may not be merged across mainframes.
- Merging pattern generator modules with unequal memory depths will result in the merged set assuming the depth of the shallowest pattern generator module.
- Pattern generator modules must have the same firmware version.
- When merged, the left-most pattern generator module is the master.

TLA7Axx Logic Analyzer Merge Procedures

Complete the following steps to create a merged module from two to five individual TLA7Axx modules.

1. Place the module on the right side.
2. Using a Torx T-10 screw driver, remove the two screws holding the merge connector to the module (see Figure E–2).

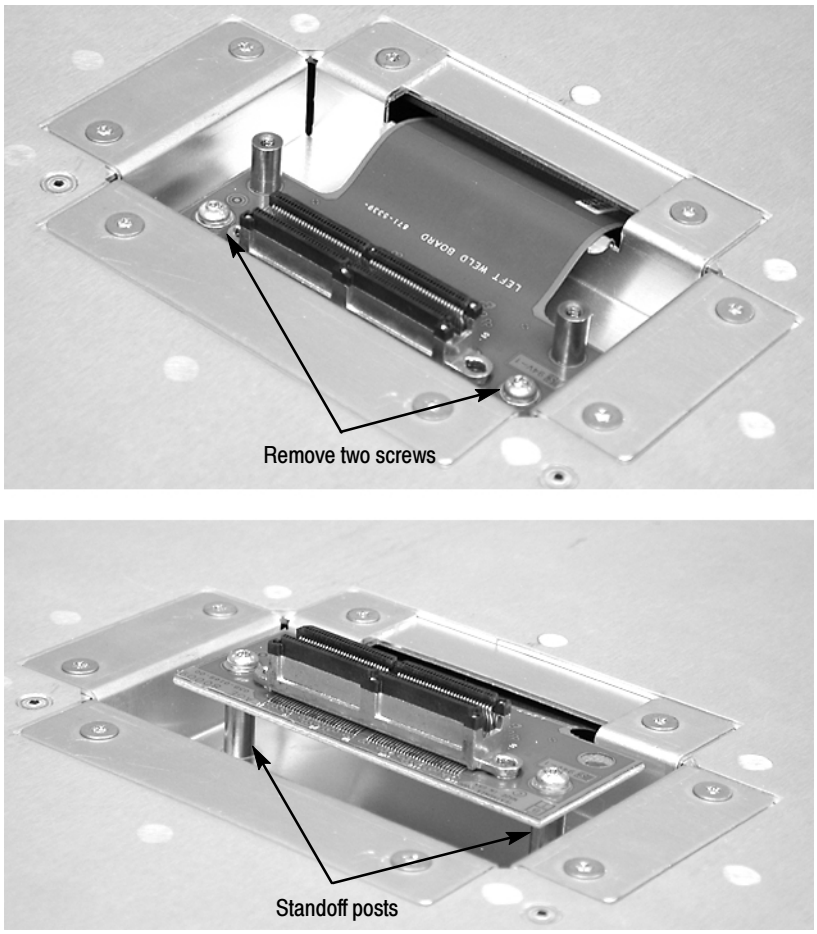


Figure E-2: Removing the merge connector assembly from the module

3. Gently lift the merge connector out of the slot and place it in the extended position such that the screw holes line up over the two standoff posts.
4. Install the two screws into the standoff posts. Tighten the screws to 4-in. lbs.
5. Repeat steps 1 through 4 for the remaining modules.

***NOTE**. When installing the merged modules into a mainframe, you may need the help of another individual.*

6. Place the first pair of modules to be merged side-by-side such that the merge connector assemblies line up and connect between the two modules (see Figure E–3).
7. Push the two modules together until the connectors are seated in place.

8. Add any additional modules to the set.

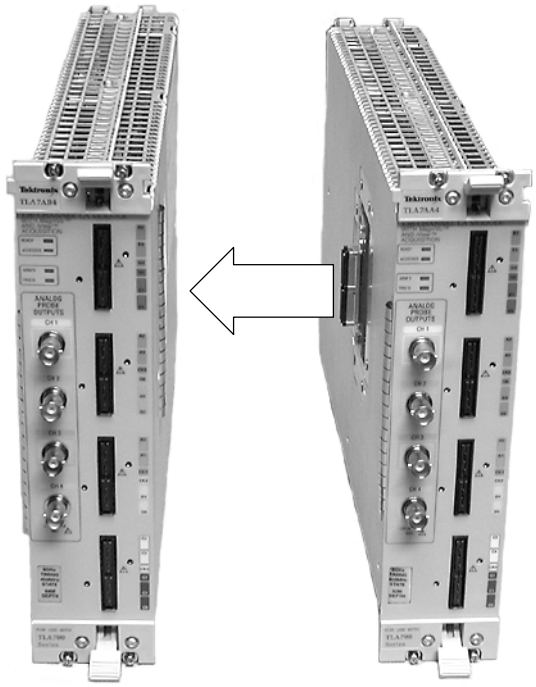


Figure E-3: Connecting modules in a merged set

CAUTION. *Ensure that the mainframe is powered-off before installing or removing the modules.*

9. Place the merged module set into the mainframe.

10. Align the tops and bottoms of the modules with the slots in the mainframe (see Figure E-4 on page E-6). You may need the help of another individual if your merged module set contains more than two modules.

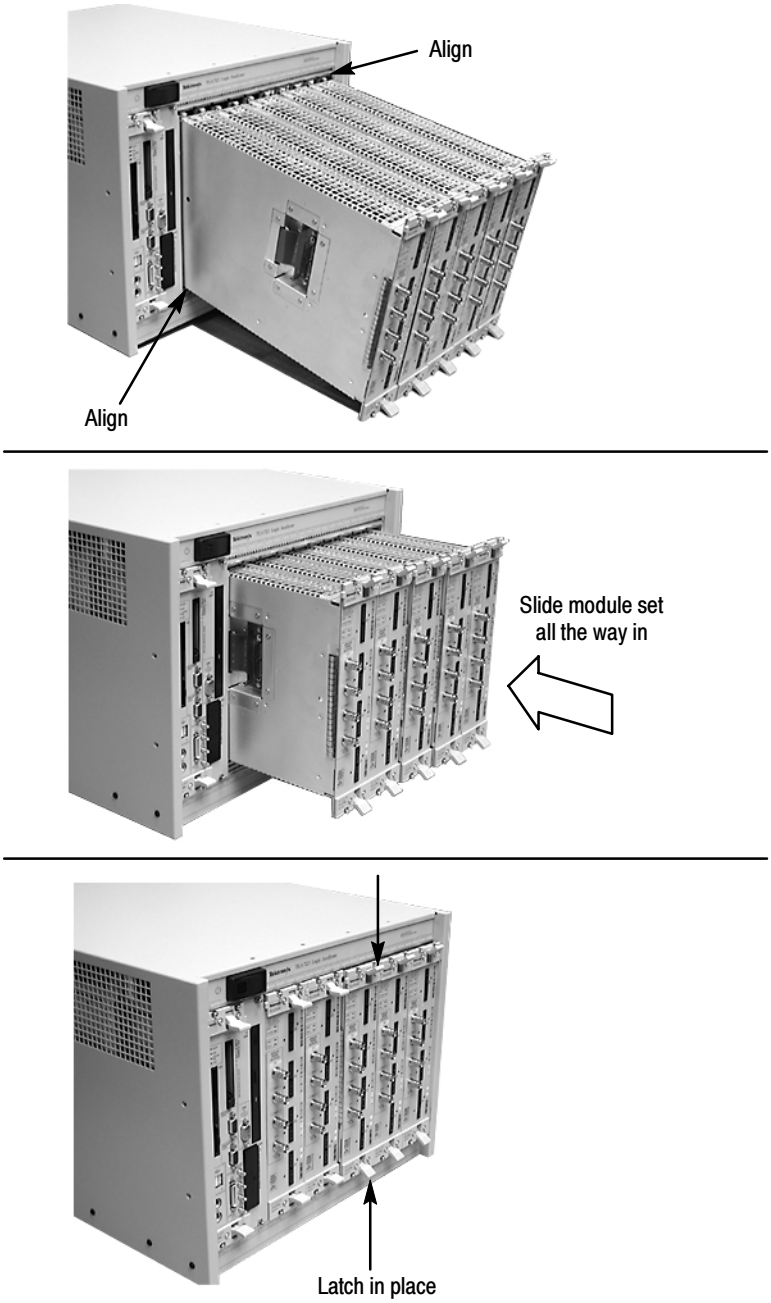


Figure E-4: Installing the merged module set in the mainframe

11. Slide the modules all the way into the mainframe until they rest against the rear panel connectors.

12. Use the injector handles to firmly seat the modules in place one at a time. The merge cable assembly should allow enough play between two side-by-side modules.

13. After installing all of the modules, power on the mainframe and complete the merge process listed under the Merged Modules tab in the System Configuration dialog box.

Unmerge Procedure

Although you can unmerge modules from a merged set from within the TLA application without physically separating modules, there will be times when you have to physically unmerge the modules. The following procedures provide the steps for unmerging the modules.

1. Power off the mainframe before removing the modules from the mainframe.

2. Use the ejector handles to disengage each module in the merged module set from the mainframe.

3. With the assistance of another individual, slide all of the merged modules out of the mainframe and place them on a static-free working surface.

4. Gently separate the modules one at a time from the merged module set.

5. Lay the modules on their right sides.

6. Remove the two Torx T-10 screws that hold the merge cable assembly to the module.

7. Place the merge cable assembly into the recessed position.

8. Install the two Torx T-10 screws onto the assembly and tighten the screws to 4 in-lbs.

9. Repeat steps 6 through 8 for the other modules.

You can now reinstall the modules in the mainframe as needed.

TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, and TLA7Qx Logic Analyzer Merge Procedures

Use the following procedures to physically merge the logic analyzer modules together.

Two-Way Logic Analyzer Merge Procedure

The following procedure is used for merging two logic analyzer modules to form a merged set with a higher logic analyzer channel count. For information on merging three modules, see page E–13.

CAUTION. *Static discharge can damage any semiconductor component in the logic analyzer module.*

Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while performing the merge procedure.

Perform the following steps to merge two modules:

1. Power off the mainframe.
2. Determine which module will be designated as the slave module and which module will be the master module.
3. Lay the slave module on the right side (as viewed from the front panel).
4. Remove the screws from the module cover with a screwdriver with a T-10 Torx tip; refer to Figure E–5 on page E–9.
5. Remove the screws near the front of the module.
6. Remove the screws holding the merge cable bracket to the cover.
7. Remove the top part of the cable bracket and set it aside.
8. Remove the module cover and locate the merge cable.

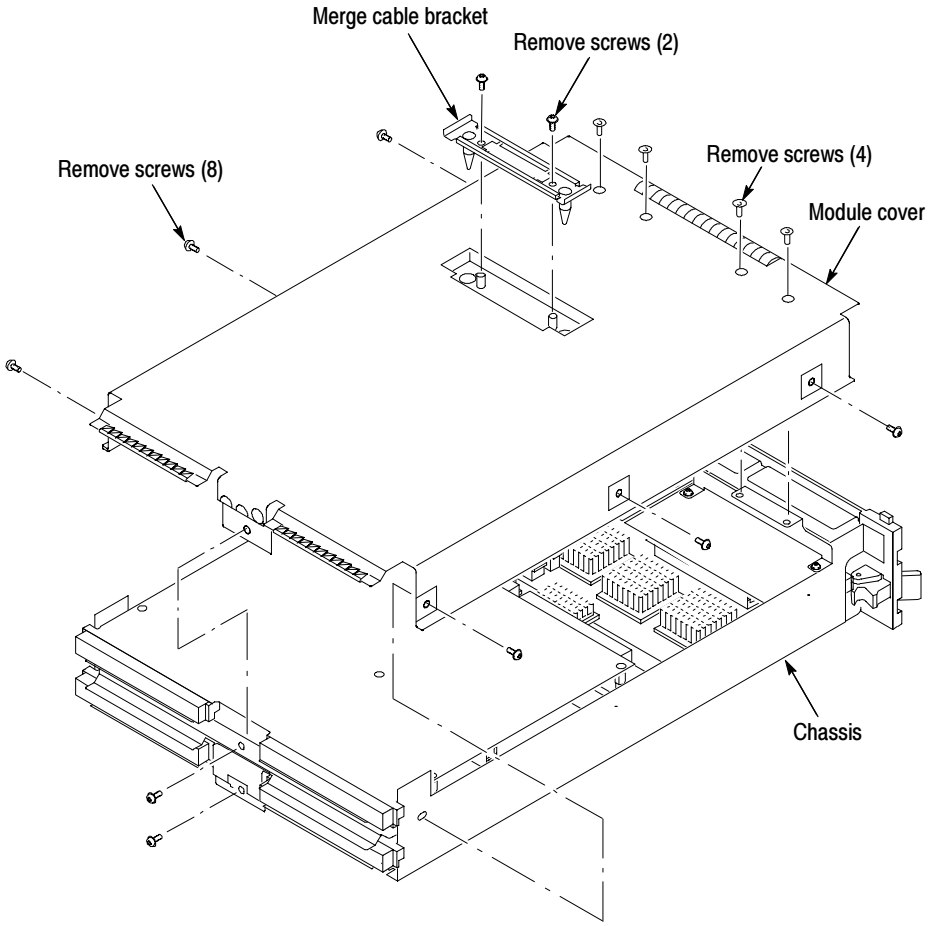


Figure E- 5: Removing the cover

9. Replace the cover while feeding the merge cable through the hole in the cover (see Figure E–6).

NOTE*. Do not twist the cable while feeding it through the hole. If the cable is twisted, the modules will not mate correctly.*

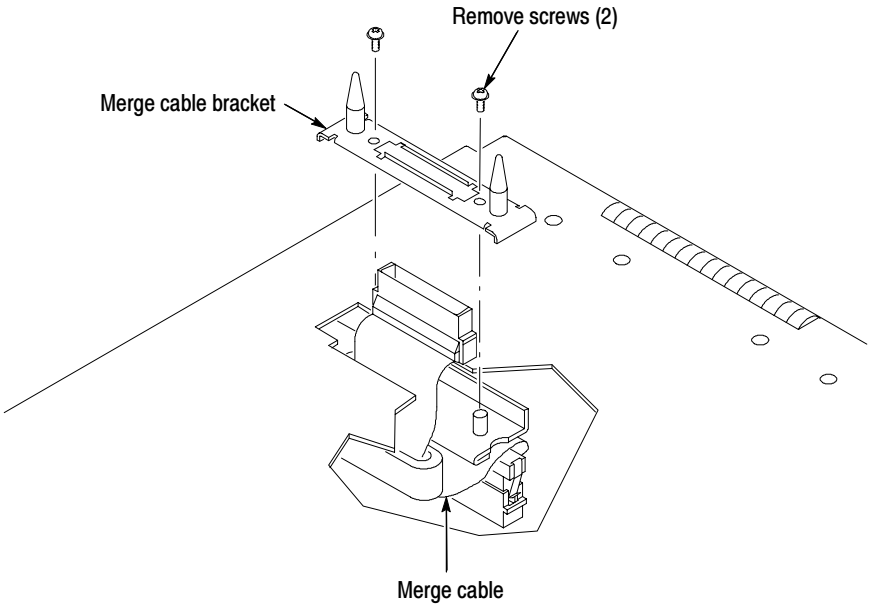


Figure E-6: Feeding the merge cable through the cover

10. Turn the merge cable bracket over so that the guide pins point up.

11. Place the bracket over the merge cable connector.

12. Install the two screws that hold the merge cable bracket in place.

CAUTION. *To prevent damage to the module during the installation process, reinstall the cover exactly as described in steps 14 through 19.*

If the cover is not properly seated, the module can be damaged when you install it in the mainframe and it will not meet EMC requirements.

13. Replace the logic analyzer module cover.

14. Push forward on the cover so the tab on the front edge of the cover inserts into the rear of the front subpanel. Make sure that the cover is fully seated (no gaps) against the front and rear chassis flanges.

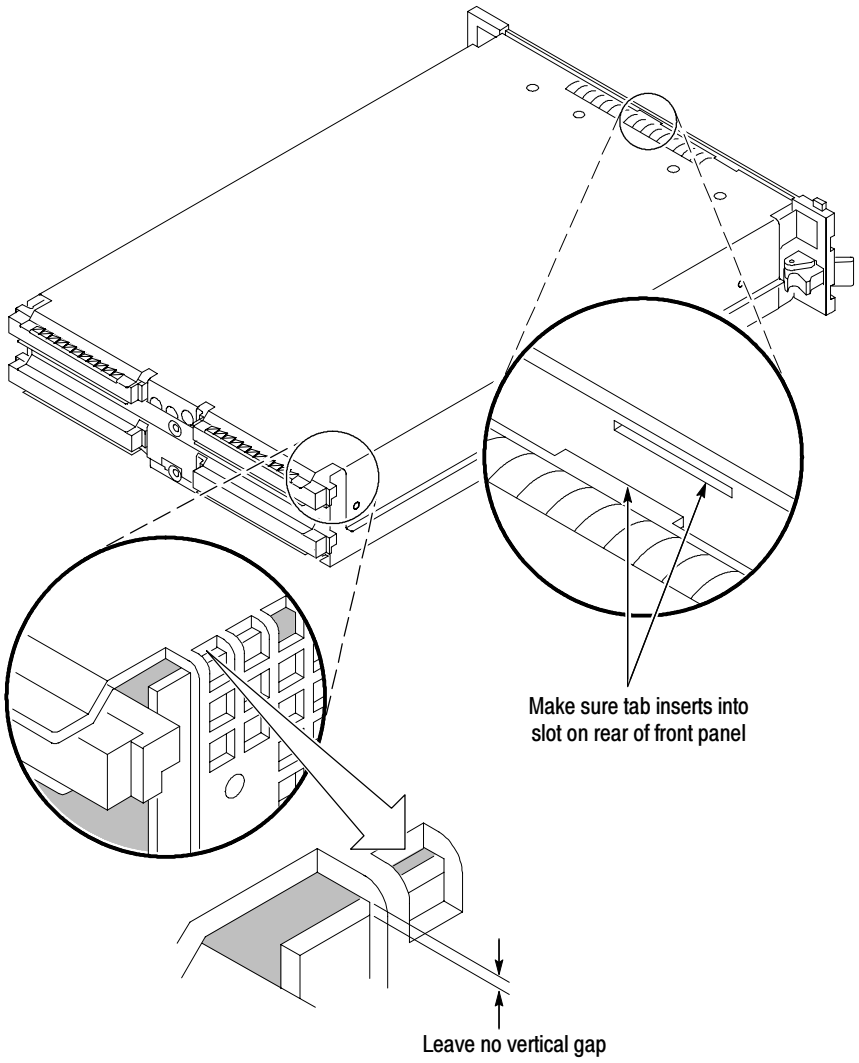


Figure E- 7: Seating the cover on the chassis

15. While holding the cover in place, install the screws nearest the front of the module (two on the top and two on the bottom) to secure the cover to the chassis.

16. Install the screws near the front of the module.

17. Slide the rear panel on the chassis and install the rear panel screws.

18. Install the top and bottom rear screws.

19. Check and tighten all screws.

20. Place the master module adjacent to the slave module so that the two guide pins from the Slave module line up with the guide pin holes in the master module.

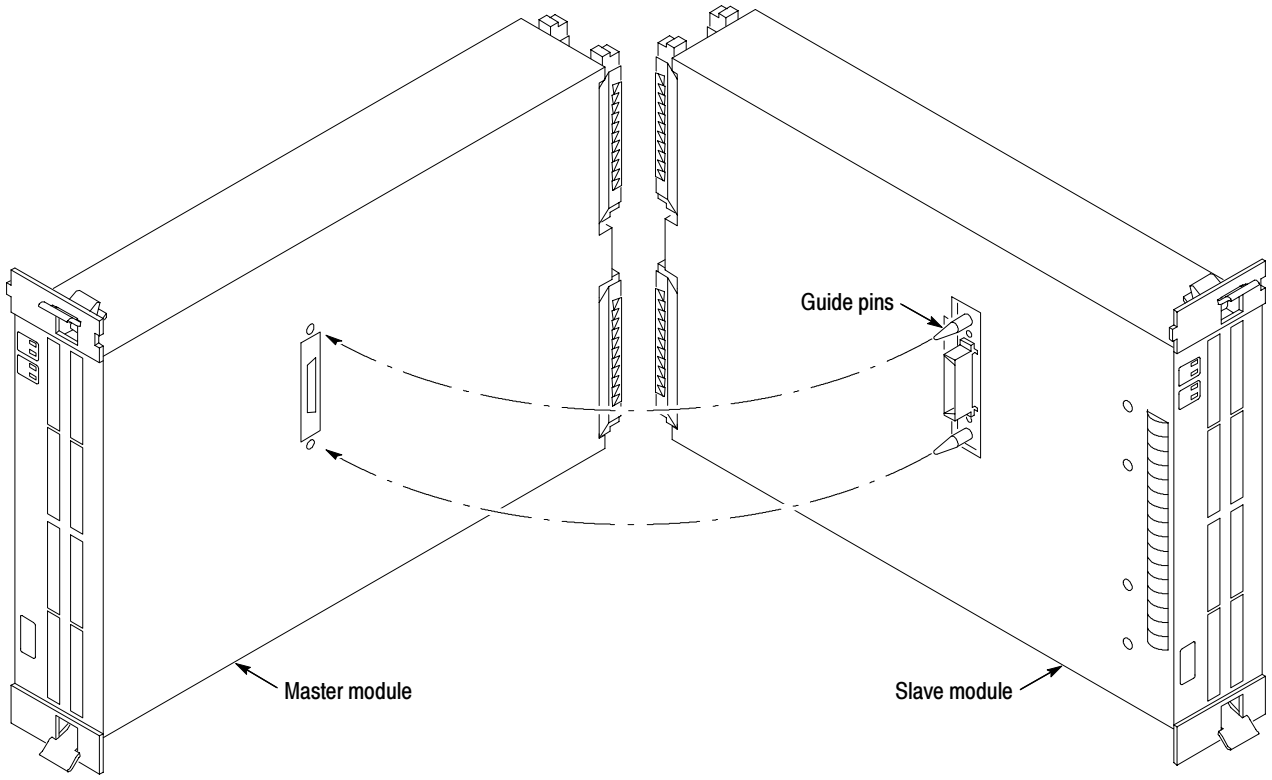


Figure E-8: Lining up the two modules

21. Gently push the two modules together so that the merge connector of the slave module mates with the merge connector on the master module.

Three-Way Logic Analyzer Merge Procedure

The following procedure is used for merging three logic analyzer modules together to form a merged set with a higher logic analyzer channel count.

In a three-way merge (TLA7Nx, TLA7Px, and TLA7Qx logic analyzer modules only), the master module is in the center. Slave module 1 is to the right of the master module. Slave module 2 is on the left of the master module as shown in Figure E–1 on page E–3.

CAUTION. *Static discharge can damage any semiconductor component in the logic analyzer module.*

Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while performing the merge procedure.

Perform the *Two-Way Logic Analyzer Merge Procedure* beginning on page E–8.

Perform the following steps to merge the second slave module:

1. Lay the two merged module set on its right side (as viewed from the front panel).
2. Follow the procedure beginning on page E–8 to merge the second slave module to the left of the center master module.

Storing the Logic Analyzer Module Merge Cable

Perform the following steps to store the logic analyzer merge cable inside the logic analyzer module:

1. Use the screwdriver with the T-10 Torx tip to remove the screws that hold the merge cable bracket in place.
2. Remove the merge cable bracket.
3. Remove the screws from the side cover and rear cover.
4. Push the merge cable through the side cover and remove the cover.
5. Position the merge cable as shown in Figure E–9.

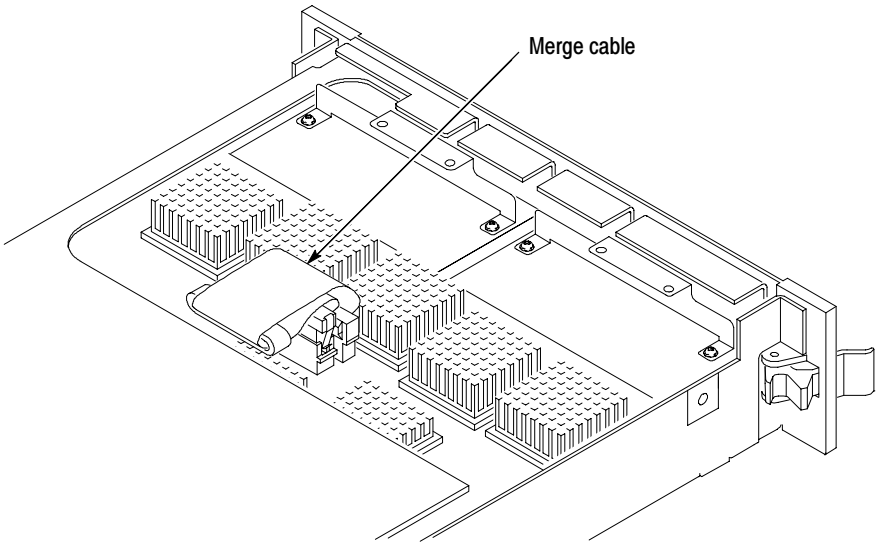


Figure E-9: Positioning the merge cable before installing the cover

6. Push forward on the cover so that you insert the tab on the front edge of the cover into the rear of the front subpanel. Make sure that the cover is fully seated and there are no gaps between the front and rear chassis flanges; refer to Figure E–7.
7. While holding the cover in place, install the screws nearest the front of the module to secure the cover to the chassis.
8. Install the screws near the front of the module.
9. Slide the rear panel on the chassis and install the rear panel screws.
10. Install the top and bottom rear screws.
11. Install the merge cable bracket so that the guide pins point into the module.
12. Install and tighten the screws on the merge cable bracket.
13. Verify that you have installed and tightened all screws on the module.

Appendix F: Power Cord and Line Fuse Requirements for the Benchtop and Expansion Mainframes

The benchtop and expansion mainframes come with two power cords and three fuses (one fuse is already installed).

CAUTION. *You must determine the correct fuse and power cord for your configuration. This is important to avoid overloading the power distribution system and ensures that you comply with the National Electrical Code.*

The power consumption depends on the number and type of instrument modules installed in the mainframes. Table F–1 lists the power consumed for each module.

To determine the total power consumption, perform the following steps:

1. Use Table F–1 to determine the power consumption for each module.
2. Add the power for each module to determine the total power consumption.
3. Determine at which line voltage you will be operating.
4. Refer to Figure F–1 on page F–3 to determine the proper power cord and line fuse for your mainframe.

Table F-1: Power for instrument modules

Module type	Power (Watts)
Mainframe[1]	100
TLA721 Benchtop Controller	70
TLA720 Benchtop Controller	50
TLA7XM Expansion Module	20
TLA7AA1	45
TLA7AA2	65
TLA7AA3	85
TLA7AA4	105
TLA7AB2	65
TLA7AB4	105
TLA7Q2	51
TLA7Q4	75

Table F-1: Power for instrument modules (Cont.)

Module type	Power (Watts)
TLA7P2	50
TLA7P4	74
TLA7N1	45
TLA7N2	58
TLA7N3	71
TLA7N4	82
TLA7L1	55
TLA7L2	73
TLA7L3	94
TLA7L4	109
TLA7M1	57
TLA7M2	76
TLA7M3	99
TLA7M4	116
TLA7D1	80
TLA7D2	111
TLA7E1	90
TLA7E2	121
TLA7PG2	110

[1] **Power for benchtop mainframe and expansion mainframe with fans operating at maximum speed.**

For power usage in the unshaded region of Figure F-1, use either the power cord with the 15 A plug (two parallel prongs and ground) or the power cord with the 20 A plug (two perpendicular prongs and ground).

For high power usage combined with low input line voltages (shaded region), use only the power cord with the 20 A plug. Select the proper fuse based on the ranges shown in Figure F–1.

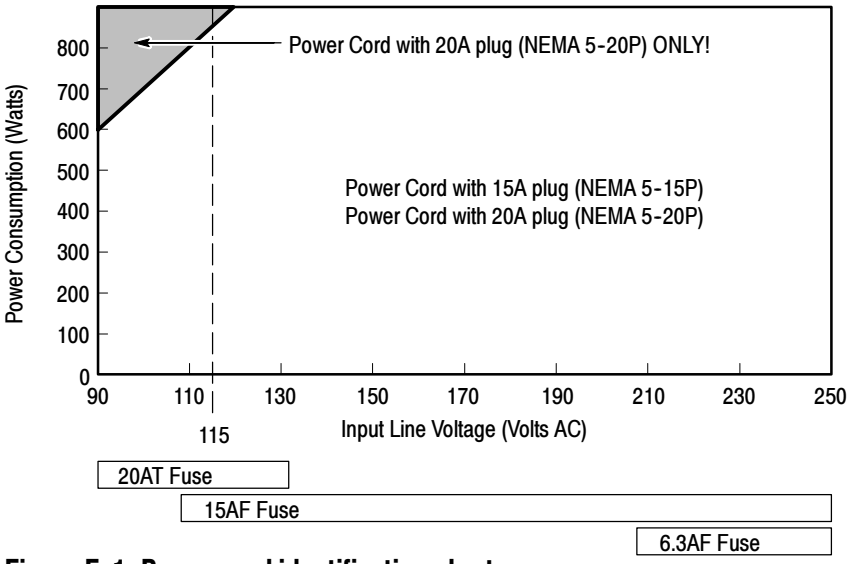


Figure F- 1: Power cord identification chart

For example, assume that your TLA721 benchtop system consists of four TLA7Q4 Logic Analyzer Modules and one TLA7E2 DSO Module. Also assume that you will be operating the mainframe at 90 VAC.

Add 121 Watts (for the DSO Module) + 4 X 75 Watts (for the logic analyzer modules) + 70 Watts (for the controller) + 100 Watts for the mainframe to come up with a total value of 591 Watts.

Because the power consumption (at 90 VAC) is approaching the shaded area of the graph in Figure F–1, you should consider using the 20A power cord.

NOTE*. If you are configuring an expansion mainframe, remember to use the power value for the expansion module instead of the benchtop controller.*

Appendix G: Installing Software

Most of the software comes factory-installed when you receive your logic analyzer. You should only need to refer to this appendix if you reinstall your software. These instructions only refer to reinstalling the latest version of the application software running on the Windows 2000 Professional operating system. If you want to upgrade to the latest application software version and to the Windows 2000 Professional operating system, contact your local Tektronix representative about purchasing either the TLA6UP or TLA7UP field upgrade kits. This appendix also provides information on installing related logic analyzer software on a PC for remote operation or for offline applications.

When reinstalling software on your logic analyzer hard disk, you can reinstall the entire software or the individual software components.

***NOTE**. If you install or reinstall any software on a remote PC, make sure that the software version matches that of the main application on the logic analyzer.*

Refer to the following topics in this appendix to install or reinstall software:

- To reinstall the entire software on your logic analyzer, refer to the instructions under *Restoring the Hard Disk Image* beginning on page G–2.
- To reinstall the latest version of Tektronix Logic Analyzer application software, follow the instructions under *Reinstalling the TLA Application Software* beginning on page G–16.
- To reinstall the latest version of Tektronix Pattern Generator application software, follow the instructions under *Reinstalling the Pattern Generator Application Software* beginning on page G–17.
- To reinstall the latest version of the TPI or PPI remote operation software follow the instructions under *Installing the Remote Operation Software* beginning on page G–18.
- To reinstall the latest version of the TLAVu offline software, refer to *Installing the TLAVu Software* beginning on page G–19.
- To reinstall the latest version of the PatGenVu offline software, refer to *Installing the PatGenVu Software* beginning on page G–20.
- To reinstall other software, refer to the instructions that came with your software.
- To upgrade the firmware on the TLA products, refer to *Upgrading or Restoring Firmware* beginning on page G–20.

Restoring the Hard Disk Image

The next several pages describe the steps needed to restore the logic analyzer application software and operating system on the hard disk. The following procedures will overwrite the entire contents of your hard disk. You must back up any files that you want saved to another media before completing these procedures.

These procedures assume that you are restoring TLA application software V4.2 and the Windows 2000 Professional operating system. If your instrument does not have TLA application software V4.2, you are encouraged to purchase one of the TLA6UP or TLA7UP field upgrade kits. Contact your local Tektronix representatives for more information on the upgrade kits.

The restore procedures will also restore the Pattern Generator application software and any other software applications that came with your logic analyzer.

CAUTION. *The software installation procedure using the Hard Disk Image CD will overwrite the* ***entire contents*** *of your hard disk. If you want to save any files or software applications on the hard disk, back them up to another media (a second hard drive, floppy disks, or a network drive) before continuing with this procedure.*

TLA600, TLA714, or TLA720 Instruments. Before restoring the software on your instrument, you are encouraged to update the BIOS settings. To update the BIOS or to verify the BIOS settings, follow the procedures under *Flashing the BIOS* before restoring the software on your hard disk.

If you feel that your BIOS settings do not need updating, continue with the steps under *Reinstalling the Hard Disk Image* beginning on page G–11.

TLA715 or TLA721 Instruments. If you have a TLA715 or TLA721 logic analyzer, there is no need to update the BIOS settings. Continue with the steps under *Reinstalling the Hard Disk Image* beginning on page G–11.

Flashing the BIOS

You may need to flash the controller BIOS on your logic analyzer to update the controller with the latest flash image before reinstalling software on the hard disk. The procedures for flashing the BIOS differ between the TLA600 logic analyzers and the TLA700 logic analyzers. Refer to the proper procedure before flashing the BIOS image on your logic analyzer.

Flashing the BIOS on the TLA600 Logic Analyzer

This procedure is only necessary if you need to update the latest flash image. To flash the BIOS, complete the following steps:

1. Exit all applications and power off the logic analyzer.
2. Insert the TLA600 BIOS disk, Version P09, in the floppy disk drive.
3. Power on the logic analyzer and allow the logic analyzer to boot from the floppy disk. After booting from the floppy disk, the program on the floppy disk will automatically flash the BIOS on the TLA600 controller.
4. Wait for the flash procedure to complete.
5. After the flash procedure has completed, power off the logic analyzer and remove the floppy disk.

CAUTION. *To avoid rendering the system inoperable, do not remove the floppy disk or power down the logic analyzer during the flash operation.*

Setting Up the TLA600 Controller BIOS

This procedure is necessary after replacing the hard disk or when the CMOS settings are corrupted or lost. To configure the Controller BIOS, complete the following steps:

1. Power on the logic analyzer and press function key F2 before the logic analyzer boots the Windows operating system.
2. Press function key F9, select Yes, and then press Enter to set the default settings. Verify that the hard disk was auto-recognized and that the correct size of the hard disk is displayed in the Primary Master setting.
3. Verify that all of the settings are the same as the settings in Table G–1.
4. Press function key F10 to exit and save the BIOS setup.

Table G- 1: TLA600 Controller BIOS setup

Parameter	Setting/Description	2nd Field setting	Memo
Main			
Processor Type	Intel Celeron		No active selections
Processor Speed	500 MHz		No active selections
Cache RAM	128 KB		No active selections
Total Memory	64 MB		64 MB or 128 MB
Memory Bank 0	64 MB		
Memory Bank 1	Not Installed		Will be installed as an option
System Time	*Set to current time*		
System Date	*Set to current date*		
Advanced			
▶ **Boot Configuration**			
Plug & Play O/S	[No]		
Reset Configuration Data	[No]		
Numlock	[Off]		
▶ **Peripheral Configuration**			
Serial Port A	[Auto]		
Serial Port B	[Disabled]		
Parallel Port	[Auto]		
Mode	[ECP]		
Audio Device	[Enabled]		
LAN Device	[Enabled]		
Legacy USB Port	[Enabled]		
▶ **IDE Configuration**			
IDE Controller	[Both]		
Hard Disk Pre-Delay	[Disabled]		
▶ Primary IDE Master	[Mfg. name - model] (HDD)		e.g.: Autodectable
▶ Primary IDE Slave	[Not installed]		
▶ Secondary IDE Master	[Mfg. name - model] (CD ROM)		e.g.: Autodectable
▶ Secondary IDE Slave	[Not installed]		

Table G- 1: TLA600 Controller BIOS setup (Cont.)

Parameter	Setting/Description	2nd Field setting	Memo
▶ **Diskette Configuration**			
Diskette Controller	[Enabled]		
Floppy A	[1.44/1.25 MB 3 1/2		
Diskette Write Protect	[Disabled]		
▶ **Event Log Configuration**			
Event Log	[Space Available]		Not Active Selections
Event Log Validity	[Valid]		Not Active Selections
▶ View Event Log		Event Log: Pre-Boot Error: CMOS Checksum Error	On the 2nd attempt reading "No unread events"
Clear Event Log	[No]		
Event Logging	[Enabled]		
▶ Mark Events as Read		[Yes]	
▶ **Video Configuration**			
Primary Video Adapter	[PCI]		PCI = Internal Display AGP = External Monitor
▶ **Security**			
Supervisor Password Is	[Not Installed]		Not Active Selections
User Password Is	[Not Installed]		Not Active Selections
▶ Set Supervisor Password		Enter Password	
▶ Set User Password		Enter Password	
▶ **Power**			
Power Management	[Enabled]		
Inactivity Timer	[Off]		
Hard Drive	[Enabled]		
Video Power Down	[Disabled]		
ACPI Suspend State	[S1 State]		
▶ **Boot**			
Quiet Boot	[Disabled]		
Quick Boot	[Enabled]		
Scan Upper Flash Area	[Disabled]		
After Power Failure	[Last State]		
On Modem Ring	[Stay Off]		
On LAN	[Power On]		

Table G- 1: TLA600 Controller BIOS setup (Cont.)

Parameter	Setting/Description	2nd Field setting	Memo
On PME	[Stay Off]		
1st Boot Device	[Floppy]		
2nd Boot Device	[IDE-HDD]		
3nd Boot Device	[ATAPI CDROM]		
4th Boot Device	[Intel UNDI, PXE-2.0 (b)]		
5th Boot Device	[Disabled]		
▶ IDE Drive Configuration			
	▶ Primary IDE Master	[1st IDE]	
	▶ Primary IDE Slave	[2nd IDE]	
	▶ Secondary IDE Master	[3rd IDE]	
	▶ Secondary IDE Slave	[4th IDE]	
▶ **Exit**			
▶ Exit Saving Changes	Yes or No		
▶ Exit Discarding Changes	Yes or No		
▶ Load Setup Defaults	Yes or No		
▶ Load Custom Defaults	Yes or No		
▶ Save Custom Defaults	Yes or No		
▶ Discard Changes	Yes or No		

Flashing the BIOS on the TLA700 Logic Analyzers

This procedure is only necessary if you need to update the latest flash image. To flash the BIOS, complete the following steps (use the TLA700 BIOS floppy disk that came with your instrument or with the TLA7UP Upgrade kit):

1. Power on the logic analyzer and press function key F2 before the Windows operating system starts. The BIOS Setup menu displays.
2. From the BIOS Setup menu, go to the Exit menu.
3. Insert the TLA700 BIOS disk in the floppy disk drive.
4. From the Exit menu, choose Exit & Update BIOS.
5. When the system displays a dialog box asking if you want to proceed with the Flash update, confirm your choice.

   The display goes blank during the flash operation, which lasts about one minute. When the BIOS update is complete, the logic analyzer automatically reboots.
6. Remove the BIOS disk from the floppy disk drive.

CAUTION. *Do not remove the floppy disk drive or power down the logic analyzer during the flash operation. Doing so will cause the system to become inoperable.*

Setting Up the TLA700 Controller BIOS

This procedure is necessary after replacing the hard disk or when the CMOS settings are corrupted or lost. To configure the Controller BIOS, complete the following steps:

1. Power on the logic analyzer and press function key F2 before the logic analyzer boots the Windows operating system.
2. Press function key F9, select Yes, and then press Enter to set the default settings. Verify that the hard disk was auto-recognized and that the correct size of the hard disk is displayed in the Primary Master setting.
3. If you have a TLA715 or TLA721 logic analyzer, all of the settings are the default settings. Press function key F10 to exit and save the BIOS setup and then continue with the hard disk image installation procedure beginning on page G–11.
4. If you have a TLA714 or TLA720 logic analyzer verify that all of the settings are the same as the settings in Table G–2.
5. Press function key F10 to exit and save the BIOS setup.

Table G-2: TLA714 and TLA720 Controller BIOS setup

Parameter	Factory setting	Submenu parameter	Factory setting
Main			
System Time	*Set to current time*		
System Date	*Set to current date*		
Legacy Diskette A	[1.44/1.25 MB, 3 1/2"]		
▶ Primary Master	*hard disk drive size*		
		Type	[Auto]
		Cylinders	*Set by Autotype*
		Heads	*Set by Autotype*
		Sectors	*Set by Autotype*
		Maximum Capacity	*Set by Autotype*
		Multi-sector transfers	*Set by Autotype*
		LBA Mode Control	*Set by Autotype*
		32-Bit I/O	[Disabled]
		Transfer Mode	*Set by Autotype*
		Ultra DMA Mode	*Set by Autotype*
▶ Primary Slave	[None]		
▶ Secondary Master	[CD-ROM]		
▶ Secondary Slave	[None]		
Enable SimulScan	[Disabled]		
Summary Screen	[Disabled]		
▶ Memory Cache			
		Memory Cache	[Enabled]
		External Cache	[Disabled]
		Cache System BIOS area:	[Enabled]
		Cache Video BIOS area:	[Disabled]
		Cache D000 - D3FF:	[Disabled]
		Cache D400 - D7FF:	[Disabled]
		Cache D800 - DBFF:	[Disabled]
System Memory	640 KB		
Extended Memory	*Installed memory - 640 K*		

Table G-2: TLA714 and TLA720 Controller BIOS setup (Cont.)

Parameter	Factory setting	Submenu parameter	Factory setting
Advanced			
▶ I/O Device Configuration			
		Local Bus IDE Adapter	[Both]
		Serial port A	[Enabled]
		Base I/O Address	[3F8]
		Interrupt	[IRQ4]
		Serial port B	[Enabled]
		Mode	[Normal]
		Base I/O Address	[2F8]
		Interrupt	[IRQ3]
		Parallel Port	[Enabled]
		Mode	[ECP]
		Base I/O Address	[378]
		Interrupt	[IRQ7]
		DMA Channel	[DMA 1]
		Floppy disk controller	[Enabled]
▶ Advanced Chipset Control			
		DRAM Speed	[60 ns]
		DMA Aliasing	[Enabled]
		16 Bit I/O Recovery	[4.5]
		8 Bit I/O Recovery	[4.5]
Plug & Play O/S	[Yes]		
Reset Configuration Data	[No]		
PS/2 Mouse	[AutoDetect]		
Large Disk Access Mode:	[Other]		
Secured Setup Configurations	[No]		
▶ PCI Configuration			
		ISA graphics device installed	[No]
		▶ PCI/PNP ISA UMB Region Exclusion	
		C800 - CBFF	[Available]
		CC00 - CFFF	[Available]
		D000 - D3FF	[Available]

Table G- 2: TLA714 and TLA720 Controller BIOS setup (Cont.)

Parameter	Factory setting	Submenu parameter	Factory setting
		D400 - D7FF	[Available]
		D800 - DBFF	[Available]
		DC00 - DFFF	[Available]
		▶ PCI/PNP ISA IRQ Resource Exclusion	
		IRQ3	[Available]
		IRQ4	[Available]
		IRQ5	[Available]
		IRQ7	[Available]
		IRQ9	[Available]
		IRQ10	[Available]
		IRQ11	[Available]
		IRQ14	[Available]
		IRQ15	[Available]
Power			
Power Savings	[Disabled]		
Standby Timeout:	[Off]		
Auto Suspend Timeout	[Off]		
Resume On Time	[Off]		
IDE Drive 0 Monitoring	[Disabled]		
IDE Drive 1 Monitoring	[Disabled]		
IDE Drive 2 Monitoring	[Disabled]		
IDE Drive 3 Monitoring	[Disabled]		
PCI Bus Monitoring	[Disabled]		

Table G-2: TLA714 and TLA720 Controller BIOS setup (Cont.)

Parameter	Factory setting	Submenu parameter	Factory setting
Boot			
1.	[Diskette Drive]		
2.	[Removable Devices]		
3.	[Hard Drive]		
4.	[ATAPI CD-ROM Drive]		
▶ Hard Drive			
		1.	*Currently installed drive ID*
		2.	[Bootable Add-in Card]
▶ Removable Devices			
Exit			
▶ CMOS Save & Restore			
		CMOS Restore Condition	[Never]

Reinstalling the Hard Disk Image

The Tektronix Logic Analyzer comes with a CD containing Microsoft Windows 2000 Professional operating system and the latest application software. All software required to run the logic analyzer comes with the CD with the exception of any Microprocessor support packages or non-logic analyzer application software. The process of reloading the software on the hard disk will destroy any files or programs installed on the hard disk.

Use the appropriate CD for your application.

- For TLA715 or TLA721 instruments (or upgraded TLA714 and TLA720 instruments with new controllers), use the CD labeled *TLA715 & TLA721 Hard Disk Image*. Upgraded TLA714 and TLA721 instruments can be identified by a TLA7UP Option 16 or Option 17 label on the instrument.
- For TLA714 or TLA720 instruments, use the CD labeled *TLA714 & TLA720 Hard Disk Image*.
- For TLA600 instruments, use the CD labeled *TLA600 Hard Disk Image*.

CAUTION. *To avoid destroying the* ***entire contents*** *of your hard disk, save any files or applications by backing them up to another media (a second hard drive, CD, or a network drive) before continuing with this procedure.*

Backing Up Files

Before loading the Hard Disk Image software, make sure that you back up any files, applications, and personal documents to an external storage device. You can do this using one of the following methods:

- Move the files to another PC via a network or via another backup medium such as a ZIP drive.
- If you have a TLA700 series logic analyzer, purchase TLA7UP Option 12 (for instruments with TLA Application software version 4.2) or TLA7UP Option 10 (for instruments with TLA Application software version 4.1 and below). This allows you to install a second hard disk drive so that you can still access the user files. Refer to the *TLA7UP Logic Analyzer Field Upgrade Kit Instruction Manual* for information on installing the second hard disk.

You can find most TLA user files using the Windows Search utility. For example, open Windows Explorer and select the C:\My Documents folder. Right click on the folder and select Search. Enter one of the suffixes from Table G–3 to locate the files in the current folder and all subfolders:

Table G-3: TLA user file suffixes

Suffix	Description
.tla	TLA setup files
.tsf	TLA symbol files
.tbf	Tektronix binary format
.tls	TLA script file
.tpg	Tektronix pattern generator files
.txt	Tektronix TLA data exchange format files

Once you find the files, copy or drag them to the external storage device. Use this procedure to find any files or applications that you may want to save.

If you purchased any microprocessor support packages, you need to reinstall the application after you reinstall the hard disk image. If you don't have a copy of the microprocessor support software, contract your Tektronix Account Manager to order a replacement copy. If you cannot contact the account manager, contact the Tektronix Support Center (refer to *Contacting Tektronix* on page xxiv at the beginning of this document).

***NOTE**. You can reinstall Windows 2000 Professional, SnagIt, CheckIt Utilities, and other software only from the Hard Disk Image CD that came with your instrument. These software applications are licensed and cannot be reinstalled by any other method without violating the license agreements.*

Installing Windows 2000 Professional and the TLA Application Software

This procedure reformats the hard disk, installs the Windows 2000 Professional Operating system software, and installs the Tektronix Logic Analyzer application software. Because this procedure reformats the hard disk drive, be sure to back up any files or software that you want to preserve by following the steps in the previous section.

***CAUTION.** To avoid losing files or applications on your hard disk, back them up before proceeding.*

After installing the hard disk image, you must reset the BIOS boot settings to the Tektronix defaults.

Change the BIOS Boot Settings. Before installing the Hard Disk Image, you must change the BIOS settings.

1. Restart the logic analyzer and then press function key F2 to enter the BIOS setup.
2. In the BIOS setup, go to the Boot menu.
3. Set the Boot devices for your instrument as shown in Table G–4 (follow the on-screen instructions to change the settings).

Table G- 4: Bios Boot settings for reinstalling software

Instrument	Setting	
TLA715 or TLA721	ATAPI CD-ROM Drive	
	+Removable Devices	
	+Hard Drive	
TLA714 or TLA720	First Boot Device:	[ATAPI CDROM Drive]
	Second Boot Device:	[Diskette Drive]
	Third Boot Device:	[Hard Drive]
TLA600 series	First Boot Device:	[ATAPI CDROM Drive]
	Second Boot Device:	[Floppy]
	Third Boot Device:	[IDE-HDD]

4. Save the settings by pressing function key F10 and confirm that you want to save the new settings.

Load the Hard Disk Image. Complete the following steps to load the Hard Disk Image.

1. Insert the Hard Disk Image CD in the CD-ROM drive.
2. Reboot the logic analyzer.
3. Review the license agreement. If you agree to the terms of the license agreement, proceed with the next step.

NOTE. *Use care when proceeding through the software license agreement to avoid confirming that you want to cancel the software installation procedure.*

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4. After you review the software license agreement, the EasyRestore dialog box displays and prompts you to either continue or cancel the upgrade process. Click Continue to begin loading the contents of the upgrade CD.
5. The EasyRestore program displays a warning that the contents of your hard disk will be destroyed if you choose to continue. Click Yes to continue the process.
6. The program will automatically start and guide you through the rest of the procedure. The image loading procedure is fully automatic and takes approximately 15 minutes to complete.

   The image loading procedure automatically installs and sets up the logic analyzer application. You should not need to make any changes to the setup to use the logic analyzer.
7. After the image is loaded, remove the CD from the CD-ROM drive and reboot the logic analyzer.
8. The Systems Settings Change error message displays, prompting you to restart the instrument before your changes can take effect. Click Yes to restart the instrument.
9. Reinstall any user files that you backed up previously. Reinstall any software (such as the microprocessor support packages) that you want to use on the logic analyzer.
10. If desired, reconfigure the TLA network interface.

Reset the BIOS Boot Settings. After you have successfully installed the hard disk image, you should reset the BIOS boot settings so that your logic analyzer boots properly.

1. Restart the logic analyzer and then press function key F2 to enter the BIOS setup.
2. In the BIOS setup, go to the Boot menu.
3. Set the Boot devices for your instrument as shown in Table G–5 (follow the on-screen instructions to change the settings).

Table G-5: Bios Boot settings for reinstalling software

Instrument	Setting	
TLA715 or TLA721	+Removable Devices	
	+Hard Drive	
	ATAPI CD-ROM Drive	
TLA714 or TLA720	First Boot Device:	[Diskette Drive]
	Second Boot Device:	[Removable Devices]
	Third Boot Device:	[Hard Drive]
	Third Boot Device:	[ATAPI CDROM Drive]
TLA600 series	First Boot Device:	[Floppy]
	Second Boot Device:	[Removable Devices]
	Third Boot Device:	[IDE-HDD]
	Fourth Boot Device:	[[ATAPI CDROM Drive]

4. Save the settings by pressing function key F10 and confirm that you want to save the new settings.

Reinstalling the TLA Application Software

Complete the following steps to reinstall the latest version of the TLA application software. Use these steps as a first resort to recovering from application software problems. If you still experience problems with the software after completing these steps, follow the instructions under *Restoring the Hard Disk Image* beginning on page G–2.

While using this procedure you will be asked to log on as Administrator. The logic analyzer is initially set up to automatically log on as Administrator (with no password) so you may not see the login prompt. If the network setups have been changed on your instrument, make sure that you log on as Administrator or as a user who has administrator privileges. Failure to do so can prevent the software upgrade from completing successfully.

1. Log on to the instrument as Administrator and quit any applications.
2. Install Disc 1 of the Tektronix Logic Analyzer Family Application Software in the CD-ROM drive of the logic analyzer.
3. Click Run in the Windows Start menu to display the Run dialog box.
4. Enter D:\TLA Application SW\Disk1\Setup.exe in the Run dialog box (if your CD-ROM drive is not the D-drive, enter the appropriate letter for your drive).
5. Click OK to perform the installation.

   If you have an existing version of the software on the hard disk, the installation program will detect it and ask if you want to remove it. Follow the on-screen instructions to remove the software, answering "Yes" to any prompts. Reboot the instrument when prompted. Repeat Step 4 to reinstall the software following any on-screen prompts.
6. After the software has been successfully installed, restart the instrument.

Reinstalling the Pattern Generator Application Software

Complete the following steps to reinstall the latest version of the pattern generator application software. Use these steps as a first resort to recovering from application software problems. If you still experience problems with the software after completing these steps, follow the instructions under *Restoring the Hard Disk Image* beginning on page G–2.

While using this procedure you will be asked to log on as Administrator. The instrument is initially set up to automatically log on as Administrator (with no password) so you may not see the login prompt. If the network setups have been changed on your instrument, make sure that you log on as Administrator or as a user who has administrator privileges. Failure to do so can prevent the software upgrade from completing successfully.

1. Log on to the instrument as Administrator.
2. Install Disc 1 of the Tektronix Logic Analyzer Family Application Software in the CD-ROM drive of the logic analyzer.
3. Click Run in the Windows Start menu to display the Run dialog box.
4. Enter D:\Pattern Generator Application SW\Disk1\Setup.exe in the Run dialog box (if your CD-ROM drive is not the D-drive, enter the appropriate letter for your drive).
5. Click OK to perform the installation.

   If you have an existing version of the software on the hard disk, the installation program will detect it and ask if you want to remove it. Follow the on-screen instructions to remove the software, answering "Yes" to any prompts. Reboot the instrument when prompted. Repeat Step 4 to reinstall the software following any on-screen prompts.
6. After the software has been successfully installed, restart the instrument.

Installing the Remote Operation Software

The TPI client software and the PPI client software are two software packages that allow you to remotely control the logic analyzer or pattern generator from a remote PC. These software packages are located on Disc 1 of the dual CD-ROM set. You must ensure that the version of the TPI and PPI client software is the same as that of TLA and pattern generator application on your logic analyzer.

Complete the following steps to update the client software packages on your PC. If you have an older version already installed on your PC, the program will automatically detect it and replace it during the upgrade process.

1. Install Disc 1 of the Tektronix Logic Analyzer Family Application Software in the CD-ROM drive of the PC.
2. Click Run in the Windows Start menu to display the Run dialog box.
3. To install the TPI client software, enter D:\TPI Client SW\Disk1\Setup.exe in the Run dialog box.
4. To install the PPI client software, enter D:\PPI Client SW\Disk1\Setup.exe in the Run dialog box.
5. Click OK to perform the installation. Follow any on-screen instructions.
6. If you have an earlier version of either software package installed on your PC, the Setup.exe program will uninstall the application before installing the new version. If you are prompted for permission to remove unused shared files or any read-only files, select Yes to All.

Installing the TLAVu Software

TLAVu application software allows you to view data and create setups for your logic analyzer on a PC. You must ensure that the version of the TLAVu application software is the same as that of TLA application. The TLAVu application software is located on Disc 2 of the dual CD-ROM set.

Complete the following steps to update the TLAVu application software on your PC. If you have an older version already installed on your PC, the program will automatically detect it and replace it during the upgrade process.

1. Install Disc 2 of the Tektronix Logic Analyzer Family Application Software in the CD-ROM drive of the PC.
2. Click Run in the Windows Start menu to display the Run dialog box.
3. Enter D:\TLAVu\Disk1\Setup.exe in the Run dialog box.
4. Click OK to perform the installation. Follow any on-screen instructions.
5. If you have an earlier version of the TLAVu application installed on your PC, the Setup.exe program will uninstall the old application before installing the new version. If you are prompted for permission to remove unused shared files or any read-only files, select Yes to All.

***NOTE**. The ReadMe file for the TLAVu application contains most of the information that you need to run the application. Access the ReadMe file by selecting: Start → Programs → Tektronix Logic Analyzer → TLA Documentation → TLAVu ReadMe.*

Installing the PatGenVu Software

The PatGenVu application software allows you to view data and create setups for your pattern generator on a PC. You must ensure that the versions of the PatGenVu software are the same as the pattern generator application. The PatGenVu software application is located on Disc 2 of the dual CD-ROM set.

Complete the following steps to upgrade the PatGenVu application software on your PC. If you have an older version already installed on your PC, the installation program will automatically detect it and replace it during the upgrade process.

1. Install Disc 2 of the Tektronix Logic Analyzer Family Application Software in the CD-ROM drive of the PC.
2. Click Run in the Windows Start menu to display the Run dialog box.
3. Enter D:\PatGenVu\Disk1\Setup.exe in the Run dialog box.
4. Click OK to perform the installation. Follow any on-screen instructions.
5. If you have an earlier version of the PatGenVu application installed on your PC, the Setup.exe program will uninstall the old application before installing the new version. If you are prompted for permission to remove unused shared files or any read-only files, select Yes to All.

NOTE. *The ReadMe file for the PatGenVu application contains most of the information that you need to run the application. Access the ReadMe file by selecting: Start → Programs → Tektronix Pattern Generator → Pattern Generator Documentation → PatGenVu ReadMe.*

Upgrading or Restoring Firmware

You may have to upgrade the firmware on the logic analyzer or on individual modules if the firmware version is not compatible with the TLA application software version. This may be evident when a module does not appear in the TLA System window. The most current firmware for the TLA application software resides in a file on the hard disk of the logic analyzer.

Although the firmware update procedures are similar, there are some key differences between the Tektronix Logic Analyzer products and are therefore listed as separate procedures. If you have mixed modules within your TLA700 mainframe, you should review the procedures for each of the modules before beginning the upgrade.

Upgrading Firmware on TLA7Axx Logic Analyzer Modules

Use the following procedure to upgrade the firmware for the TLA7Axx Series Logic Analyzer Modules.

1. Note which modules require new firmware.

   If any modules are missing from the System window, you can verify the status of the modules by doing the following steps:

   a. Select System Properties from the System menu.

   b. Click the Modules tab.

   c. Note the information under the Messages column for any installed modules. If any modules indicate invalid or similar messages, you must update the firmware for those modules.

2. Disconnect probes connected to the modules that you want to update.

3. Exit the logic analyzer application.

4. Click Start → Programs → Tektronix Logic Analyzer → TLA Firmware Loader.

5. You may be prompted to cycle the power on the mainframe after completing the upgrade operation. Click Yes to continue.

   The logic analyzer will scan the mainframe to determine which modules are installed and which modules can have their firmware upgraded. If you have any older modules, you may see them listed in the bottom half of the window. These modules cannot be updated until you install the flash jumper on the rear of the modules.

6. Select the modules that you want to update from the list of modules displayed in the Supported list box near the top of the window. If you are updating more than one module at a time, note the slot location of the module in the selection box.

7. Select Load Firmware from the Execute menu.

8. Click the TLA7A.lod file for the selected module.

***NOTE**. Be sure to select the proper .lod file for each module. Note the slot number in the title bar so that you select the correct module for the .lod file.*

9. Click OK. You will be prompted to confirm your action; click Yes.

***NOTE**. The program will not allow you to load firmware to an incompatible module. For example, the program will not load DSO firmware to a logic analyzer module.*

The program will load the firmware for each module one at a time. The process may take several minutes per module.

10. Exit the firmware loader program and power down the logic analyzer. You must power down the logic analyzer to allow the TLA application to start up properly.
11. Remove the logic analyzer module from the mainframe.
12. Locate the big label on the side of the module.
13. Record the firmware version that is printed on the label. You will need this information to see that the firmware version matches the label.
14. Reinstall the module in the mainframe and power on the mainframe.
15. After the logic analyzer completes the power-on diagnostics, select System Properties from the System menu.
16. Click the module tab (for example, LA1).
17. Verify that the firmware version for the selected module matches the version on the label that you recorded in step 13.
18. If the firmware versions do not match, power down the mainframe, remove the module from the mainframe and update the label.

Upgrading the TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px TLA7Qx or DSO Firmware

Complete the following steps to upgrade the module firmware on the TLA7Lx, TLA7Mx, TLA7Nx, TLA7Px, or TLA7Qx logic analyzer modules and the TLA7Dx or TLA7Ex DSO modules. These modules require you to install a jumper on the rear of the module before you can upgrade the firmware.

1. Note which of the modules that may require new firmware.

   If any modules are missing from the System window, you can verify the status of the modules by doing the following steps:

   a. Select System Properties in the System menu.

   b. Click the Modules tab.

   c. Note the information under the Messages column for any installed modules. If any modules indicate invalid or similar messages, you must update the firmware for those modules.

2. Turn off the logic analyzer and disconnect the power cord.

3. Disconnect any probes connected to the modules that you want to upgrade.
4. Remove the modules from the logic analyzer.
5. Refer to Figure G–1 and locate the flash programming pins on the rear of each module.
6. Install a jumper on the flash programming pins (use one of the spare jumpers that came with your logic analyzer).
7. Reinstall the module(s) in the logic analyzer.

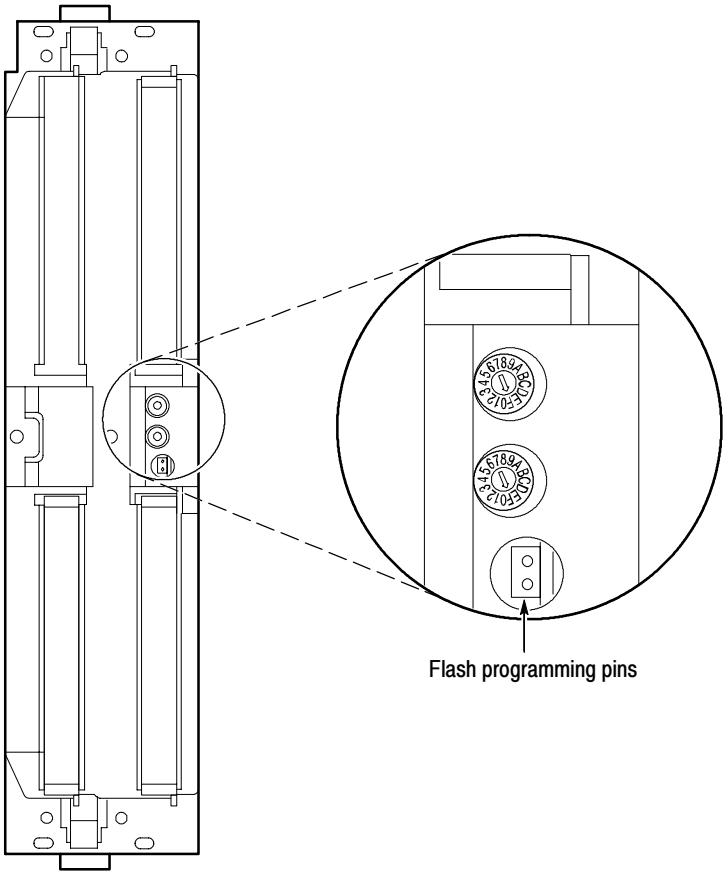

Figure G-1: Flash programming pins

8. Reconnect the power cord and then power on the logic analyzer.
9. Wait for the TLA application to start.

***NOTE**. Any modules with the flash programming jumper installed will not display in the System window.*

10. Exit the TLA application (and pattern generator application if you have it installed on your instrument).
11. Click Start → Programs → Tektronix Logic Analyzer → TLA Firmware Loader.
12. Select the modules that you want to update from the list of modules displayed in the Supported list box near the top of the window. This selects the modules for the upgrade.
13. If you are upgrading more than one module at a time, note the slot location of the module in the selection box.
14. Select Load Firmware from the Execute menu.
15. Click the proper .lod file for the selected module; refer to Table G–6 if necessary. (The .lod files are located in the C:\Program Files\TLA 700\Firmware directory).

***NOTE**. Be sure to select the proper .lod file for each module. Note the slot number in the title bar so that you select the correct module for the .lod file.*

Table G-6: TLA firmware files

Module type	.lod file
TLA7Nx, TLA7Px, TLA7Qx logic analyzer modules	TLA7NPQ.lod
TLA7Lx and TLA7Mx logic analyzer modules	TLA7LM.lod
TLA7Dx and TLA7Ex DSO modules	FirmwareDSO.lod
TLA720 Benchtop controller module	TLA720.lod

16. Click OK. You will be asked to confirm your action; click Yes when prompted.

***NOTE**. The program will not allow you to load firmware to an incompatible module. For example, the program will not load DSO firmware to a logic analyzer module.*

The program will load the firmware for each module one at a time. The process may take several minutes per module.

17. When the upgrade is complete, exit the program.

18. Turn off the logic analyzer and disconnect the power cord.
19. Remove the module from the instrument and remove the jumper from the Flash programming pins on the rear of the module. Keep the jumper for future updates.
20. Locate the big label on the side of the module.
21. Record the firmware version that is printed on the label. You will need this information to see that the firmware version matches the label.
22. Reinstall the module in the mainframe and power on the mainframe.
23. After the logic analyzer completes the power-on diagnostics, select System Properties from the System menu.
24. Click the module tab (for example, LA1).
25. Verify that the firmware version for the selected module matches the version on the label that you recorded in step 21.
26. If the firmware versions do not match, power down the mainframe, remove the module from the mainframe and update the label.

Upgrading Firmware on the Pattern Generator Modules

Use the following procedure to upgrade the firmware on the pattern generator modules.

1. Note which modules require new firmware.

   If any modules are missing from the System window, you can verify the status of the modules by doing the following steps:

   a. Select System Properties in the System menu.

   b. Click the Modules tab.

   c. Note the information under the Messages column for any installed modules. If any modules indicate invalid or similar messages, you must update the firmware for those modules.

2. Power down the mainframe and disconnect the power cord.
3. Disconnect probes connected to the modules that you want to upgrade.
4. Remove the modules from the mainframe.

5. Refer to Figure G–2 and locate the flash programming pins on the rear of each module.
6. Install a jumper on the flash programming pins (use one of the spare jumpers that came with your pattern generator).
7. Reinstall the modules in the mainframe.

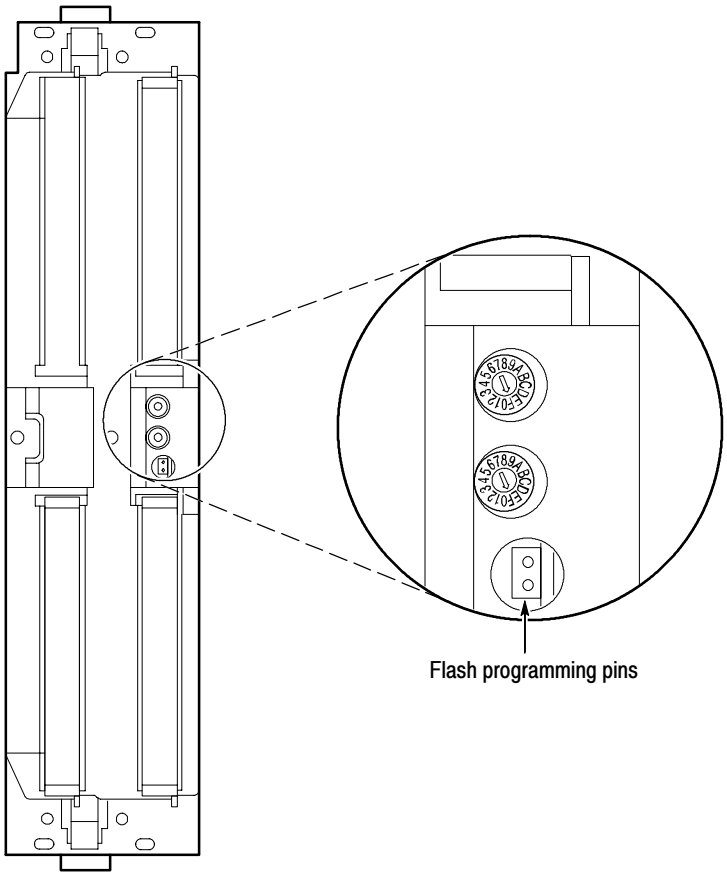

Figure G-2: Flash programming pins

8. Reconnect the power cord and then power on the mainframe.
9. Wait for the pattern generator application to start.

NOTE. *Any modules with the flash programming jumper installed will not display in the System window.*

10. Exit the pattern generator application (and the TLA application).

11. Click Start → Programs → Tektronix Logic Analyzer → TLA Firmware Loader.
12. Select the modules that you want to update from the list of modules displayed in the Supported list box near the top of the window. This selects the modules for the upgrade.
13. If you are upgrading more than one module at a time, note the slot location of the module in the selection box.
14. Select Load Firmware from the Execute menu.
15. Select the tla7pg2.lod file for the selected module; if necessary, navigate to the C:\Program Files\Tektronix Pattern Generator\Firmware folder.
16. Click OK. You will be prompted to confirm your action; click Yes.

    The program will load the firmware for each module one at a time. The process may take several minutes per module.
17. When the upgrade is complete, exit the program.
18. Power down the mainframe and disconnect the power cord.
19. Remove the module from the instrument and remove the jumper from the Flash programming pins on the rear of the module. Keep the jumper for future updates.
20. Locate the big label on the side of the module.
21. Record the firmware version that is printed on the label. You will need this information to see that the firmware version matches the label.
22. Reinstall the module in the mainframe and power on the mainframe.
23. After the instrument completes the power-on diagnostics, select System Properties from the System menu.
24. Click the module tab (for example, PG1).
25. Verify that the firmware version for the selected module matches the version on the label that you recorded in step 21.
26. If the firmware versions do not match, power down the mainframe, remove the module from the mainframe and update the label.

Upgrading Firmware on TLA600 Series Logic Analyzer

Use the following procedure to upgrade the firmware for the TLA600 Series Logic Analyzers. Because the TLA600 Series Logic analyzers are monolithic instruments you can easily tell if the firmware needs updating by the absence of the logic analyzer module in the System window.

1. Disconnect any probes connected to the logic analyzer.
2. Exit the logic analyzer application.
3. Click Start → Programs → Tektronix Logic Analyzer → TLA Firmware Loader.
4. You will be prompted to cycle the power on the mainframe after completing the upgrade operation. Click Yes to continue.
5. Select the module from the Supported list box near the top of the window.
6. Select Load Firmware from the Execute menu.
7. Click the TLA6xx.lod file.
8. Click OK. You will be prompted to confirm your action; click Yes.
9. Exit the firmware loader program and power down the logic analyzer. You must power down the logic analyzer to allow the TLA application to start up properly.
10. Locate the big label on the back of the instrument.
11. Record the firmware version that is printed on the label. You will need this information to see that the firmware version matches the label.
12. Power on the instrument.
13. After the logic analyzers completes the power-on diagnostics, select System Properties from the System menu.
14. Click the LA1 tab.
15. Verify that the firmware version matches the version on the label that you recorded in step 11.
16. If the firmware versions do not match, update the label on the back of the instrument.

Appendix H: User Service

This appendix describes service information and procedures for the Tektronix logic analyzers. Mainframe and module service troubleshooting procedures are located in the service manuals.

Service Offerings

Tektronix provides service to cover repair under warranty as well as other services that are designed to meet your specific service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians are well equipped to service the logic analyzers. *Services are provided at Tektronix Services Centers and on-site at your facility, depending on your location.*

Warranty Repair Service

Tektronix warrants this product for one year from date of purchase. (The warranty appears behind the title page in this manual.) Tektronix technicians provide warranty service at most Tektronix service locations worldwide. The Tektronix product catalog lists all service locations worldwide or you can visit us on our *Customer Services World Center* web site at:

www.tektronix.com/Measurement/Service

Calibration and Repair Service

In addition to warranty repair, Tektronix Service offers calibration and other services that provide cost-effective solutions to your service needs and quality-standards compliance requirements. Our instruments are supported worldwide by the leading-edge design, manufacturing, and service resources of Tektronix to provide the best possible service.

The following services can be tailored to fit your requirements for calibration and/or repair of the TLA logic analyzers:

Service Options. Tektronix Service Options can be selected at the time you purchase your instrument. You select these options to provide the services that best meet your service needs. These service options are listed on the *Tektronix Service Options* page following the title page of this manual.

Service Agreements. If service options are not added to the instrument purchase, then service agreements are available on an annual basis to provide calibration services or post-warranty repair coverage for the TLA logic analyzers. Service agreements may be customized to meet special turn-around time and/or on-site requirements.

Service on Demand. Tektronix also offers calibration and repair services on a "per-incident" basis that is available with standard prices for many products.

Self Service. Tektronix supports repair to the replaceable-part level by providing for circuit board (module) exchange.

Use this service to reduce down-time for repair by exchanging faulty circuit boards for remanufactured ones. Tektronix ships updated and tested exchange boards. Each board comes with a 90-day service warranty.

For More Information. Contact your local Tektronix service center or sales engineer for more information on any of the calibration and repair services.

Service Options

Tektronix offers the following service options. These options are modular, flexible, and easy to order with your instrument. Designed to ease installation and startup, to support tracking of calibration to requirements of ISO9000, and to provide for extended repair coverage, these options help fix your long-term maintenance costs and eliminate unplanned expenditures. These options can be converted from service at Tektronix service depots to service on-site (see Option S1 and S3), which helps keep downtime to a minimum.

TLA600 Series Service Options

The following service options are available for your TLA600 series logic analyzer.

Three years repair coverage	Option R3	Extends product repair warranty to a total of three years.
Five years repair coverage	Option R5	Provides a total of five years of repair coverage, including the product warranty period
Three years of calibration services	Option C3	Provides factory calibration certification on delivery, plus two more years of calibration coverage. Throughout the coverage period the instrument will be calibrated according to its Recommended Calibration Interval.
Five years of calibration services	Option C5	Provides five full years of coverage including the initial calibration within the delivery of the product. C5 is available for traceable products.
Test data	Option D1	Provides initial Test Data Report from factory on delivery.
Test data	Option D3	Provides test data on delivery plus a Test Data Report for every calibration performed during 3 years of coverage – requires Option C3.
Test data	Option D5	Available for traceable products. It delivers a calibration data report with the calibration performed in conjunction with Option C5.

TLA700 Series Service Options

The following service options are available for your TLA700 series logic analyzer.

Three years repair coverage	Option R3	Extends product repair warranty to a total of three years.
Five years repair coverage	Option R5	Provides a total of five years of repair coverage, including the product warranty period
Three years of calibration services	Option C3	Provides factory calibration certification on delivery, plus two more years of calibration coverage. Throughout the coverage period the instrument will be calibrated according to its Recommended Calibration Interval.
Five years of calibration services	Option C5	Provides five full years of coverage including the initial calibration within the delivery of the product. C5 is available for traceable products.
One year upgrade to on-site service[1, 2]	Option S1	Upgrades the standard one year, "return to depot" warranty to an on-site warranty.
Three year upgrade to on-site service[1, 2]	Option S3	Upgrades any C3, D3, and R3 options purchased to on-site coverage for three years.
Test data	Option D1	Provides initial Test Data Report from factory on delivery.
Test data	Option D3	Provides test data on delivery plus a Test Data Report for every calibration performed during 3 years of coverage – requires Option C3.
Product installation service	Option IN	Available for traceable products. It delivers a calibration data report with the calibration performed in conjunction with Option C5.

1 Availability of installation and on-site services depends on the type of product and may vary by geography.

2 Upgrade options are ordered with the mainframe products and cover individual modules.

General Care

Protect the instrument from adverse weather conditions. The instrument is not waterproof.

Do not store or leave the instrument where the LCD display will be exposed to direct sunlight for long periods of time.

CAUTION. *To avoid damage to the instrument, do not expose it to sprays, liquids, or solvents.*

Module Self Calibration

Use the Self Calibration property page to run self calibration procedures for installed modules and merged modules. For all modules, you should run these procedures after repair. At a minimum, you should run these procedures once a year. For the DSO module you should also run these procedures if the ambient operating temperature has changed more than 5 °C since last calibration or once a week if vertical settings of 50 mV full scale or less are used.

Perform self calibration after a 30 minute warm up.

Complete the following steps to run the self calibration procedure:

1. From the System menu and select Calibration and Diagnostics.
2. Click the Self Calibration tab.
3. Select the module to calibrate.
4. Click the Run button.

NOTE*. For merged modules, run the self-calibration procedure on the modules as a merged set.*

Preventive Maintenance

Once a year the electrical performance should be checked and the instrument accuracy certified (calibrated). This service should be performed by a qualified service technician using the procedures outlined in the appropriate service manual for the Tektronix Logic Analyzer product.

Preventive maintenance mainly consists of periodic cleaning. Periodic cleaning reduces instrument breakdown and increases reliability. Clean the instrument as needed, based on the operating environment. Dirty conditions may require more frequent cleaning than computer room conditions.

Cleaning the P6860 and P6880 Probe Compression Footprints

Prior to connecting the probe to the target system, the compression footprints on the customer board must be properly cleaned. Clean the compression footprints according to the following steps:

1. Use a cleanroom wipe (such as Wypall Medium Duty Wipes, #05701, available from Kimberly-Clark Corporation) moistened with isopropyl alcohol to gently wipe the footprint surface.
2. Remove any remaining lint using a nitrogen air gun.

Cleaning the P6860 and P6880 Probe Heads

Prior to connecting the P6860 and P6880 probes to the target system, the probe heads must be properly cleaned. Clean the probe heads according to the following steps:

CAUTION. *Static discharge can damage any semiconductor component in the probe head. Always wear a grounded antistatic wrist strap whenever handling the probe head. Also verify that anything to which the probe head is connected does not carry a static charge.*

1. Moisten a cleanroom wipe (such as Wypall Medium Duty Wipes, #05701, available from Kimberly-Clark Corporation) with isopropyl alcohol.
2. Gently wipe the edge print pads.

Flat Panel Display Cleaning

The LCD flat panel is a soft plastic display and must be treated with care during cleaning.

CAUTION. *Improper cleaning agents or methods can damage the flat panel display.*

Do not use abrasive cleaners or commercial glass cleaners to clean the display surface.

Do not spray liquids directly on the display surface.

Do not scrub the display with excessive force.

Clean the flat panel display surface by gently rubbing the display with a cleanroom wipe (such as Wypall Medium Duty Wipes, #05701, available from Kimberly-Clark Corporation).

If the display is very dirty, moisten the wipe with distilled water or a 75% isopropyl alcohol solution and gently rub the display surface. Avoid using excess force or you may damage the plastic display surface.

Exterior Surfaces

Clean the exterior surfaces with a dry, lint-free cloth or a soft-bristle brush. If dirt remains, use a cloth or swab dampened with a 75% isopropyl alcohol solution. A swab is useful for cleaning in narrow spaces around the controls and connectors. Do not use abrasive compounds on any part of the instrument.

CAUTION. *To avoid damaging the instrument follow these precautions:*

Avoid getting moisture inside the instrument during external cleaning and use only enough solution to dampen the cloth or swab.

Do not wash the front-panel On/Standby switch. Cover the switch while washing the instrument.

Use only deionized water when cleaning. Use a 75% isopropyl alcohol solution as a cleanser and rinse with deionized water.

Do not use chemical cleaning agents; they may damage the instrument. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Floppy Disk Drive

The floppy disk drive requires routine maintenance to operate at maximum efficiency. The disks can be damaged if dirt and dust accumulate on the recording surfaces. To prevent damage, the disks should be properly stored in their protective containers where they will not be exposed to dust or dirt. In addition, the head should be cleaned periodically.

You will need a 3.5-inch floppy disk head-cleaning kit for routine maintenance. Perform the routine maintenance as follows:

Clean the face of the floppy disk drive monthly with a dampened cloth.

CAUTION. *Do not allow moisture to enter the disk drive. When power is applied, the internal components can be damaged.*

Clean the head monthly following the instructions provided with the head-cleaning kit.

In Case of Problems

This section provides information to help you address problems you may encounter while installing and using your logic analyzer.

Diagnostics

The logic analyzer runs power-on diagnostics every time you power on the instrument. You can view the results of the diagnostics by selecting Calibration and Diagnostics from the System menu. You can run more detailed diagnostics by selecting Extended diagnostics. Here you can run all tests, loop on one or more tests, or loop on a test until a failure occurs.

The following diagnostic tools are available with your logic analyzer:

Power-On Diagnostics. Power-on diagnostics run when you first turn on the logic analyzer, or when you first start the TLA or the pattern generator application. If any diagnostic failures occur during turn on, the Calibration and Diagnostics property page appears.

Extended Diagnostics. Extended diagnostics test the logic analyzer more thoroughly than the power-on diagnostics. The extended diagnostics test the modules in the benchtop mainframe as well as the modules in the expansion mainframe(s). You can use the extended diagnostics to isolate problems to an individual module.

Before running the extended diagnostics, disconnect any attached probes.

NOTE. *Some items in the extended diagnostics menu will fail if a module is running. Stop all modules before performing the extended diagnostics.*

TLA Mainframe Diagnostics. The TLA mainframe diagnostics program is a stand-alone Windows application. These diagnostics check operation of the mainframe beyond the basic PC circuitry. These diagnostics also check the front panel knobs of the portable mainframe.

Expansion Mainframe Diagnostics. At power-on, the expansion mainframe runs two power-on diagnostics: “Power, Cables A & B and config”, and “Cable C Connection Test”.

If either of these power-on diagnostics fail, none of the modules associated with the expansion mainframe, and the expansion mainframe , will be recognized. The result will be as if the expansion mainframe were not connected.

Turn off the mainframes. Remove the two blue expansion cables and the gray expansion cable. Examine the connectors for bent or missing pins. Reconnect the two blue expansion cables and the expansion cable, and tighten the two connector screws. Turn on the mainframes and run the diagnostics again.

CheckIt Utilities. The CheckIt Utilities is a separate Windows application located in the Windows Start Programs menu. The diagnostics check the basic PC operations of the controller. (Earlier versions of the logic analyzers used QA+Win32 diagnostics.)

Software Problems

Your logic analyzer comes with most software installed. Before running any of the diagnostics, you should check the online release notes to verify that the logic analyzer software is compatible with the module firmware.

Many software problems can be due to corrupted or missing software files. In most cases the easiest way to solve software problems is to reinstall the software and follow the on-screen instructions. Refer to *Upgrading Software* for instructions on reinstalling or upgrading software.

Refer to Table H–1 on page H–10 for a list of software and hardware trouble-shooting information and recommended action. Note that this table can be used to identify problems for the entire Tektronix logic analyzer family.

If you suspect problems with the application software, contact your local Tektronix representative.

Hardware Problems

If you are certain that you have installed the logic analyzer correctly, run the extended diagnostics (located under the System menu) to identify any problems.

If your logic analyzer powers up so that you have access to the desktop, run the CheckIt Utilities software to identify possible controller hardware problems.

You can also run the external TLA mainframe diagnostics to identify problems not covered by other diagnostics. The TLA mainframe diagnostics are located under the Start menu under the Tektronix Logic Analyzer programs.

Check for Common Problems

Use Table H–1 to help isolate problems. This list is not exhaustive, but it may help you eliminate problems that are easy to fix, such as an open fuse, loose cable, or defective module (TLA700 series).

CAUTION. *To avoid damaging the instrument, do not install or remove any modules while the instrument is turned on.*

Table H-1: Failure symptoms and possible causes

Symptom	Possible causes and recommended action
Instrument does not turn on.	Verify that all power cords are connected to the instrument and to the power source. Check that the instrument receives power when you press the On/Standby switch. Check that fans start and that front-panel indicators light. Check that power is available at the power source. Check for failed fuses. Instrument failure: contact your local Tektronix service center.
Expansion mainframe does not turn on.	Verify that all power cords are connected to the expansion mainframe and to the power source. Check that all of the expansion modules are firmly seated, and that the mounting screws on the expansion modules are tightened. Check that the cables between the mainframe and the expansion mainframe are correctly connected: A → A, B → B, and C → C. Check that the expansion module is in slot 0 of the expansion chassis. Check that power is available at the power source. Check for failed fuses. Expansion mainframe failure: contact your local Tektronix service center.
Monitor does not turn on.	Check the monitor power cord connection. Check for failed fuse. Monitor failure: contact the vendor of your monitor for corrective action.
Monitor display is blank.	Check that the monitor is connected to the mainframe; replace the cable if necessary. If instrument display is blank, try connecting an external monitor; if both displays are blank, contact your local Tektronix service center. External monitor controls turned down; adjust monitor controls for brightness and contrast. Verify that the monitor is connected to the correct video port on the instrument. Check the controller BIOS setups for the monitor. Faulty monitor; contact the vendor of your monitor for corrective action.

Table H-1: Failure symptoms and possible causes (Cont.)

Symptom	Possible causes and recommended action
Instrument turns on but does not complete the power-on sequence.	If the instrument is a TLA700 series, turn off the instrument and check that all of the modules are fully inserted. If the mainframe is a benchtop mainframe, check the status of the SYSTEM FAIL and TEST LEDs on the benchtop controller. If either LED stays on, contact your local Tektronix service center. Check the status of the READY and ACCESSED LEDs on the front panel of the application modules. The READY LED turns on when the module passes the power-on diagnostics and when the module is ready to communicate with the controller. The ACCESSED LED turns on any time the controller accesses the module. Check for disk in floppy disk drive; make sure mainframe boots from the hard disk drive. Check for faulty module. Remove modules one at a time and turn on the instrument. If the instrument completes the power-on sequence, replace the faulty module. Possible software failure or corrupted hard disk; see *Software Problems* at the beginning of this chapter.
Power-on diagnostics fail.	Isolate problem to a faulty mainframe or to a faulty module. Multiple diagnostic failures across modules indicate a faulty mainframe. Diagnostic failures confined to an single module most likely indicate a faulty module. Contact your local Tektronix service center.
Instrument does not recognize accessories such as monitor, printer, or keyboard	Check that accessories are properly connected or installed. Try connecting other standard PC accessories or contact your local Tektronix service center.
LA Module merge not allowed in TLA700 Application.	Merge cable between LA modules not installed. LA modules are not compatible: TLA7Nx and TLA7Px LA modules may not be merged with TLA 7Lx and TLA7Mx LA modules. Refer to the Merge Rules on page E-1.
Windows comes up but the TLA or pattern generator application does not.	Instrument not set up to start the TLA application at power-on. Start application from the desktop, by double-clicking on the TLA Final Setup icon located on your desktop. Faulty or corrupt software. Reinstall the application software.
Windows comes up in Safe mode.	Exit the Safe mode and restart the instrument. Incompatible hardware and hardware driver software. Either install hardware driver or remove the incompatible hardware.
Application starts but modules do not display in System window.	Module firmware has not been updated. The flash jumper was not removed after the module firmware was updated. Turn off instrument off and check that all modules are fully inserted. Module address switches not set correctly. Turn the instrument off and remove module. Set address switches to FF and reinstall module. Module failure; replace with known-good module or contact your local Tektronix service center. Instrument failure; contact your local Tektronix service center. Automatic merging sometimes looks like a missing module.

Table H-1: Failure symptoms and possible causes (Cont.)

Symptom	Possible causes and recommended action
Expansion mainframe is not recognized by the system. Expansion mainframe does not show up in the system window.	Note: If there is no DSO or LA module installed in the expansion mainframe, the expansion mainframe will not show up in the System window. If modules are installed, follow these instructions: Turn off the mainframe(s). Check that both of the TLA7XM expansion modules are firmly seated, and that the mounting screws on the TLA7XM expansion modules are tightened. Remove the two blue expansion cables and the gray expansion cable. Examine the connectors on the cables for bent or broken pins. Examine the connectors on the expansion mainframe. Reconnect the two blue expansion cables and the gray expansion cable and tighten the screws on the connectors. Verify that the cables are not crossed; verify that the cables are connected: A → A, B → B, and C → C. Power on the benchtop mainframe and the expansion mainframe(s). (The mainframe power must be recycled in order for the ResMan32 (resource manager) application to correctly configure.) Expansion mainframe failure; contact your local Tektronix service center.
Expansion mainframe is recognized by the system, but installed modules are not.	Turn off the benchtop mainframe. Turn on the benchtop mainframe. The mainframe power must be recycled in order for the ResMan32 (resource manager) application to correctly configure. Module address switches not set correctly. Turn off the benchtop mainframe and remove the module(s) from the expansion mainframe. Set address switches to FF and reinstall module. Turn off the benchtop mainframe, install a known good module from the benchtop mainframe into the expansion mainframe (the expansion mainframe where the modules were not recognized). Turn on the benchtop mainframe and retry. Module failure; contact your local Tektronix service center.
Portable mainframe will not turn off with On/Standby switch.	The mainframe utilities may be set up to disable hard power-off. Check the setting of the mainframe utilities (the mainframe utilities are located in the Windows Control Panel). This is a Windows operating system problem. Try turning off the instrument using the Windows shutdown procedure. If the instrument still does not turn off, disconnect power cord and reconnect after 10 seconds to reboot the instrument.
Expansion Mainframe will not turn off with On/Standby switch.	If the expansion mainframe was incorrectly shut down (for example, the power cord was disconnected while the expansion mainframe was running), the expansion mainframe utility still registers the expansion mainframe as in the powered on condition. To correct this condition, press and hold the expansion mainframe power switch for three to four seconds. The expansion mainframe will turn off on its own. Power off the benchtop mainframe. Power on the benchtop mainframe; the expansion mainframe will turn on normally.

Startup Sequence

The following information is intended to provide troubleshooting hints in case the logic analyzer fails to complete the startup sequence. Refer to Figure H–1 on page H–14 while reading the following paragraphs.

At power-on, the mainframe software starts the mainframe and module kernel tests. If the mainframe passes the kernel tests, it begins to boot the Windows operating system. If the mainframe fails the kernel tests, it displays the error code(s), beeps, and terminates the startup sequence.

The Windows operating system starts the resource manager. The resource manager (ResMan32) performs the following tasks:

- Runs mainframe power-on self tests.
- Runs expansion mainframe power-on self tests.
- Verifies the power-on self test status.
- Inhibits any failed modules.
- Records the power-on self test failures.
- Determines the logic analyzer configuration.
- Executes the system controller power-on diagnostics.

After completing all of the preceding tasks, the logic analyzer starts the TLA application which performs the following tasks:

- Runs power-on diagnostics on all installed modules.
- Runs power-on diagnostics on the TLA system.
- Records the Pass/Fail status in the Calibration and Diagnostics property sheet.

If no failures occur, the application is ready to use for regular tasks.

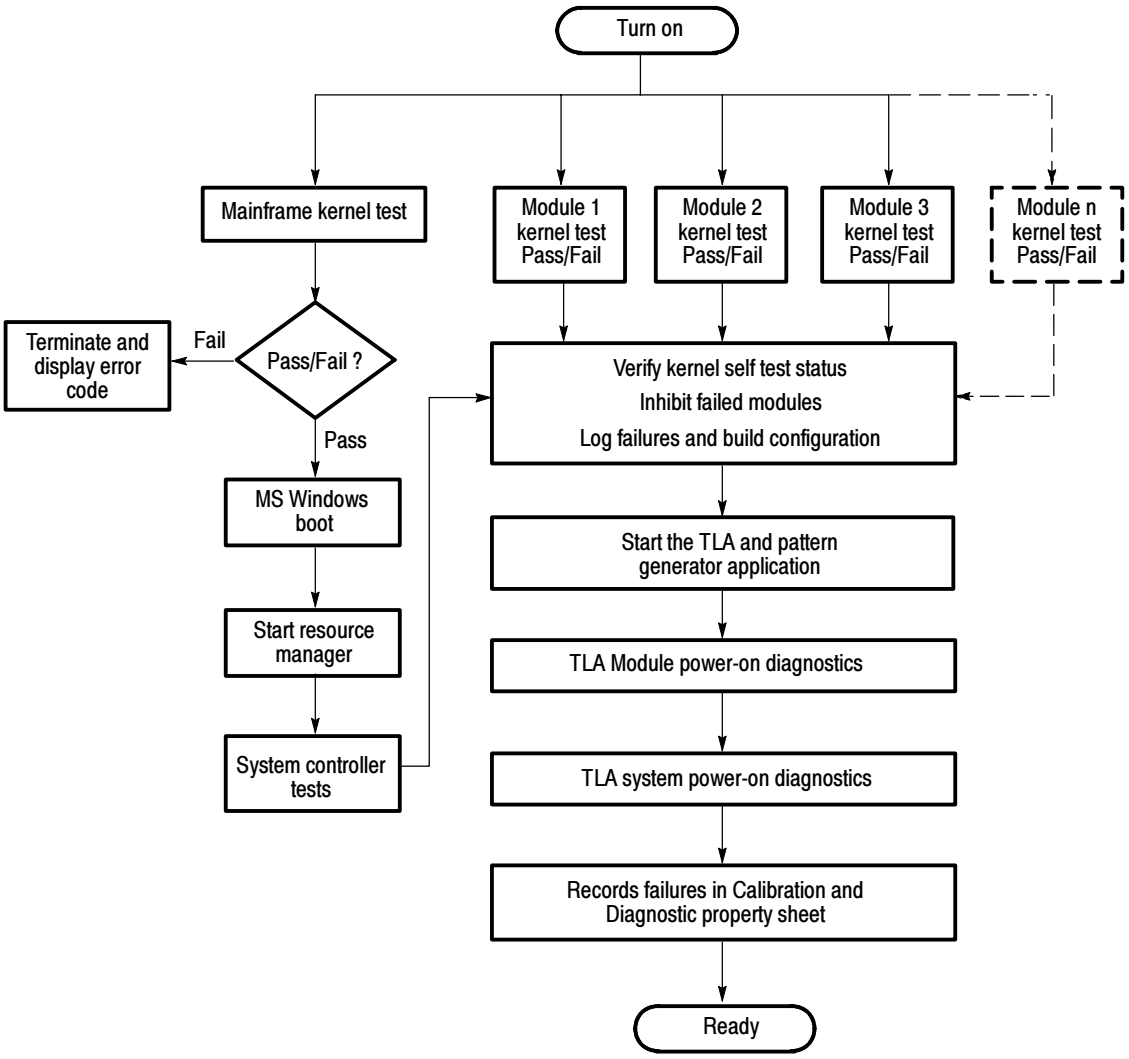

Figure H-1: TLA startup sequence

Isolating Problems

If you have completed all the troubleshooting procedures up to this point and the application fails to display any modules in the System window, you may have a system problem. Although most of the following steps apply to the TLA700 series, some of the steps may also be helpful in identifying problems with the TLA600 series.

- Verify that all modules are properly installed in the mainframe.
- Verify that the module address switches are set correctly. Power off the instrument and remove the modules. Set the address switches to FF and reinstall the modules.
- Verify that the modules do not have the flash programming jumper installed on the rear of the module. Power off the instrument and remove the modules. Remove the jumper and reinstall the modules.
- Try placing a suspected module in a different slot to verify slot dependency problems. For example, if you have a module in one set of slots, power off the instrument, move the module to a different set of slots, and then try the tests again. If the module works in the new location, you have identified a faulty slot in the instrument.
- Check for bent or broken pins on the backplane of the instrument.

You can execute the internal resource manager program (ResMan32.exe) to identify if any of the installed modules are being identified in the instrument slots. Table H–2 lists some of the command line options for executing the ResMan32 software.

Table H-2: Command line options for ResMan32

Option	Description
-a, -A, -o ,-O	ResMan32 will not close the text window after executing and displaying the results the major functions (default).
-p, -P	ResMan32 will not execute the mainframe power-on self test diagnostics (default).
-v, -V	ResMan32 records the resource manager actions in the text window in a short form or nonverbose mode.
+a, +A, +o ,+O	ResMan32 will terminate the tests and display the resultant action information in the text window.
+p, +P	ResMan32 will perform the mainframe power-on self test diagnostics.
+v, +V	ResMan32 records all actions in a text window in the verbose mode (default).

Table H-2: Command line options for ResMan32 (Cont.)

Option	Description
+t, +T	ResMan32 will not display the text window and the tests will terminate after executing regardless of the error conditions.
+m, +M	ResMan32 displays in a minimized window.

Complete the following steps to start the ResMan32 software:

1. Exit all applications.
2. Click the Windows Start button and select Run.
3. In the dialog box enter the following path:

   C:\Program Files\TLA700\System\ResMan32.exe

4. Click OK.

   The ResMan32 (resource manager) program will check all of the installed modules and their address locations. The program will print out data similar to that in Figure H-2. In this example the mainframe has two logic analyzer modules installed.

   If resource manager encounters any errors (such as an unsupported module), the resource manager will stop further communications and display information on why or at what point the module was disabled.

```
Auto Exit - Off
Identify Static Configure Devices
                Found a device at LA 1
                Found a device at LA 2
Identify Dynamic Configure Devices
Finding expansion devices
Matching Devices to Slots
Configuring slots for 2 instruments ...
                match la=1 to slot=1 in frame=0
                match la=2 to slot=3 in frame=0
Checking device self test
Setting VISA Attributes
      la 1, slot 1: device_class 2, manf_id 0xffd, model_code 0x7eb, addr_spc 0
      la 2, slot 3: device_class 2, manf_id 0xffd, model_code 0x7f4, addr_spc 0
Setting VISA Address Maps
      A24 device @ la 1 - reqmem:7
      A24 device @ la 1 - starting address 200000x, size 65536
      A24 device @ la 2 - reqmem:7
      A24 device @ la 2 - starting address 210000x, size 65536
Enabling Events & Responses
                Default IRQ for system: 4
                la 1: Int ID 1 assigned to IRQ 4
                Enabling Events: 8-9 16-32 47-63 124-125 127
                la 1: Asynchronous Enable succeeded
                                **Responses are unsupported by this device
                la 2: Int ID 1 assigned to IRQ 4
                Enabling Events: 16-32 124-125 127
                la 2: Asynchronous Enable succeeded
                                **Responses are unsupported by this device
Begin Normal Operation
   slot 1, LA 1, started successfully
   slot 3, LA 2, started successfully
VISA Data
      Frame 0, Slot 01:  la_1=1,1,4093,2027,2,0,1,7,2097152
      Frame 0, Slot 03:  la_2=2,3,4093,2036,2,0,1,7,2162688
```

Figure H-2: Example ResMan32 program output

Expansion Mainframe Problems

Because the expansion mainframe adds a level of complexity to troubleshooting problems, this section will concentrate on tips to aid you in troubleshooting expansion mainframe related problems.

If you have exhausted all of the failure symptoms and possible causes listed in Table H–1 beginning on page H–10, try some of the following tips.

Look and Listen for the Expansion Mainframe Power-On Sequence. There are certain signs that the expansion mainframe is not powering up correctly. By looking at and listening to these signs you can determine if the expansion mainframe is not powering up due to missing signals from the expansion module.

Upon powering up the benchtop mainframe, the expansion module sends a signal from the benchtop mainframe to the expansion module in the expansion mainframe via the three expansion cables. If the expansion mainframe does not receive this signal, the expansion mainframe will not power up.

If the poweron signal is received by the expansion mainframe, the fan starts and the lamp on the mainframe lights. Further indications that the mainframe receives signals from the expansion module are blinking lights on the expansion module and on other installed modules.

Substitute a Known Good Expansion Module. If you have a known good expansion module, try the following procedure:

1. Verify that the expansion module is installed in slot 0 and that the logical address switches on the back of the module are set to FF.
2. Try swapping the expansion module from the benchtop mainframe with the expansion module from the expansion mainframe. This sometimes works because one module is a sender while the other module is a receiver.

CAUTION. *To ensure expansion module full seats in the mainframe, do not use the mounting screws to engage the module into the backplane of the chassis. The single-wide expansion module requires up to 60 lbs. of insertion force to engage it into the backplane.*

The mounting screws will not provide enough force to seat the expansion module, and you can easily strip the threads.

3. Install the known good expansion module in slot 0 of the expansion chassis.
4. Power on the benchtop mainframe and check for normal operation.
5. If the failure symptoms are still present with the known good expansion module, the problem is most likely in the expansion mainframe.

6. If your expansion mainframe operates normally with the known good expansion module, then the suspect expansion module needs to be serviced.

Check the Expansion Mainframe. If you do not have a known good expansion module, perform the following procedure:

1. Remove all modules from the expansion mainframe except the for the expansion module.
2. Power on the benchtop mainframe and determine if the expansion mainframe is recognized by the instrument.

Replace the Expansion Module with a Benchtop Controller Module. Make the expansion mainframe simulate a benchtop mainframe. Do this by removing the expansion module from the slot 0 position in the expansion mainframe and replacing it with a known good benchtop controller module from the benchtop mainframe.

Because the expansion mainframe is set up to power on from a signal from the expansion module (which is no longer present) you need to press the On/Standby switch on the expansion mainframe.

If the expansion mainframe powers on correctly, the problem can be isolated to either the expansion module(s) or to the expansion cable(s).

Repacking for Shipment

If a mainframe or module is to be shipped to a Tektronix field office for repair, attach a tag to the mainframe or module showing the owner's name and address, the serial number, and a description of the problem(s) encountered and/or service required. Always include the module and the probes so that the entire unit can be tested.

When packing an instrument for shipment, use the original packaging. If it is unavailable or not fit for use, contact your Tektronix representative to obtain new packaging.

Glossary

Glossary

AC coupling
A DSO mode that blocks the DC component of a signal but passes the dynamic (AC) component of the signal. Useful for observing an AC signal that is normally riding on a DC signal.

Acquisition
The process of sampling signals from input channels, processing the results, and displaying the data.

Active module
The module highlighted by the pointer in the System window.

Aliasing
The condition that occurs when data is sampled at a rate slower than the rate at which data changes. When this happens, misleading data is displayed because the instrument misses the changes in data that occurred between sample points. Data pulses that fall between samples meet the technical definition of a glitch and are stored and displayed as glitches. See also *asynchronous acquisition* and *glitch*.

For DSO data, the displayed waveform may appear to be untriggered and much lower in frequency. For complex waveforms, distortion occurs due to the impact of aliasing on the high-order harmonics.

All samples
A Histogram window term. The total number of data samples analyzed.

Arm
To specify when the module should begin looking for a trigger.

Assert
To cause a signal or line to change from its logic false state to its logic true state.

Asynchronous acquisition
An acquisition that is made using a clock signal generated internally by the logic analyzer. This clock is unrelated to the clock in the system under test, and you can set it to a different rate. You should use an asynchronous clock rate that is five to ten times faster than your data rate to avoid aliasing. See also *Aliasing*.

Attenuation
The degree the amplitude of a signal is reduced when it passes through an attenuating device such as a DSO probe or attenuator (the ratio of the input measure to the output measure). For example, a 10X probe attenuates, or reduces, the input voltage of a signal by a factor of 10.

Benchtop Chassis
A benchtop chassis is a benchtop mainframe without a benchtop controller installed.

Chassis
A chassis is a mainframe without a controller or expansion module installed.

Clause
A trigger program term. The combination of one or more events (If statements) or actions (Then statements). When the Event is satisfied, the action is performed. See also *State*.

Clock cycle
A clock sequence that includes both high- and low-going transitions.

Clock equation
The Boolean combination of events needed to generate a storage clock. You can define a variety of clock inputs and link them using Boolean operators. Data will be sampled and stored in memory only when this clock equation is true.

Clock qualification
The process of filtering out irrelevant data by combining an acquisition clock with one or more bus signals.

Clock qualifier
An external signal that acts as a gate for the acquisition clock. When the external signal is false, the acquisition clock is not allowed to load acquired data into the acquisition memory.

COFF file formats
The COFF (Common Object File Format) format contains a number of variations and extensions, such as ECOFF and XCOFF. This flexibility enables it to be used with a wide variety of different microprocessors. Some code-generation tool vendors also extend this format in nonstandard ways that may make their files unreadable by the TLA logic analyzers.

Color range symbols
Color range symbols define the beginning and ending group values where color is displayed.

Compression Footprint
A connectorless, solderless contact between the customer PCB and the

P6860 and P6880 Probes. Connection is obtained by applying pressure between the customer's PCB and the probe through a Z-axis elastomer.

Counter
A trigger program device that records occurrences of an event.

Cursors
Paired markers that you can use to make measurements between two data locations.

Custom clocking
Custom clocking is used only with microprocessor support packages. Custom clocking can enable and disable a variety of microprocessor-specific clock cycle types (such as DMA cycles).

Data differences
Highlighted data in a Listing or Waveform window that indicate that there are differences between the acquired data and saved data during a compare operation.

Data equalities
Highlighted data in a Listing or Waveform window that indicate that there are no differences between the acquired data and saved data during a compare operation.

Data sample
The data logged in during one occurrence (or one cycle) of the acquisition clock. A data sample contains one bit for every channel.

Data window
A window used to display acquired data. There are two types of data windows, Listing windows and Waveform windows.

DC coupling
A DSO mode that passes both AC and DC signal components to the DSO circuit. Available for both the trigger system and the vertical system.

Delta measurement
The difference between two points in memory. For example, the voltage difference between the two cursors in a selected waveform.

Demultiplex
To identify and separate multiplexed signals (for instance, some signals from a microprocessor). To separate different signals sharing the same line and organize those signals into useful information.

Digital real-time signal acquisition
A digitizing technique that samples the input signal with a sample frequency of four to five times the DSO bandwidth. Combined with sin(x)/x interpolation, all frequency components of the input up to the bandwidth are accurately displayed.

Digitizing
The process of converting a continuous analog signal such as a waveform to a set of discrete numbers representing the amplitude of the signal at specific points in time.

Don't care
A symbol (X) used in place of a numeric character to indicate that the value of a channel or character is to be ignored.

EasyTrigger program list
A collection of predefined trigger programs for the LA module. You can load an individual program into the Trigger window and modify it for your requirements.

Edge
A signal transition from low to high, or high to low.

Edge trigger
Triggering that occurs when the module detects the source passing through a specified voltage level in a specified direction (the trigger slope).

Event condition
Event conditions are a logical combination of trigger events within a single clause. If you set up a logical AND statement, all event conditions in the clause must be fulfilled before the clause can execute the action. If you set up a logical OR statement, any one of the event conditions can be fulfilled before the clause can execute the action.

Expansion Chassis
An expansion chassis is an expansion mainframe without an expansion module installed.

External clock
A clock external to the logic analyzer and usually synchronous with the system under test.

Internal signal
An internal communication line that can be set as a marker. An internal signal can be used as either an event or an action in a trigger program. When used as an event, the internal signal is tested for true/false value like any other event; when used as an action, the signal can simply be set or cleared as the result of a condition being satisfied.

Glitch
An unintentional signal that makes a transition through the threshold voltage two or more times between successive sample clock cycles. Noise spikes and pulse ringing are examples of glitches.

Ground (GND) coupling
A DSO coupling option that disconnects the input signal from the vertical system.

Histogram window
A data window used to observe the performance of software routines.

IEEE695 file format
This object file format refers to the IEEE695 specification. This format is used primarily by compilers for a wide variety of Motorola microprocessors and compatible microprocessors from other vendors. This format provides for the inclusion of column information in source symbols, but not all compilers use this capability.

Internal clock
A clock mode in which the sampling of input logic signals occurs asynchronously to the activity of the system under test.

Interpolation
Display method used to connect the sample points acquired and display them as a continuous waveform. The logic analyzer uses sin(x)/x interpolation to display DSO signals.

Linear generation
A Histogram window term. The histogram ranges are evenly distributed from the highest range boundary to the lowest range boundary.

Listing window
A data window used to observe the data flow in the system under test. The acquired data is displayed in a listing (tabular text) format.

Log generation
A Histogram window term. The histogram ranges are distributed over a logarithmic scale.

MagniVu
An acquisition technology enabled by the logic analyzers provides up to 1000 picosecond timing resolution on all channels and requires no additional probing.

MagniVu data
High-speed data stored in a special memory.

Matched samples
A Histogram window term. The total number of data samples analyzed that matched a defined range. These samples exclude any samples outside of the defined ranges.

Merge modules
To physically or logically join LA modules together to form a single module with greater channel width.

Microprocessor support
Optional microprocessor support software that allows the logic analyzer to disassemble data acquired from microprocessors.

Mnemonic disassembly
A display format for data acquired from a microprocessor or a data bus. A logic analyzer decodes bus activity and displays it in formats such as: cycle types, instruction names, and interrupt levels. Advanced forms of mnemonic disassembly can detect queue flushes, and provide a display that resembles the original assembly language source code listing.

Module
The unit that plugs into a mainframe, providing instrument capabilities such as logic analysis.

Module trigger (trigger)
A trigger specific to a single module. When a module trigger occurs, the module continues to acquire data until the specified amount of posttrigger data is acquired, and then stops.

OMF51 file format
This format holds symbolic information and executable images for a 8051 or equivalent microprocessor.

OMF86 file format
A file format that holds symbolic information and executable images for an 8086 or equivalent microprocessor. It is also used for code intended to run on 80286, 80386, or higher-level microprocessors in real or 8086-compatible mode.

OMF166 file format
This format holds symbolic information and executable images for the Siemens (Infinion) C166 microprocessor family, or equivalent microprocessor.

OMF286/386 file formats
These file formats hold symbolic informaton and executable images for 80286 80386, or equivalent microprocessors. They are also used for executable images intended to run on the 8086 or other microprocessors in the 80x86 families.

PCB
An acronym for Printed Circuit Board; also known as Etch Circuit Board (ECB).

PCMCIA
An acronym for Personal Computer Memory Card Industry Association.

Podlet
A circuit contained in a flex lead and attached to a probe that provides square-pin connections to the circuit under test for one data acquisition channel and a ground pin.

Pretrigger
The specified portion of the data record that contains data acquired before the trigger event.

Post trigger
The specified portion of the data record that contains data acquired after the trigger event.

Probe head
The end of the probe that connects to the target system.

Probe adapter
A microprocessor-specific lead set that connects the LA module probe to a target system.

Qualification gap
Qualification gaps indicate that data samples were not stored due to storage qualification or Don't Store trigger actions. In a Listing window, qualification gaps are indicated by a horizontal gray line. In a Waveform window, qualification gaps are indicated by a blank vertical gap.

Range recognizer
A trigger term. Use range recognizers to trigger the logic analyzer on ranges of data.

Record length
The specified number of samples in an acquisition.

Sample clock
The clock signal that determines the points in time when the module samples data. A sample clock can be set up to occur at regular intervals specified by an internal clock (asynchronous acquisition), or to occur when a Boolean expression combining an external clock and qualifier signals is "true" (synchronous acquisition).

Sample rate
The frequency at which data is logged into the logic analyzer.

Sampling
The process of capturing an input signal, such as a voltage, at a discrete point in time and holding it constant so that it can be quantized.

Skew
The relative time difference between input channels, specified in terms of one edge relative to another. Also, the misrepresentation of data caused by parallel channels with different propagation delays.

Source Synchronous Clocking
Clocking mode that sends a strobe signal with the data signal. Data is synchronized with the strobe signal instead of the clock signal.

Source Window
A data window where you can view the execution of source code.

Standby (STBY)
The off-like state when the instrument in not in use. Some circuits are active even while the instrument is in the standby state.

State
A trigger program term. A step in a trigger program, made up of one or more clauses. See also *clause*.

Storage qualification
The process of filtering out data that has been acquired but which you do not want to store in acquisition memory. This allows you to avoid filling up your module's acquisition memory with irrelevant data samples.

Symbolic range generation
A Histogram window term. The histogram ranges are defined in a range symbol file. The highest and lowest ranges depend on the maximum and minimum boundaries for the ranges defined in the symbol file.

Symbolic radix
A format that allows you to substitute mnemonics (names) for radix numbers in the Trigger and data windows.

Synchronous acquisition
An acquisition that is made using a clock signal generated external to the logic analyzer. This clock is usually the clock in the system under test. The external clock is usually synchronous with the system under test and may or may not be periodic.

System trigger (trigger all)
An overriding command to all modules that causes them to stop looking for a trigger, and to acquire their posttrigger data, regardless of whether they have been armed or have fulfilled their own trigger conditions. The system trigger also functions as the primary reference point for the entire data acquisition. In data windows, timing and location information is relative to the system trigger.

Time correlation
Tracking independent events captured by different modules and indicating how they relate to each other in time. Specifically, the chronological interleaving of data from different modules into a single display. Shows real-time interactions between independently clocked circuits.

Time stamp
A separate clock value stored with each acquisition cycle.

Timer
A trigger program device that records elapsed time.

Threshold voltage
The voltage to which the input signals are compared.

Trigger
An event or condition that leads to the end of an acquisition cycle. When started, the instrument continuously acquires data from a system under test until the trigger occurs. After triggering, the instrument continues to acquire data until the post-fill requirement is met.

Trigger position
Where the trigger resides in acquisition memory. Electing to place the trigger in the center of memory means that half of the acquisition consists of data that occurred after the trigger.

Trigger program
A series of conditions, similar to software code, that defines the data you want to capture and view. The trigger program also specifies actions for data events. The trigger program filters acquired data to find a specific data event or series of data events. The trigger program can accept information from other modules or send signals external to the logic analyzer.

TSF
TLA Symbol File (TSF) format (a text format). The TSF format is used by the logic analyzer when it exports symbol files.

Unassert
To cause a signal or line to change from its logic true state to its logic false state.

Waveform window
A data window used to observe timing relationships in the system under test. The acquired data is displayed as a series of waveforms.

Way station
An intermediate probe part used to connect the heads of the P6810 and P6880 Probes to a single ribbon cable.

Word recognizer
A trigger term. Word recognizers are specific patterns of data or words. Use word recognizers to trigger the logic analyzer on specific data combinations.

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