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Tektronix Logic Analyzers

TLA7Sxx Serial Analyzer Modules



Breakthrough Solutions for PCI Express Analysis

PCI Express 2.0 introduces new challenges for validation engineers. Time to market pressures require a solution that can quickly pinpoint problems. The TLA7Sxx Series serial analyzer modules provide an innovative approach to PCI Express validation that spans all layers of the protocol from the physical layer to the transaction layer.

For the first time, parallel and serial acquisition modules can be utilized in both the TLA7012 portable mainframe and the TLA7016 benchtop mainframe offering the highest degree of flexibility. Additionally, the TLA7Sxx Series serial analyzer modules have unsurpassed ability to capture and trigger on PHY layer events, whether problems exists during link training or while the link is going into or out of power management states. Complete support for LOs and L1 power management is critical as power saving techniques become more prevalent in system designs. The TLA7Sxx Series serial analyzer acquisition capability is complemented by analysis tools which provide protocol decode and error reporting capabilities.

Hardware developers, hardware/software integrators and embedded system designers will appreciate the tight integration with the Tektronix Logic Analyzer. Correlation with other system buses or general purpose debug signals uses the TLA common system timestamp. Elusive problems that may have been propagated from other system buses can be efficiently debugged in a single environment.

Coupled with the P67xx Series mid-bus probes engineers have flexible options for platform accessibility.

Features & Benefits

8/16 Channel Serial Analyzer Modules with 32M 8b/10b Symbols Memory Depth per Channel

2.5 Gb/s and 5 Gb/s Acquisition Speed for PCI Express 1.0 and PCI Express 2.0

Frequency Margining at 2.5 Gb/s +/– 10% or 5.0 Gb/s +/– 10%

Supports x1, x2, x4, x8, and x16 PCI Express Links

Sync to L0s within 12 FTS Packets (Typical)

Track 2.5 Gb/s to 5.0 Gb/s Data Rate Change

Dynamically Track Changes in Link Width

Powerful Trigger State Machine Spans all Layers of the Protocol (Physical, Data Link, and Transaction)

Hardware Filtering Extends Link Capture Time

Compression Probing System Provides Minimal Intrusion on Circuits

Internal or External Reference Clock with or without Spread Spectrum Clocking (SSC)

Protocol Decode and Error Reporting in Listing and Waveform Views

Real Time Link Status Indicators

Applications

PCI Express Validation for:

- Silicon Validation
- Computer System Validation
 Embedded System Debug and Validation



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► Characteristics

General

| Number | of | Channels |
|--------|----|----------|
| | | |

| bols per channel |
|--|
| pols per channel |
| |
| |
| resolution |
| but SSC (Spread Spectrum Clocking), External Reference Clock (100 MHz Hz) with or without SSC |
| |
| |
| |

Module Configuration Requirements

Bi-directional Link Width

| | x1 | x4 | x8 | x16 |
|---------|----|----|----|-----|
| TLA7S08 | 1 | 1 | 0 | 0 |
| TLA7S16 | 1 | 1 | 1 | 2 |

Input Characteristics (with P67xx probes)

Signaling

| olgrialing | | |
|--------------------|------------------------|--|
| Capacitive Loading | See P67xx Probe Manual | |
| Minimum data eye | See P67xx Probe Manual | |

Acquisition Characteristics (with P67xx probes)

General

| Dynamic link width switch latency consumes up to 48 symbols (typical) |
|---|
| FTS support consumes up to 12 FTS packets (typical) |

Filter Characteristics

| Logical Idle | |
|--------------|---|
| Ordered Sets | TS1, TS2, SKP, EIOS, FTS, EIEOS |
| DLLPs | Ack, Nak, PM, Vendor Specific, InitFC1, InitiFC2, UpdateFC |
| TLPs | MRd, MRdL, MWr, IORd, IOWr, CfgRd0, CfgWr0, CfgRd1, CfgWr1, Msg, MsgD, CpI, CpID, CPILk, CPIDLk |

Trigger Characteristics

| Ingger Characteristics | |
|--|---|
| Independent Trigger States | 8 |
| Maximum Independent If/then Clauses per State | 8 |
| Maximum Number of Events per If/Then Clause | 8 |
| Maximum Number of Actions per If/Then Clause | 8 |
| Maximum Number of Event Counters per State | 2 |
| Event Counter Range | 16-Bits |
| Number of TLP Packet Recognizers per link direction | 4 |
| Number of DLLP Packet Recognizers per link direction | 4 |
| Number of Sequence Recognizers | 4 |
| Number of Symbols per Sequence Recognizer | 16 |
| Number of Link Event Recognizers | 4 |
| Number of Global Counter/Timers | 4 |
| Trigger Event Types | Anything, TLP, DLLP, Sequence, Link Event, Counter, Timer |
| Trigger Action Types | Trigger, Trigger All Modules, Wait for System Trigger, Go To, Increment Counter, Decrement Counter, Reset Counter, Start Timer, Reset Timer, Reset and Start Timer, Stop Timer, Reset and Stop Timer, Set Signal Out, Clear Signal Out, Arm Module, Start Storage, Stop Storage, Do Nothing |
| Counter/Timer Range | 48-Bits (~5 days with 3.6 ns resolution) |
| Storage Control (data qualification) | by State (Start/Stop) |

Physical Characteristics

| | ті | TLA7S16 | | TLA7S08 | |
|------------|-------|---------|-------|---------|--|
| Dimensions | mm | in. | mm | in. | |
| Height | 262 | 10.3 | 262 | 10.3 | |
| Width | 61 | 2.4 | 61 | 2.4 | |
| Depth | 381 | 15 | 381 | 15 | |
| Weight | kg | lb. | kg | lb. | |
| Net | 2.45 | 5.40 | 2.345 | 5.17 | |
| Shipping | 6.505 | 14.34 | 6.445 | 14.21 | |

Ordering Information

TLA7Sxx Logic Analyzer Modules

TLA7Sxx Logic Analyzer Modules

Includes: Statement of Compliance, one-year warranty (return to Tektronix), and installation manual. Reference clock cable, reference clock jumper cable. Probes must be ordered separately.

| Module | | |
|---------|---|--|
| TLA7S16 | 16 channel Serial Analyzer module, 2.5 Gb/s and 5.0 Gb/s acquisition, 32M symbols depth per channel | |
| TLA7S08 | 8 channel Serial Analyzer module, 2.5 Gb/s and 5.0 Gb/s acquisition, 32M symbols depth per channel | |

Logic Analyzer TLA7Sxx Module Options

| · · · · · · · · · · · · · · · · · · · | |
|---------------------------------------|-----------------|
| Opt. 88 | Factory Install |
| Opt. LO | English Manual |
| Opt. L5 | Japanese Manual |
| Opt. L10 | Russian Manual |
| Opt. L99 | No Manual |

Logic Analyzer Probe Selection Guidelines

A flexible choice of logic analyzer probes is available for use with TLA7Sxx modules. Please see the logic analyzer probe data sheets for further information.

| TLA7Sxx Optional Accessories | | |
|------------------------------|-------------|--|
| Reference Clock Cable | 672-6285-00 | |
| Reference Clock Jumper Cable | 174-5392-00 | |

► TLA7Sxx Service Options

| F TLA75XX Service Options | | |
|------------------------------|--|--|
| Calibration Service 3 Years | | |
| Calibration Service 5 Years | | |
| Single Calibration | | |
| Repair Service 3 Years | | |
| Repair Service 5 Years | | |
| Product Installation Service | | |
| | Calibration Service 3 Years Calibration Service 5 Years Single Calibration Repair Service 3 Years Repair Service 5 Years | |

► TLA7Sxx Service Products

| TLA7Sxx Service Products | Repair Service Coverage |
|--------------------------|---|
| TLA7S08-R1PW | 1 Year Post Warranty |
| TLA7S08-R2PW | 2 Years Post Warranty |
| TLA7S08-R3DW | 3 Years (includes Product Warranty Period). 3 Year period starts at time of instrument purchase |
| TLA7S08-R5DW | 5 Years (includes Product Warranty Period). 5 Year period starts at time of instrument purchase |
| TLA7S16-R1PW | 1 Year Post Warranty |
| TLA7S16-R2PW | 2 Years Post Warranty |
| TLA7S16-R3DW | 3 Years (includes Product Warranty Period). 3 Year period starts at time of instrument purchase |
| TLA7S16-R5DW | 5 Years (includes Product Warranty Period). 5 Year period starts at time of instrument purchase |

Contact Tektronix:

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