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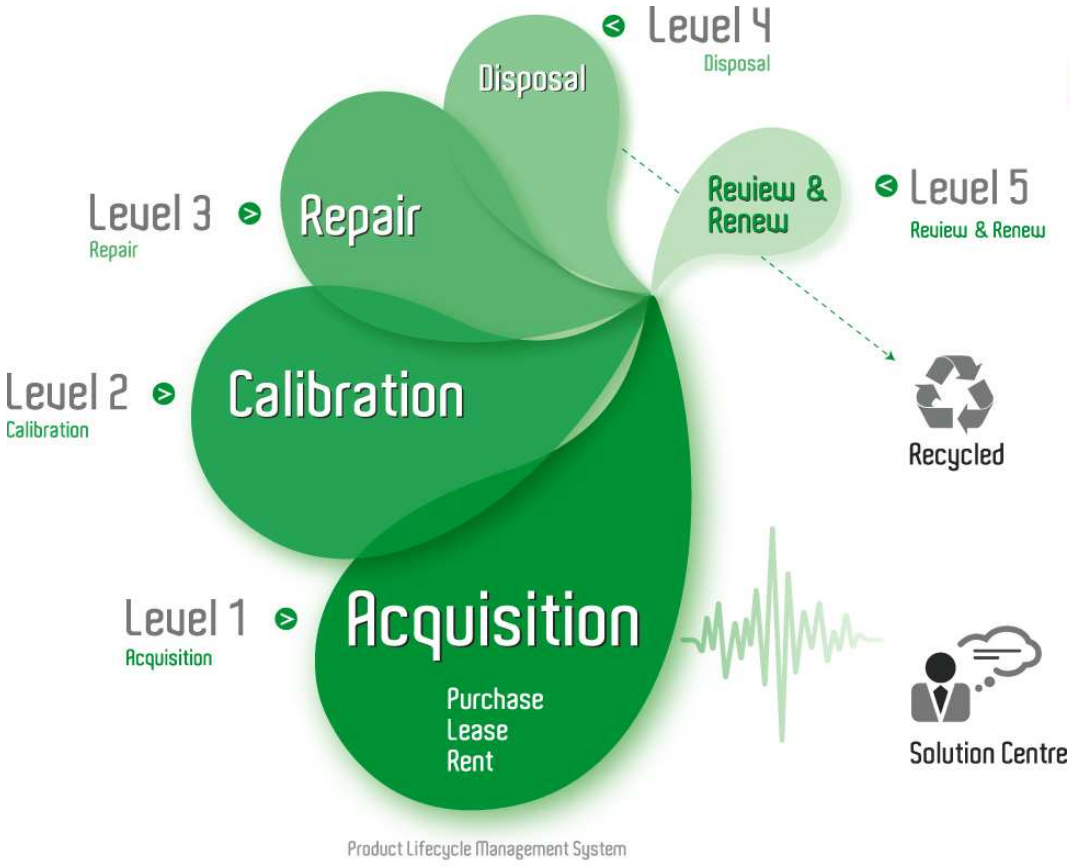

Instruction Manual

Tektronix

TMS805
RapidIO Bus Support

071-1081-01

www.tektronix.com

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

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Table of Contents

Getting Started

Operating Basics

Reference

Specifications

Index

List of Figures

List of Tables

Preface

This instruction manual contains specific information about the TMS805 RapidIO software support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating bus support packages on the logic analyzer for which the TMS805 RapidIO support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating bus support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of bus support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of logic analyzer online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the target system
- Setting up the logic analyzer to acquire data from the target system
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into packets and control symbols.
- The phrase “information on basic operations” refers to logic analyzer online help or a user manual, covering the basic operations of the bus support.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Contacting Tektronix

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Getting Started

Getting Started

This section contains information on the TMS805 RapidIO bus support, and information on connecting your logic analyzer to your target system.

Support Package Description

The TMS805 bus support package acquires, decodes and displays RapidIO bus cycles. The support package allows you to acquire bus cycles with minimal impact on the normal environment of the system.

The TMS805 software contains six support packages that you can load to handle the various combinations of bus widths and data rates. A description of each support package is listed here.

RIO8 The features of the RIO8 support package are:

- Supports 8-bit RapidIO bus implementations
- Clock rates from DC up to 375 MHz
- Data rates from DC up to 750 Mb/s
- Provides state, timing, triggering, and disassembly support
- Combined transmit and receive clocking (assuming a common crystal)
- 100% of trigger machine resources available
- Adjusts Setup/Hold time using AutoDeskew
- Real-time filtering of idle control symbols using EasyTriggers when acquiring either transmit or receive buses only

RIO16 The features of the RIO16 support package are:

- Supports 16-bit RapidIO bus implementations
- Clock rates from DC up to 375 MHz
- Data rates from DC up to 750 Mb/s
- Provides state, timing, triggering, and disassembly support
- Combined transmit and receive clocking (assuming a common crystal)
- 100% of trigger machine resources available

- Adjusts Setup/Hold time using AutoDeskew
- Real-time filtering of idle control symbols using EasyTriggers when acquiring either transmit or receive buses only

RIO8_T The features of the RIO8_T support package are:

- Supports 8-bit RapidIO bus implementations
- Clock rates from DC up to 500 MHz
- Data rates from DC up to 1 Gb/s
- Provides MagniVu and Analog Mux support

RIO16_T The features of the RIO16_T support package are:

- Supports 16-bit RapidIO bus implementations
- Clock rates from DC up to 500 MHz
- Data rates from DC up to 1 Gb/s
- Provides MagniVu and Analog Mux support

RIO8_34 The features of the RIO8_34 support package are:

- Supports 8-bit RapidIO bus implementations
- Clock rates from DC up to 375 MHz
- Data rates from DC up to 750 Mb/s
- Provides MagniVu and Analog Mux support
- Adjusts Setup/Hold time using AutoDeskew
- Acquires only transmit or receive buses but not both
- Provides state, timing, triggering, and disassembly support

RIO16_34 The features of the RIO16_34 support package are:

- Supports 16-bit RapidIO bus implementations
- Clock rates from DC up to 375 MHz
- Data rates from DC up to 750 Mb/s
- Provides MagniVu and Analog Mux support

- Adjusts Setup/Hold time using AutoDeskew
- Acquires only transmit or receive buses but not both
- Provides state, timing, triggering, and disassembly support

MagniVu Support. The RIO8_T and RIO16_T do not support state acquisition; however, you may view the data in MagniVu. MagniVu provides a waveform timing view with 125 ps between samples. MagniVu memory is 16 K samples deep. Special groups, Tx_Data and Rx_Data, have been created for the waveform display.

Analog Mux Support. Analog mux provides a way to use an external oscilloscope to view the analog features of the bus while the bus is being probed by the P6880 differential probes. For more information, refer to the information on basic operations.

Triggering Support. The RIO8, RIO16, RIO8_34, and RIO16_34 support packages contain a library of EasyTrigger programs to enable you to quickly trigger on common aspects of the RapidIO protocol. For RIO8, and RIO16 support packages, you can also use the EasyTriggers to filter idle control symbols in real-time.

Disassembly Support. The RIO8, RIO16, RIO8_34, and RIO16_34 support packages disassemble data acquired from the RapidIO bus. The salient features of these disassemblers are:

- Control symbol decoding and display of individual fields (physical layer)
- Packet decoding and display of individual fields for each protocol layer (physical, transport, and logical)
- Simultaneous decoding of both transmit and receive data buses (only for RIO8 and RIO16 support packages)
- Transaction level linking and operation level linking of request and response packets between the acquired transmit and receive buses (only for RIO8 and RIO16 support packages)
- Layer-level (physical, transport and logical) color highlighting in the mnemonics column
- Packet-style display using existing logic analyzer listing window architecture
- Identification and display of training patterns
- CRC computation and error detection

***NOTE**. Only RapidIO protocol tracking is performed. The disassembler does not attempt to perform packet payload decoding.*

To use this support package efficiently, refer to these documents:

- *RapidIO™ Interconnect Specification, Rev 1.1 3/8/2001*, developed by RapidIO Trade Association.
- *RapidIO™ Interconnect Specification Part V: Globally Shared Memory Logical Specification Rev. 1.1, 3/2001*

Logic Analyzer Software Compatibility

The label on the bus support CD-ROM states which version of logic analyzer software this support package is compatible with.

Logic Analyzer Configuration

The TMS805 support package allows a choice of required minimum module configurations.

The support packages, RIO8 and RIO16, require one 136-channel TLA7Axx module for each RapidIO port. This includes capture of both the transmit and the receive buses of the target port assuming a common clock crystal. Systems with unique clocks for the transmit and receive buses require two independent modules for simultaneous capture. The support packages, RIO8_34 and RIO16_34, require one 34-channel TLA7Axx module for acquiring either transmit or receive bus. Module acquisition speed depends on your requirements, but the TLA7Axx module speed is 450 MHz by default. This applies to both 8-bit and 16-bit buses.

For the RIO8 and RIO16 support packages, you need four P6880 high-density differential probes to probe an entire 16-bit RapidIO port and two probes to probe an entire 8-bit RapidIO port. If you need to probe only the transmit or receive half of the port, then you need two probes for a 16-bit bus and one probe for an 8-bit bus. For the RIO8_34 and RIO16_34 support packages, you need one P6880 high-density differential probe to probe either the transmit or receive half of the port for an 8-bit or a 16-bit RapidIO bus.

Requirements

Review the electrical specifications in the *Specifications* section in this manual as they pertain to your target system, as well as the following descriptions of TMS805 RapidIO support package requirements.

Hardware Reset If a hardware reset occurs in your system during an acquisition, the application disassembler might acquire an invalid sample.

Clock Rate The TMS805 RapidIO bus support package can acquire data from the RapidIO bus operating at 500 MHz[1] for timing only. The maximum rate for state acquisition is 375 MHz.

Setup/Hold Time Adjustments After loading the RIO8, RIO16, RIO8_34, and RIO16_34 support packages, AutoDeskew can be used to deskew and verify the logic analyzer Setup/Hold window. The adjustments are made for each channel. AutoDeskew can also be used to test for Setup/Hold violations of the current setting. For more information, refer to the section *Setup/Hold Time Adjustments* on page 2–25.

Nonintrusive Acquisition Acquiring RapidIO bus cycles is nonintrusive to the target system. That is, the TMS805 RapidIO support package does not intercept, modify, or present signals back to the target system.

Limitations of the Support

The TMS805 RapidIO support package has these limitations:

- Trigger libraries support only a 16 bit transport type (tt) field in the RapidIO protocol.
- Trigger libraries do not support extended address bits in logical packets of the RapidIO protocol.
- For combined transmit and receive capture, the transmit and receive bus clocks must be based on the same crystal. This ensures that the two clocks do not phase drift over time.
- The support package performs only RapidIO protocol tracking. The disassembler does not perform packet payload decoding. The support only identifies and displays payloads.
- The support package does not decode the first few acquired samples until and unless, the FRAME signals toggle (Tx_Frame must toggle for the transmitter and Rx_Frame must toggle for the receiver). Instead the message, "*** INSUFFICIENT DATA TO DISASSEMBLE ***" is displayed.

[1] **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

- When you start acquiring data from the middle of a packet, the packet is not decoded, until the FRAME signal toggles (Tx_Frame must toggle for the transmitter and Rx_Frame must toggle for the receiver). If the FRAME signal toggles indicating an embedded control symbol, this control symbol is decoded properly, but the continuation of the packet is treated as "UNKNOWN DATA".

Connecting the Logic Analyzer to a Target System

You can use the channel probes and clock probes to make the connections between the logic analyzer and your target system.

To connect the probes to TMS805 RapidIO signals in the target system, follow the steps:

1. Power off your target system. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the target systems, probes, and the logic analyzer module in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the target system.

2. Place the target system on a horizontal, static-free surface.
3. Use Tables 3–18 through 3–54 starting on page 3–17 to connect the channel probes to TMS805 RapidIO bus signals in the target system.

Labeling P6880 Probes

The TMS805 RapidIO bus support package relies on the channel mapping and labeling scheme for the P6880 Probes. Apply labels, using the instructions described in the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction* manual (Tektronix part number 071-1059-XX).

Operating Basics

Setting Up the Support

This section provides information on how to set up the software support and use clocking options.

The information in this section is specific to the operations and functions of the TMS805 RapidIO support package on any Tektronix logic analyzer for which the support can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and display disassembled data, you need to load the support package and specify the setups for clocking and triggering as described in the information on basic operations. The support package provides default values for each of these setups, but you can change the setups as needed.

Installing the Support Software

To install the TMS805 RapidIO software on your Tektronix logic analyzer, follow these steps:

1. Insert the CD-ROM in the CD drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the CD-ROM. A copy of the instruction manual is available on the CD-ROM.

To remove or uninstall software, follow the above instructions and select Uninstall. You need to close all windows before you uninstall any software.

Support Package Setups

The software installs six support packages. Each support package offers different clocking and display options.

Acquisition Setup. The TMS805 RapidIO support package consists of six different supports. You must make connections and load the appropriate support package. The support package affects the logic analyzer setup menus (and submenus) by modifying existing fields, and adding bus-specific fields. The six support packages that you can load are:

- RIO8
- RIO16
- RIO8_T
- RIO16_T
- RIO8_34
- RIO16_34

The TMS805 support adds these six selections to the "Load Support Package" dialog box, under the File pulldown menu.

Clocking Options

A special custom clocking program is loaded into the module every time you load one of the six support packages from the TMS805 RapidIO support package. Each support package offers different clocking options. You may use the default clocking options or choose an alternate by clicking the "More..." button in the logic analyzer setup window.

RIO8 Custom Clocking. The software provides four custom clocking options for RIO8 support:

- Tx and Rx (clocked by TCLK0). This option captures both transmit (Tx) and receive (Rx) buses. The transmit and receive buses are captured by the transmit clock (TCLK0). Both buses must operate at the same frequency. Setup/Hold values for data and frame signals on the Tx and Rx buses must be referenced to TCLK0.

- Tx and Rx (clocked by RCLK0). This option captures both transmit and receive buses. The transmit and receive buses are captured by the receive clock (RCLK0). Both buses must operate at the same frequency. Setup/Hold values for data and frame signals on the Tx and Rx buses must be referenced to RCLK0.
- Tx only (clocked by TCLK0). This option captures the transmit bus only. The transmit clock (TCLK0) is used to capture the bus. Setup/Hold values for data and frame must be referenced to TCLK0.
- Rx only (clocked by RCLK0). This option captures the receive bus only. The receive clock (RCLK0) is used to capture the bus. Setup/Hold values for data and frame must be referenced to RCLK0.

RIO16 Custom Clocking. The software provides eight custom clocking options for RIO16 support:

- Tx and Rx (clocked by TCLK0). This option captures both transmit and receive buses. The transmit and receive buses are captured by TCLK0. Both buses must operate at the same frequency. Setup/Hold values for data and frame signals on the Tx and Rx buses must be referenced to TCLK0.
- Tx and Rx (clocked by RCLK0). This option captures both transmit and receive buses. The transmit and receive buses are captured by the receive clock (RCLK0). Both buses must operate at the same frequency. Setup/Hold values for data and frame signals on the Tx and Rx buses must be referenced to RCLK0.
- Tx only (clocked by TCLK0). This option captures the transmit bus only. The transmit clock (TCLK0) is used to capture the bus. Setup/Hold values for data and frame must be referenced to TCLK0.
- Rx only (clocked by RCLK0). This option captures the receive bus only. The receive clock (RCLK0) is used to capture the bus. Setup/Hold values for data and frame must be referenced to RCLK0.
- Tx and Rx (clocked by TCLK1). This option captures both transmit and receive buses. The transmit and receive buses are captured by TCLK1. Both buses must operate at the same frequency. Setup/Hold values for data and frame signals on the Tx and Rx buses must be referenced to TCLK1.
- Tx and Rx (clocked by RCLK1). This option captures both transmit and receive buses. The transmit and receive buses are captured by RCLK1. Both buses must operate at the same frequency. Setup/Hold values for data and frame signals on the Tx and Rx buses must be referenced to RCLK1.
- Tx only (clocked by TCLK1). This option captures the transmit bus only. TCLK1 is used to capture the bus. Setup/Hold values for data and frame must be referenced to TCLK1.

- Rx only (clocked by RCLK1). This option captures the receive bus only. RCLK1 is used to capture the bus. Setup/Hold values for data and frame must be referenced to RCLK1.

***NOTE**. The first four clocking options give you the option of using an additional probe head to ease routing. The last four clocking options trade routing for minimal number of probe heads required.*

RIO8_34 and RIO16_34 Custom Clocking. The software provides one custom clocking option for the supports:

All cycles. This option captures either the transmit (Tx) or the receive (Rx) bus. Setup/Hold values for data and frame signals on the Tx or Rx buses must be referenced to the clock signal CLK0 for RIO8_34 and to CLK1 for RIO16_34.

Clocking State Machines (CSM)

The Clocking State Machine of each support package is described below:

RIO8 CSM. On a RapidIO bus, data is aligned to a 32-bit boundary. The acquisition module captures an 8-bit bus and performs a four-way demux to 32 bits. These 32 bits can match the RapidIO 32-bit boundary or be 50% out of phase. The RIO8 CSM ensures that the captured 32 bits match the RapidIO 32-bit boundary for both transmit and receive buses before storing the data.

RIO16 CSM. In the RIO16 support, the 32 bits of captured data (two-way demuxed from the 16-bit bus) always matches the alignment of the RapidIO 32-bit boundary. Therefore, the RIO16 CSM has only one state that stores data on every clock.

RIO8_34 CSM. On a RapidIO bus, data is aligned to a 32-bit boundary. The acquisition module captures an 8-bit bus and performs a four-way demux to 32 bits. The RIO8_34 CSM ensures that the captured 32 bits match the RapidIO 32-bit boundary before storing the data.

RIO16_34 CSM. In the RIO16_34 support, the 32 bits of captured data (two-way demuxed from the 16-bit bus) always matches the alignment of the RapidIO 32-bit boundary. Therefore, the RIO16_34 CSM has only one state that stores data on every clock.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The following information covers these topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Viewing cycle type labels
- Changing the way data is displayed

Acquiring Data

The TMS805 RapidIO software package installs six different supports: RIO8, RIO16, RIO8_T, RIO16_T, RIO8_34, and RIO16_34.

Once you load the support package, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help.

Viewing Disassembled Data

You can view disassembled data in RIO8, RIO16, RIO8_34, and RIO16_34 support packages in three display formats:

All
Packets & Symbols
Packets Only

The information on basic operations describes how to select the disassembly display formats.

***NOTE**. You must set the selections in the Disassembly property page correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2-11.*

If a channel group is not visible, you must use Add Column or Ctrl+L to make the group visible.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–1 shows these special characters and strings and describes what they represent.

Table 2-1: Description of special characters in the display

Character or string displayed	Description
>	Insufficient room on the screen to show all available data.
h	The values of different fields of all three layers are displayed in hexadecimal. This character is suffixed with the field value.

All Display Format

In this option the information pertaining to all the three layers along with payload and special messages are displayed. Figure 2–1 shows an example of the All display format for the RIO8 support package.

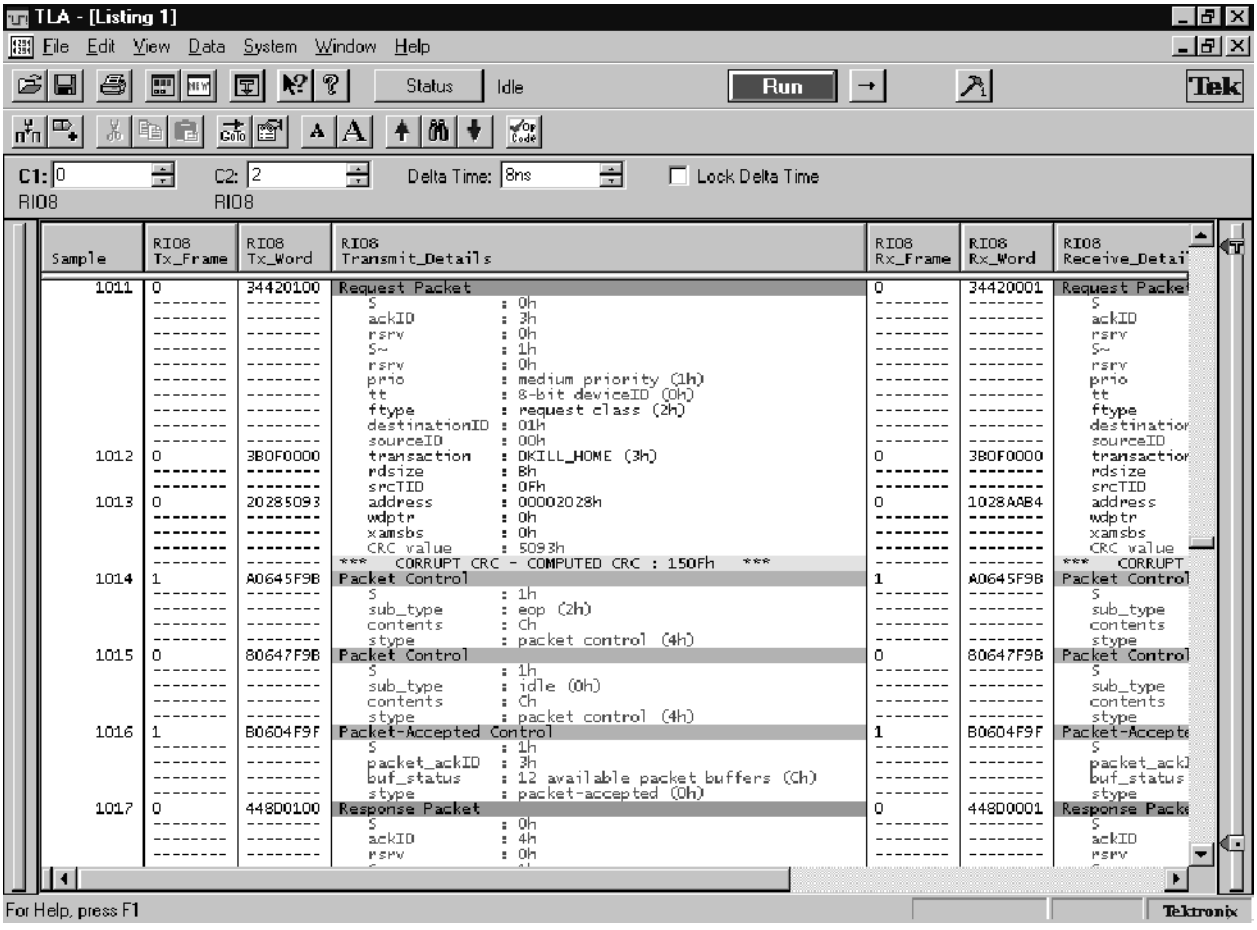


Figure 2-1: Example of All display format for the RIO8 support package

Figure 2-2 shows an example of the All display format for the RIO16 support package.

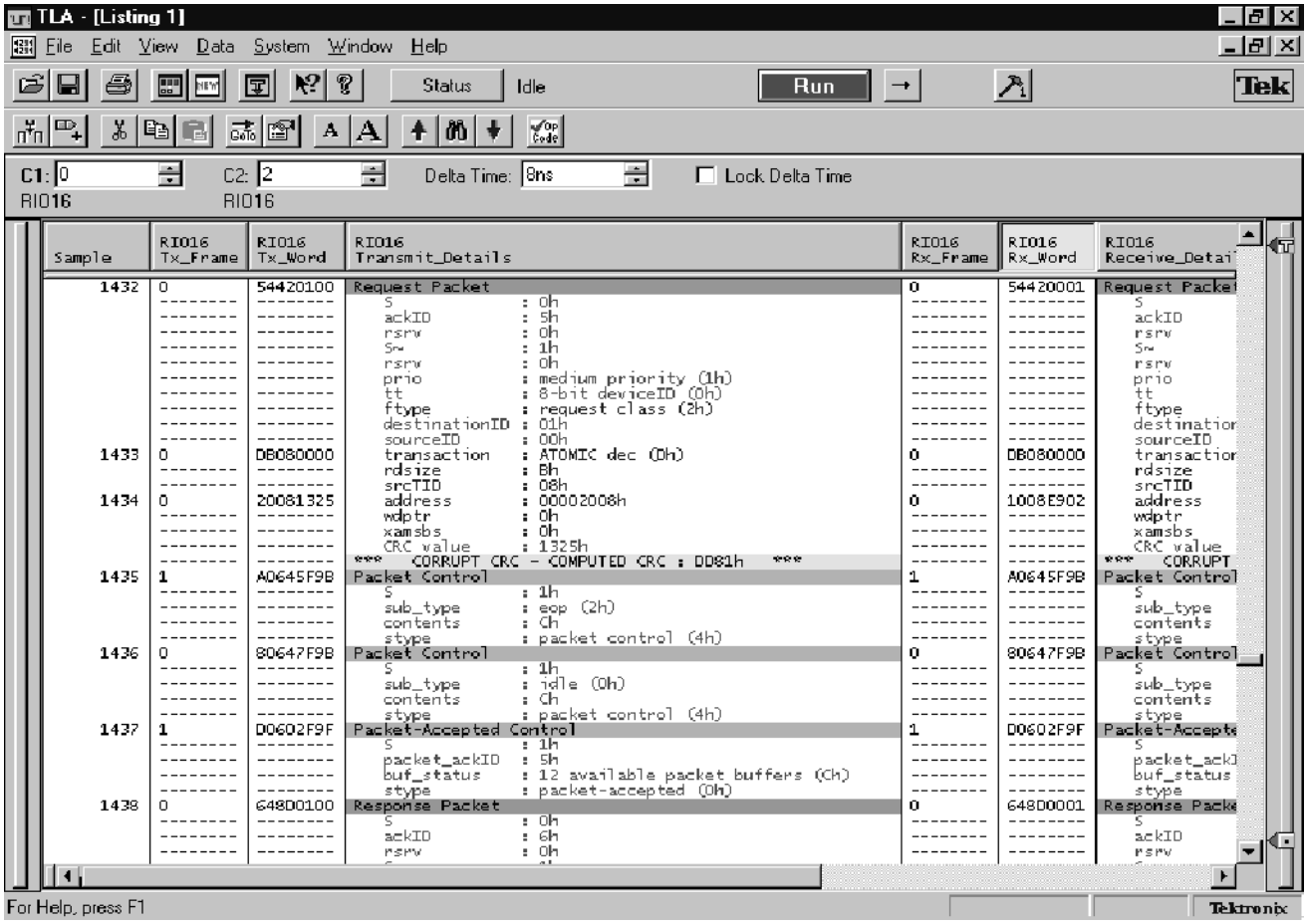


Figure 2-2: Example of All display format for the RIO16 support package

Packets & Symbols Display Format

The Packets & Symbols display format displays information about all packets, control symbols and special messages except the message "*** INSUFFICIENT DATA TO DISASSEMBLE ***". For more information on special messages, refer to the section *Special Messages* on page 2–11.

Packets Only Display Format

The Packets Only display format displays information about all packets and special messages except the message "*** INSUFFICIENT DATA TO DISASSEMBLE ***". The display format does not display control symbols. For more information on special messages, refer to the section *Special Messages* on page 2–11.

***NOTE**. The All Display Format has the highest priority followed by Packets & Symbols and Packets Only Display Formats. When Transmit and Receive buses are being simultaneously decoded and displayed, the cycle type labels and the special messages are displayed according to the display format priority.*

The training patterns are shown in all three display formats.

Example: In a sample, if the support displays a packet for a transmit bus and a control symbol for a receive bus, and you choose the Packets Only option, the control symbol on the receive side continues to be displayed.

Disassembled Data

During data disassembly, the support packages RIO8, RIO16, RIO8_34, and RIO16_34 follow these conditions:

- If the combination of "read data size (rdsize)" and the "word pointer (wdptr)" is reserved, then the number of payload bytes is assumed to be zero.
- If the combination of "write data size (wrsize)" and the "word pointer (wdptr)" is reserved, then the number of payload bytes is assumed to be zero.
- For Streaming-Write packet, the TMS805 support package assumes a data payload size of 256 bytes by default.
- The "address" field is displayed as a 32-bit value. The value of the address field is displayed only when all the 29 bits of this field are acquired.
- The value of the "extended address" field is displayed only when all the 16 bits (in case of a 16-bit ext_address field) or all the 32 bits (in case of a 32-bit ext_address field) of that field are acquired.
- The value of the "config_offset" field is displayed only when all the 21 bits of this field are acquired.
- The value of the "reserved" field in Maintenance Response packets is displayed only when all the 24 bits of this field are acquired.
- The value of payload data is displayed as 8 bits when the payload size is less than 8 bytes and displayed as 16-bits when the payload size is greater than 8 bytes.

Cycle Type Labels

The TMS805 RapidIO support decodes and displays the individual fields for the Physical, Transport and Logical layers of the protocol. These fields are displayed in colors that are unique for each layer. The Physical Layer fields are displayed in green. The Transport Layer fields are displayed in red. The Logical Layer fields are displayed in blue.

The Packet Name is highlighted in green. Table 2–2 shows the cycle type labels for the packet names.

Table 2-2: Cycle type labels for RapidIO packet names

Cycle type labels	Description
Implementation-Defined Request Packet	Type 0 Packet Name
Intervention-Request Packet	Type 1 Packet Name
Request Packet	Type 2 Packet Name
Reserved Request Packet	Type 3 Packet Name
Reserved Request Packet	Type 4 Packet Name
Write Packet	Type 5 Packet Name
Streaming-Write Packet	Type 6 Packet Name
Reserved Request Packet	Type 7 Packet Name
Maintenance Packet	Type 8 Packet Name
Reserved Request Packet	Type 9 Packet Name
Doorbell Packet	Type 10 Packet Name
Message Packet	Type 11 Packet Name
Reserved Response Packet	Type 12 Packet Name
Response Packet	Type 13 Packet Name
Reserved Response Packet	Type 14 Packet Name
Implementation-Defined Response Packet	Type 15 Packet Name

The Control symbol name is highlighted in cyan. Table 2–3 shows the cycle type labels for the control symbol names.

Table 2-3: Cycle type labels for control symbol names

Cycle type labels	Description
Packet-Accepted Control	Type 0 Control Symbol Name
Packet-Retry Control	Type 1 Control Symbol Name
Packet-Not-Accepted Control	Type 2 Control Symbol Name

Table 2-3: Cycle type labels for control symbol names (Cont.)

Cycle type labels	Description
Reserved Control	Type 3 Control Symbol Name
Packet Control	Type 4 Control Symbol Name
Link Maintenance Request Control	Type 5 Control Symbol Name
Link Maintenance Response Control	Type 6 Control Symbol Name
Reserved Control	Type 7 Control Symbol Name

The Training Patterns are highlighted in silver. Table 2–4 shows the cycle type labels for training pattern names.

Table 2-4: Cycle type labels for training pattern names

Cycle type labels	Description
Training Pattern	Indicates Training Pattern

The packet continuation name is highlighted in green. Table 2–5 shows the cycle type labels for packet continuation names.

Table 2-5: Cycle type labels for packet continuation names

Cycle type labels	Description
Implementation-Defined Request Packet Continues	Type 0 Packet Continuation
Intervention Request Packet Continues	Type 1 Packet Continuation
Request Packet Continues	Type 2 Packet Continuation
Write Packet Continues	Type 5 Packet Continuation
Streaming-Write Packet Continues	Type 6 Packet Continuation
Maintenance Packet Continues	Type 8 Packet Continuation
Doorbell Packet Continues	Type 10 Packet Continuation
Message Packet Continues	Type 11 Packet Continuation
Response Packet Continues	Type 13 Packet Continuation
Implementation-Defined Response Packet Continues	Type 15 Packet Continuation

Special Messages

This section gives information about the special messages used in the TMS805 software support. The disassembler uses special messages to indicate the following significant events. These messages are highlighted in yellow. Table 2–6 shows the special messages and their descriptions.

Table 2-6: Special messages and their descriptions

RapidIO special messages	Description
*** INSUFFICIENT DATA TO DISASSEMBLE ***	The very first few acquired samples are not decoded until and unless the FRAME signals toggle (Tx_Frame should toggle for the transmitter side and Rx_Frame should toggle for the receiver side). Instead this message will be displayed.
*** CORRUPT FIRST SYMBOL-(PARITY ERROR) ***	This message is displayed when the First Symbol of a packet fails the Parity Error Check.
*** CORRUPT SYMBOL-(PARITY ERROR) ***	This message is displayed when the first 16-bits of a Control Symbol do not match the next 16 complement bits.
*** UNKNOWN DATA ***	This message is displayed when the information present on the bus is not according to RapidIO protocol.
DATA : xxxxxxxxh (IMPLEMENTATION-DEFINED)	This message is displayed when you have more than 32 bits of type 0 and type 15 packets.
*** RESERVED DATA ***	This message is displayed when there are more than 32 bits of data for all types of reserved packets.
*** PAYLOAD TRUNCATED ***	This message is displayed whenever the “double-word” combination in not present for Type 6 (S-Write) packets.
*** CORRUPT CRC - COMPUTED CRC : xxxxh ***	This message is displayed whenever a mismatch occurs between the computed CRC and the CRC present on the bus.

Changing How Data is Displayed

Common fields and features allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the TMS805 RapidIO support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles

Optional Display Selections

Table 2–7 shows the logic analyzer disassembly display options.

Table 2-7: Logic analyzer disassembly display options

Description	Option
Show:	All (default) Packets & Symbols Packets Only
Highlight	None (default)
Disassemble Across Gaps:	Yes No (default)

Bus Specific Fields

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways. For the RIO8 and RIO16 supports, the submenu has the title:

RIO8 Controls
RIO16 Controls

Figure 2–3 shows the disassembly display options for the TMS805 RapidIO support package.

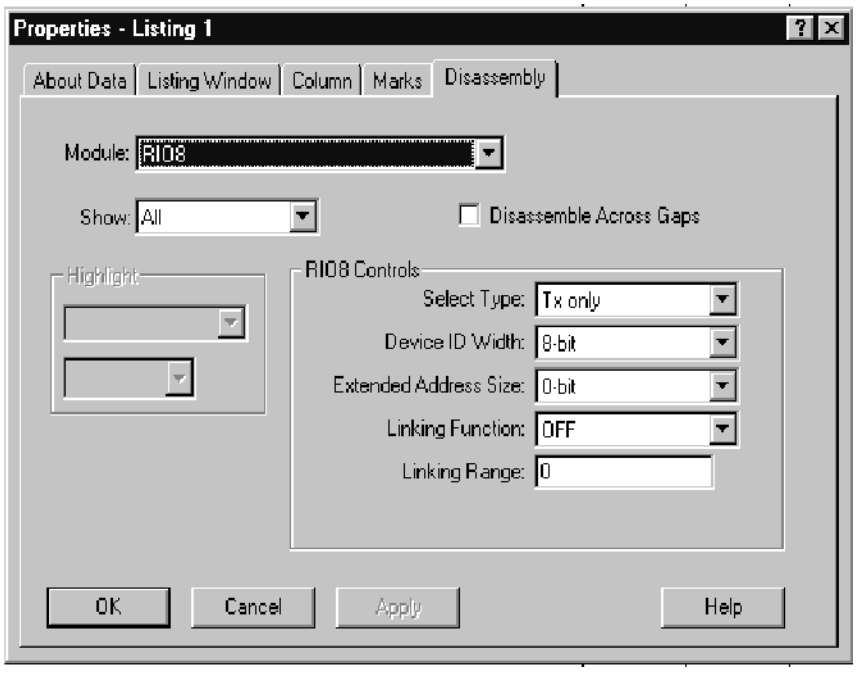


Figure 2-3: Disassembly display options

Select Type. Select the type of field for the device from one of the following:

Select Type: Tx Only (default)
Rx Only
Tx & Rx

Device ID Width. Select the field for transport type (tt) field value. Select one of the following options:

Device ID Width: 8 bit (default)
16 bit

Extended Address Size. Select the size of the extended address field. Select one of the following options:

Extended Address Size: 0 bit (default)
16 bit
32 bit

Linking Function. Select Linking Function to toggle the linking function on or off.

Linking Function: OFF (default)
ON

Linking Range. Enter the number of samples (a decimal value between 0 and 9999) to be linked. If you enter a value greater than 9999, then that value is replaced by 9999.

Linking Range: 0 (default)

NOTE*. The linking range specifies the number of samples from the Request Packet to the corresponding response packet or the corresponding control symbol containing the ID information. This option is also necessary for deciding the payload size. A detailed explanation is given in section* Linking Function *on page 2-21.*

Figure 2–4 shows the disassembly display options for the RIO8_34 and RIO16_34 support packages.

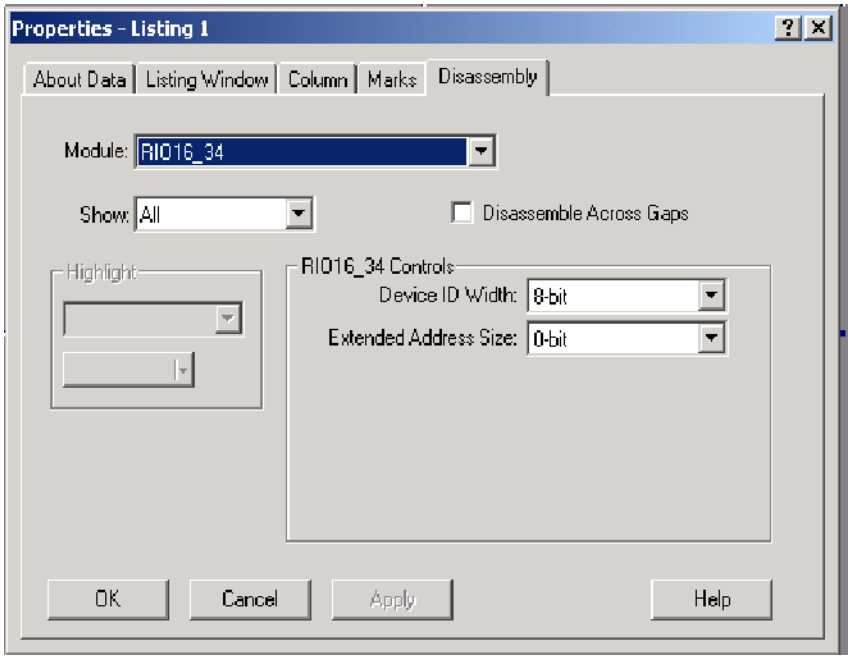


Figure 2-4: Disassembly display options for the RIO8_34 and RIO16_34 support packages

Device ID Width. Select the field for transport type (tt) field value. Select one of the following options:

Device ID Width: 8 bit (default)
16 bit

Extended Address Size. Select the size of the extended address field. Select one of the following options:

Extended Address Size: 0 bit (default)
16 bit
32 bit

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your CD-ROM to view an example of how the RapidIO bus cycles look when they are disassembled. Viewing this system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your target system.

Information on basic operations describes how to view the file.

Trigger Programs

This section describes how to load trigger programs. The RIO8, RIO16, RIO8_34, and RIO16_34 support packages contain a library of EasyTrigger programs to enable you to quickly trigger and qualify common aspects of the RapidIO protocol. Optionally, for RIO8_34 and RIO16_34, idle control symbols can also be filtered using EasyTriggers.

The TMS805 RapidIO support package installs trigger programs for each support in the following paths:

- Trigger Programs for the RIO8 support package are installed in the C:\Program Files\TLA700\Supports\RIO8\EasyTriggers folder.
- Trigger Programs for the RIO16 support package are installed in the C:\Program Files\TLA700\Supports\RIO16\EasyTriggers folder.
- Trigger Programs for the RIO8_34 support package are installed in the C:\Program Files\TLA700\Supports\RIO8_34\EasyTriggers folder.
- Trigger Programs for the RIO16_34 support package are installed in the C:\Program Files\TLA700\Supports\RIO16_34\EasyTriggers folder.

Loading Trigger Programs

To load a trigger program from any of the support packages, follow these steps:

1. Load the support package.
2. From the system window, click the 

Trigger button.

3. Figure 2–5 shows the window that opens.

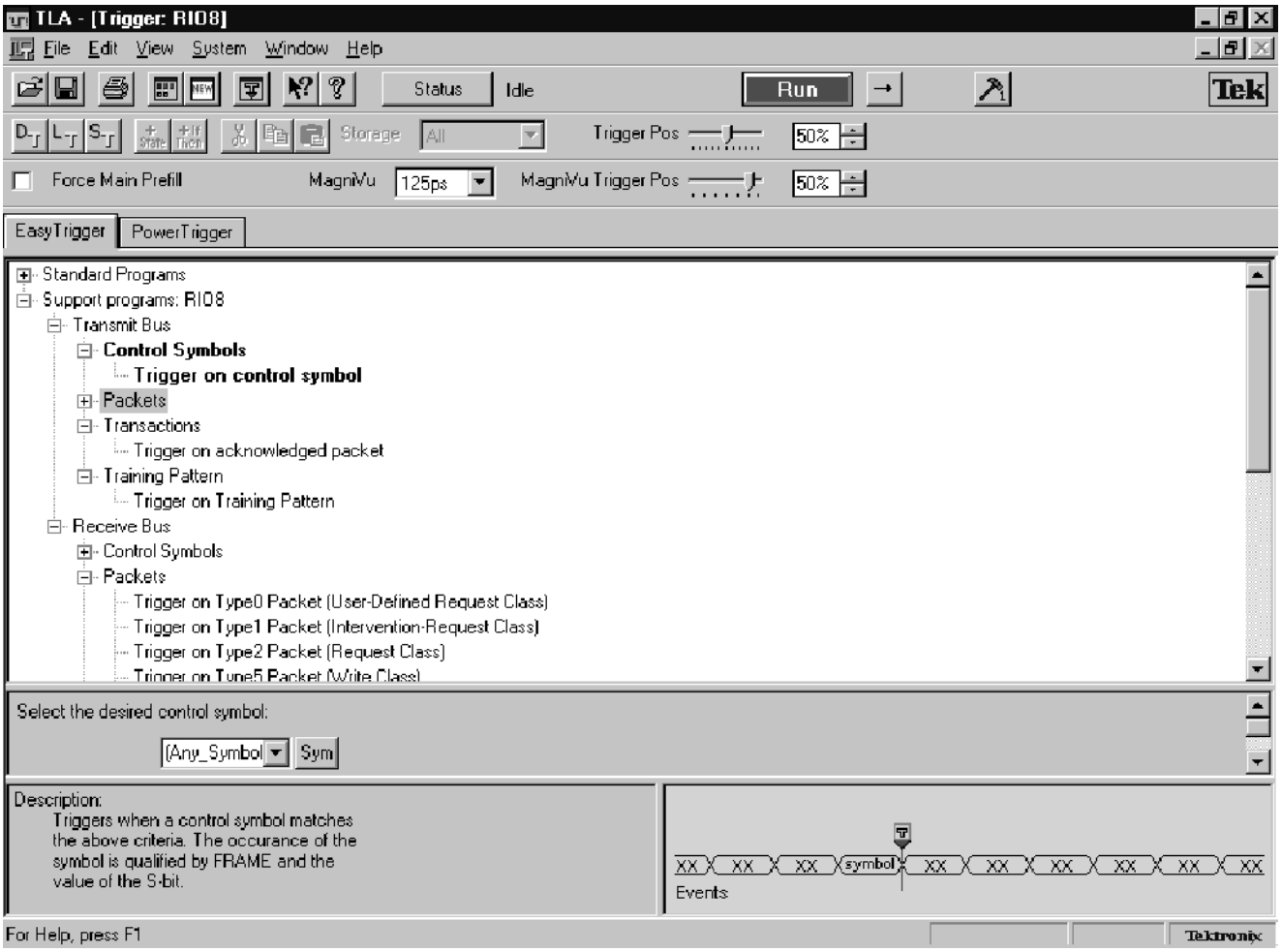


Figure 2-5: Loading trigger programs

4. Scroll through the EasyTriggers to find the trigger programs that you need.
5. Select an EasyTrigger program from the list and fill in the fields.

You are now ready to trigger on the acquired data.

For more information, refer to the logic analyzer online help and the logic analyzer user manual.

RIO8 Trigger Programs

The following is a list of EasyTrigger programs for the RIO8 support. Each of the EasyTriggers exists for both the transmit and receive side of the bus.

Trigger on control symbol
Trigger on Type0 Packet (User-Defined Request Class)
Trigger on Type1 Packet (Intervention-Request Class)
Trigger on Type2 Packet (Request Class)
Trigger on Type5 Packet (Write Class)
Trigger on Type6 Packet (Streaming-Write Class)
Trigger on Type8 Packet (Configuration Read Request)
Trigger on Type8 Packet (Configuration Read Response)
Trigger on Type8 Packet (Configuration Write Request)
Trigger on Type8 Packet (Configuration Write Response)
Trigger on Type8 Packet (Port Write Request)
Trigger on Type10 Packet (Doorbell Class)
Trigger on Type11 Packet (Message Class)
Trigger on Type13 Packet (Response without payload)
Trigger on Type13 Packet (Response with payload)
Trigger on Type13 Packet (Message Response)
Trigger on Type15 Packet (User-Defined Response Class)
Trigger on acknowledged packet
Trigger on Training Pattern

RIO16 Trigger Programs

The following is a list of EasyTrigger programs for the RIO16 support. Each of the EasyTriggers exists for both the transmit and receive side of the bus.

Trigger on control symbol
Trigger on Type0 Packet (User-Defined Request Class)
Trigger on Type1 Packet (Intervention-Request Class)
Trigger on Type2 Packet (Request Class)
Trigger on Type5 Packet (Write Class)
Trigger on Type6 Packet (Streaming-Write Class)
Trigger on Type8 Packet (Configuration Read Request)
Trigger on Type8 Packet (Configuration Read Response)
Trigger on Type8 Packet (Configuration Write Request)
Trigger on Type8 Packet (Configuration Write Response)
Trigger on Type8 Packet (Port Write Request)
Trigger on Type10 Packet (Doorbell Class)
Trigger on Type11 Packet (Message Class)
Trigger on Type13 Packet (Response without payload)
Trigger on Type13 Packet (Response with payload)
Trigger on Type13 Packet (Message Response)
Trigger on Type15 Packet (User-Defined Response Class)
Trigger on acknowledged packet
Trigger on Training Pattern

RIO8_34 Trigger Programs

The following is a list of EasyTrigger programs for the RIO8_34 support.

Trigger on control symbol
Trigger on Type0 Packet (User-Defined Request Class)
Trigger on Type1 Packet (Intervention-Request Class)
Trigger on Type2 Packet (Request Class)
Trigger on Type5 Packet (Write Class)
Trigger on Type6 Packet (Streaming-Write Class)
Trigger on Type8 Packet (Configuration Read Request)
Trigger on Type8 Packet (Configuration Read Response)
Trigger on Type8 Packet (Configuration Write Request)
Trigger on Type8 Packet (Configuration Write Response)
Trigger on Type8 Packet (Port Write Request)
Trigger on Type10 Packet (Doorbell Class)
Trigger on Type11 Packet (Message Class)
Trigger on Type13 Packet (Response without payload)
Trigger on Type13 Packet (Response with payload)
Trigger on Type13 Packet (Message Response)
Trigger on Type15 Packet (User-Defined Response Class)
Trigger on Training Pattern

RIO16_34 Trigger Programs

The following is a list of EasyTrigger programs for the RIO16_34 support.

Trigger on control symbol
Trigger on Type0 Packet (User-Defined Request Class)
Trigger on Type1 Packet (Intervention-Request Class)
Trigger on Type2 Packet (Request Class)
Trigger on Type5 Packet (Write Class)
Trigger on Type6 Packet (Streaming-Write Class)
Trigger on Type8 Packet (Configuration Read Request)
Trigger on Type8 Packet (Configuration Read Response)
Trigger on Type8 Packet (Configuration Write Request)
Trigger on Type8 Packet (Configuration Write Response)
Trigger on Type8 Packet (Port Write Request)
Trigger on Type10 Packet (Doorbell Class)
Trigger on Type11 Packet (Message Class)
Trigger on Type13 Packet (Response without payload)
Trigger on Type13 Packet (Response with payload)
Trigger on Type13 Packet (Message Response)
Trigger on Type15 Packet (User-Defined Response Class)
Trigger on Training Pattern

Linking Function

This section describes the Linking Function. The linking function provides transaction and operation level linking between the Request and the Response Packets. Transaction level linking occurs between the Request Packet and the corresponding Response Packet. Operation level linking occurs between the Request or Response Packet and the corresponding control symbol.

Linking is available only when the following disassembly options are selected and set to:

Select Type:	Tx & Rx
Linking Function:	ON
Linking Range:	values between 0–9999 (decimal)

The linking function is operational for:

- All Request Packets (except Reserved Request Packets) that have a corresponding Response Packet.
- All "Acknowledge Control Symbols" and the corresponding Request or Response Packet.
- All Request Packet (except Reserved Request Packets) in the Transmit_Details column linking is done between the corresponding Control Symbol Response and Response Packet in the Receive_Details column.
- All Request Packet (except Reserved Request Packets) in the Receive_Details column linking is done between the corresponding Control Symbol Response and Response Packet in the Transmit_Details column.

Two levels of linking — Forward Linking and Backward Linking, are performed between the Request Packets, Response Packets and intermediate Control Symbols.

***NOTE**. The Linking function is available only on RIO8 and RIO16 support packages.*

Forward Linking

This section describes Forward Linking for the TMS805 RapidIO support package.

Forward Linking Description

Forward Linking is performed between the Request Packet and the corresponding control symbol, and also between the Request Packet and the corresponding Response Packet. If Forward Linking fails, then the linking cycle type message given in Table 2–8 on page 2–23 is displayed.

Linking between the Request Packet and the intermediate Control Symbol. At every Request Packet (except Reserved Request Packet), the disassembly scans a fixed number of samples (defined by the Linking Range option) forward and tries to match the ackID fields in the Request Packet and the responding Control Symbol. If a match is found, the sample number of the responding Control Symbol is placed at the Request Packet.

Linking between the Request Packet and Response Packet. At every Request Packet (except Reserved Request Packet), the disassembly scans a fixed number of samples (defined by the Linking Range option) forward and tries to match the srcTID field in the Request Packet and the targetTID field in the Response Packets. If a match is found, the sample number and the "status" field information of the corresponding Response Packet is placed at the Request Packet.

Backward Linking

This section describes Backward Linking for the TMS805 RapidIO support package.

Backward Linking Description

Backward Linking is performed between the intermediate control symbol and the Request Packet or Response Packet, and also between the Response Packet and the Request Packet. If Backward Linking fails, then the linking cycle type message given in Table 2–8 on page 2–23 is displayed.

Linking between the intermediate Control Symbol and its Request or Response Packet. At every Acknowledge Control Symbol, the disassembly scans a fixed number of samples (defined by the Linking Range option) backwards and tries to match the ackID fields in the Control Symbol and the Request or Response Packets. If a match is found, the sample number of the responding Request or Response Packet is placed at the Control Symbol.

Linking between the Response Packet and the Request Packet. At every Response Packet, the disassembly scans a fixed number of samples (defined by the Linking Range option) backwards and tries to match the targetTID field in the Response Packet and the srcTID field in the Request Packets. If a match is found, the sample number of the corresponding Request Packet is placed at the Response Packet.

Linking Cycle Type Labels

Table 2–8 shows the linking labels and their descriptions when the Linking Function is turned on.

Table 2-8: Linking cycle type labels and their descriptions

Cycle type labels	Description
RESPONSE NOT FOUND	This message is displayed when any of the following conditions occur during forward linking: A Gap was encountered when looking for a response or symbol. The end of the acquisition was reached before finding a corresponding response or symbol. Both packet and symbol responses were not found. The Linking Range was entered as zero.
PACKET RESPONSE NOT FOUND	This message is displayed when the corresponding response packet is not found in the acquisition during forward linking.
CONTROL RESPONSE NOT FOUND	This message is displayed when the corresponding control symbol is not found in the acquisition during forward linking.
CORRESPONDING PACKET NOT FOUND	This message is displayed when backward linking for control symbols not successful.
REQUEST NOT FOUND	This message is displayed when backward linking for response packets is not successful.

Limitations

The Linking Function has the following limitations:

- If the transaction field of any Request Packet, Write Packet or Maintenance Packet is “reserved” then the corresponding Response Packet is not forward linked.
- If both the Request and the Response Packets do not lie within the linking range entered in the disassembly properties window, linking is not done.

Figure 2-6 shows a display of the RIO8 reference memory when the Linking Function is switched on.

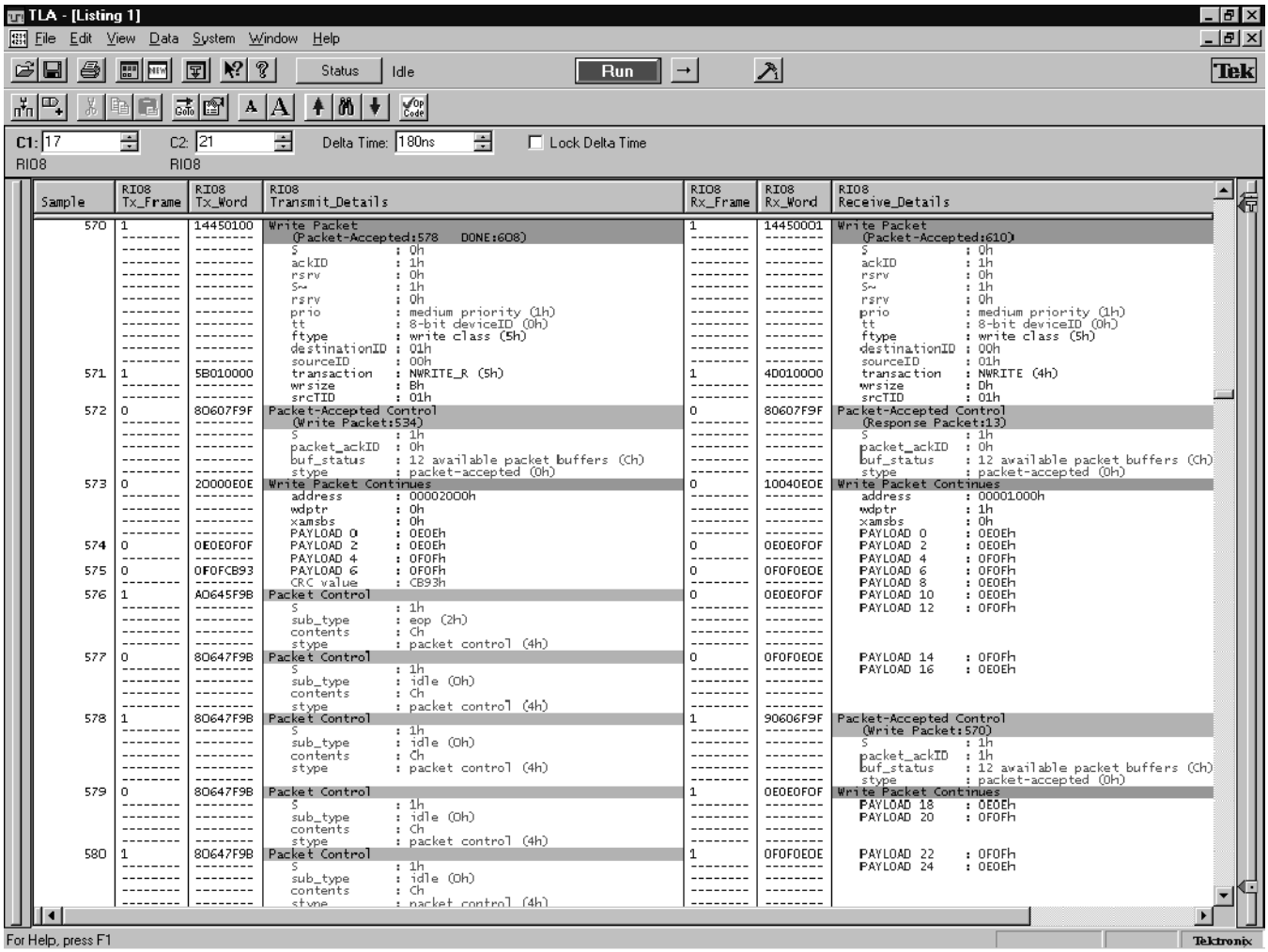


Figure 2-6: Example of the Linking Function

Setup/Hold Time Adjustments

Most devices you test require an adjustment of the Setup/Hold values in the TLA700 Application. The logic analyzer application provides AutoDeskew to automatically deskew and verify the logic analyzer Setup/Hold window. AutoDeskew can also be used to test Setup/Hold violations of the current setting. For more information on AutoDeskew, refer to the logic analyzer online help.

The Setup/Hold adjustments can be made for each channel. You can use custom clock setups and different Setup/Hold settings for each type of clocking. The AutoDeskew capability to analyze the Setup/Hold violations allows you to test for violations that occur with current Setup/Hold settings. You can automatically convert a test setup to a trigger setup for use with the logic analyzer trigger system. This allows you to determine exactly which channels may be failing the Setup/Hold requirements.

AutoDeskew is preconfigured for the support packages RIO8, RIO16, RIO8_34, and RIO16_34. Follow the steps to use AutoDeskew:

1. Load the support package and click the AutoDeskew button on the tool bar to open the AutoDeskew window.
2. Click the Define Setup button to display the AutoDeskew Setup dialog.
3. Select Custom under AutoDeskew mode. Based on the loaded support package, the AutoDeskew configurations and settings show different options.
4. Choose the appropriate options for the AutoDeskew configuration and settings.
5. Click the Analyze button to start analysis.
6. After the analysis is complete, the results are displayed.
7. Click the Apply button to apply the analyzed results. You can manually examine the window choices and move the sample point if needed before clicking the Apply button.

Each support has several AutoDeskew configurations based on the clock signal that is used as a source clock for acquisition. Each Configuration has several settings corresponding to the channels to be analyzed.

RIO8 Configurations and Settings

You can select the following configurations and settings for the RIO8 support package.

RIO8 RCLK0 AutoDeskew Configuration

The following settings are available for RIO8 RCLK0 AutoDeskew:

- Analyze RIO Receive channels
- Analyze RIO channels

RIO8 TCLK0 AutoDeskew Configuration

The following settings are available for RIO8 TCLK0 AutoDeskew:

- Analyze RIO Transmit channels
- Analyze RIO channels

RIO16 Configurations and Settings

You can select the following configurations and settings for the RIO16 support package.

RIO16 RCLK1 AutoDeskew Configuration

The following settings are available for RIO16 RCLK1 AutoDeskew:

- Analyze RIO Receive channels
- Analyze RIO channels

RIO16 RCLK0 AutoDeskew Configuration

The following settings are available for RIO16 RCLK0 AutoDeskew:

- Analyze RIO Receive channels
- Analyze RIO channels

RIO16 TCLK1 AutoDeskew Configuration

The following settings are available for RIO16 TCLK1 AutoDeskew:

- Analyze RIO Transmit channels
- Analyze RIO channels

RIO16 TCLK0 AutoDeskew Configuration

The following settings are available for RIO16 TCLK0 AutoDeskew:

- Analyze RIO Transmit channels
- Analyze RIO channels

RIO8_34 Configurations and Settings

You can select the following configurations and settings for the RIO8_34 support package.

RIO8_34 AutoDeskew Configuration

The following settings are available for RIO8_34 AutoDeskew:

- Analyze RIO channels

RIO16_34 Configurations and Settings

You can select the following configurations and settings for the RIO16_34 support package.

RIO16_34 AutoDeskew Configuration

The following settings are available for RIO16_34 AutoDeskew:

- Analyze RIO channels

Reference

Channel Group Definitions

This section lists the channel group definitions for the RapidIO product required for disassembly.

Channel Groups

Channel groups required for clocking and disassembly for TMS805 RapidIO bus support are as follows:

RIO8: The following groups are required for disassembly. Only these groups are displayed in the listing window.

Tx_Frame
Tx_Word
Transmit_Details
Rx_Frame
Rx_Word
Receive_Details
Timestamp

The following trigger groups are used for triggering and are not displayed in the listing window.

Tx_Symbol	Rx_Symbol
Tx_Packet	Rx_Packet
Tx_Sbit	Rx_Sbit
Tx_AckID	Rx_AckID
Tx_Priority	Rx_Priority
Tx_Tt	Rx_Tt
Tx_Ftype	Rx_Ftype
Tx_DestID	Rx_DestID
Tx_SrcID	Rx_SrcID
Tx_Ttype	Rx_Ttype
Tx_Msglen	Rx_Msglen
Tx_Size	Rx_Size
Tx_Status	Rx_Status
Tx_TID	Rx_TID
Tx_Letter	Rx_Letter
Tx_Mbox	Rx_Mbox
Tx_MsgSeg	Rx_MsgSeg
Tx_HopCount	Rx_HopCount
Tx_DrBellInfo	Rx_DrBellInfo

Tx_SecDomain	Rx_SecDomain
Tx_SecID	Rx_SecID
Tx_SecTID	Rx_SecTID
Tx_Config[0:7]	Rx_Config[0:7]
Tx_Config[8:20]	Rx_Config[8:20]
Tx_A[0:15]	Rx_A[0:15]
Tx_A[16:31]	Rx_A[16:31]
Tx_A[0:31]	Rx_A[0:31]
Tx_A1[0:15]	Rx_A1[0:15]
Tx_A1[16:31]	Rx_A1[16:31]
Tx_Data[0:15]	Rx_Data[0:15]
Tx_Data[16:31]	Rx_Data[16:31]
Tx_Data[0:31]	Rx_Data[0:31]
Tx_Data[0]	Rx_Data[0]
Tx_Data[8]	Rx_Data[8]
Tx_Data[16]	Rx_Data[16]
Tx_Data[24]	Rx_Data[24]
	zIdle

RIO16: The following groups are required for disassembly. Only these groups are displayed in the listing window.

Tx_Frame
Tx_Word
Transmit_Details
Rx_Frame
Rx_Word
Receive_Details
Timestamp

The following trigger groups are used for triggering and are not displayed in the listing window.

Tx_Symbol	Rx_Symbol
Tx_Packet	Rx_Packet
Tx_Sbit	Rx_Sbit
Tx_AckID	Rx_AckID
Tx_Priority	Rx_Priority
Tx_Tt	Rx_Tt
Tx_Ftype	Rx_Ftype
Tx_DestID	Rx_DestID
Tx_SrcID	Rx_SrcID
Tx_Ttype	Rx_Ttype
Tx_Msglen	Rx_Msglen
Tx_Size	Rx_Size
Tx_Status	Rx_Status

Tx_TID	Rx_TID
Tx_Letter	Rx_Letter
Tx_Mbox	Rx_Mbox
Tx_MsgSeg	Rx_MsgSeg
Tx_HopCount	Rx_HopCount
Tx_DrBellInfo	Rx_DrBellInfo
Tx_SecDomain	Rx_SecDomain
Tx_SecID	Rx_SecID
Tx_SecTID	Rx_SecTID
Tx_Config[0:7]	Rx_Config[0:7]
Tx_Config[8:20]	Rx_Config[8:20]
Tx_A[0:15]	Rx_A[0:15]
Tx_A[16:31]	Rx_A[16:31]
Tx_A[0:31]	Rx_A[0:31]
Tx_A1[0:15]	Rx_A1[0:15]
Tx_A1[16:31]	Rx_A1[16:31]
Tx_Data[0:15]	Rx_Data[0:15]
Tx_Data[16:31]	Rx_Data[16:31]
Tx_Data[0:31]	Rx_Data[0:31]
Tx_Data[0]	Rx_Data[0]
Tx_Data[16]	Rx_Data[16]
	zIdle

RIO8_T: Table 3–1 shows the RIO8_T groups listed in the same order on the screen.

Table 3-1: RIO8_T channel groups

Group name	Display radix
Tx_Data	HEX
Rx_Data	HEX

RIO16_T: Table 3–2 shows the RIO16_T groups listed in the same order on the screen.

Table 3-2: RIO16_T channel groups

Group name	Display radix
Tx_Data	HEX
Rx_Data	HEX

RIO8_34: The following groups are required for disassembly. Only these groups are displayed in the listing window.

Frame
Word
Timestamp

The following trigger groups are used for triggering and are not displayed in the listing window.

T_Symbol
T_Packet
T_Sbit
T_AckID
T_Priority
T_Tt
T_Ftype
T_DestID
T_SrcID
T_Ttype
T_Msglen
T_Size
T_Status
T_TID
T_Letter
T_Mbox
T_MsgSeg
T_HopCount
T_DrBellInfo
T_SecDomain
T_SecID
T_SecTID
T_Config[0:7]
T_Config[8:20]
T_A[0:15]
T_A[16:31
T_A[16:31]
T_A[0:31]
T_A1[0:15]
T_A1[16:31
T_Data[0:15]
T_Data[16:31]
T_Data[0:31]
T_Data[0]
T_Data[8]
T_Data[16]
T_Data[24]

RIO16_34: The following groups are required for disassembly. Only these groups are displayed in the listing window.

Frame
Word
Timestamp

The following trigger groups are used for triggering and are not displayed in the listing window.

T_Symbol
T_Packet
T_Sbit
T_AckID
T_Priority
T_Tt
T_Ftype
T_DestID
T_SrcID
T_SecDomain
T_SecID
T_SecTID
T_Config[0:7]
T_Config[8:20]
T_A[0:15]
T_A[16:31
T_A[16:31]
T_A[0:31]

T_Ttype	T_A1[0:15]
T_Msglen	T_A1[16:31
T_Size	T_Data[0:15]
T_Status	T_Data[16:31]
T_TID	T_Data[0:31]
T_Letter	T_Data[0]
T_Mbox	T_Data[8]
T_MsgSeg	T_Data[16]
T_HopCount	T_Data[24]
T_DrBellInfo	

If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–8.

Symbol and Channel Assignment Tables

This section lists the symbol tables and channel assignment tables for disassembly and timing.

Symbol Tables

The TMS805 support package supplies color symbol table files for the RIO8, RIO16, RIO8_34, and RIO16_34 supports.

Tables 3–3 through 3–4 show the definitions for color, bit pattern, and meaning of the group symbols in color symbol tables.

Table 3-3: Color symbol table definitions for transmit interface

Symbol	Binary Pattern	Description
GREEN_W	0 0 0 0 0 0	Green text with white background
RED_W	0 0 0 0 0 1	Red text with white background
BLUE_W	0 0 0 0 1 0	Blue text with white background
BLACK_L	0 0 0 0 1 1	Black text with lime background
BLACK_C	0 0 0 1 0 0	Black text with cyan background
BLACK_S	0 0 0 1 0 1	Black text with silver background
BLACK_Y	0 0 0 1 1 0	Black text with yellow background
WHITE_W	0 0 0 1 1 1	White text with white background

Table 3-4: Color1 symbol table definitions for receive interface

Symbol	Binary Pattern	Description
GREEN_W	0 0 0 0 0 0	Green text with white background
RED_W	0 0 0 0 0 1	Red text with white background
BLUE_W	0 0 0 0 1 0	Blue text with white background
BLACK_L	0 0 0 0 1 1	Black text with lime background
BLACK_C	0 0 0 1 0 0	Black text with cyan background
BLACK_S	0 0 0 1 0 1	Black text with silver background
BLACK_Y	0 0 0 1 1 0	Black text with yellow background
WHITE_W	0 0 0 1 1 1	White text with white background

Information on basic operations describes how to use symbolic values for triggering.

Channel Assignment Tables

Channel assignments shown in Table 3-5 through Table 3-16 use the following conventions:

- All signals are required by the support package, unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules, unless otherwise noted.

RIO8 and RIO16 Channel Group Assignments

Tables 3-5 through 3-8 show the channel assignments for the logic analyzer groups for the RIO8 and RIO16 support packages and the signal to which each channel connects.

Table 3-5 shows the channel assignments for the Tx_Frame group and the signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-5: Tx_Frame group assignments

Bit order	RapidIO support package channel name
0	TFRAME

Table 3-6 shows the channel assignments for the Tx_Word group and the signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-6: Tx_Word group assignments

Bit order	RapidIO support pacakge channel name
31 (MSB)	TD0
30	TD1
29	TD2
28	TD3
27	TD4
26	TD5

Table 3-6: Tx_Word group assignments (Cont.)

Bit order	RapidIO support pacakge channel name
25	TD6
24	TD7
23	TD8
22	TD9
21	TD10
20	TD11
19	TD12
18	TD13
17	TD14
16	TD15
15	TD16
14	TD17
13	TD18
12	TD19
11	TD20
10	TD21
9	TD22
8	TD23
7	TD24
6	TD25
5	TD26
4	TD27
3	TD28
2	TD29
1	TD30
0 (LSB)	TD31

Table 3–7 shows the channel assignments for the Rx_Frame group and the signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3-7: Rx_Frame group assignments

Bit order	RapidIO support package channel name
0	RFRAME

Table 3–8 shows the channel assignments for the Rx_Word group and the signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3-8: Rx_Word group assignments

Bit order	RapidIO support package channel name
31 (MSB)	RD0
30	RD1
29	RD2
28	RD3
27	RD4
26	RD5
25	RD6
24	RD7
23	RD8
22	RD9
21	RD10
20	RD11
19	RD12
18	RD13
17	RD14
16	RD15
15	RD16
14	RD17
13	RD18
12	RD19
11	RD20

Table 3-8: Rx_Word group assignments (Cont.)

Bit order	RapidIO support package channel name
10	RD21
9	RD22
8	RD23
7	RD24
6	RD25
5	RD26
4	RD27
3	RD28
2	RD29
1	RD30
0 (LSB)	RD31

RIO8_T and RIO16_T Channel Group Assignments

Tables 3-9 through 3-12 show the channel assignments for the groups of the RIO8_T and RIO16_T support packages and the signal to which each channel connects.

Table 3-9: RIO8 _T Tx_Data group assignments

Bit order	RIO8_T support package channel name
7 (MSB)	TD0
6	TD1
5	TD2
4	TD3
3	TD4
2	TD5
1	TD6
0 (LSB)	TD7

Table 3-10: RIO8_T Rx_Data group assignments

Bit order	RIO8_T support package channel name
7 (MSB)	RD0
6	RD1
5	RD2
4	RD3
3	RD4
2	RD5
1	RD6
0 (LSB)	RD7

Tables 3–11 through 3–12 show the channel assignments for the groups of the RIO16_T support package and the signal to which each channel connects.

Table 3-11: RIO16_T Tx_Data group assignments

Bit order	RIO16_T support package channel name
15 (MSB)	TD0
14	TD1
13	TD2
12	TD3
11	TD4
10	TD5
9	TD6
8	TD7
7	TD8
6	TD9
5	TD10
4	TD11
3	TD12
2	TD13
1	TD14
0 (LSB)	TD15

Table 3-12: RIO16_T Rx_Data group assignments

Bit order	RIO16_T support package channel name
15 (MSB)	RD0
14	RD1
13	RD2
12	RD3
11	RD4
10	RD5
9	RD6
8	RD7
7	RD8
6	RD9
5	RD10
4	RD11
3	RD12
2	RD13
1	RD14
0 (LSB)	RD15

Clock and Control Signal Channel Assignments

Tables 3-13 through 3-16 show the channel assignments for the clock and qualifier probes, and the signal to which each channel connects.

Table 3-13: RIO8 clock and control signal channel assignments

Logic analyzer clock/qualifer channel	RapidIO support package channel name
CK0	TFRAME
CK1	TCLK0_D
CK2	RFRAME_D
CK3	RCLK0_D
Q0	TCLK0
Q1	TFRAME_D
Q2	RCLK0
Q3	RFRAME

Table 3-14: RIO16 clock and control signal channel assignments

Logic analyzer clock/qualifier channel	RapidIO support package channel name
CK0	TFRAME
CK1	RCLK1
CK2	NOT CONNECTED
CK3	TCLK1
Q0	TCLK0
Q1	NOT CONNECTED
Q2	RCLK0
Q3	RFRAME

Table 3-15: RIO8_T clock and control signal channel assignments

Logic analyzer clock/qualifier channel	RapidIO support package channel name
CK0	TFRAME
CK1	NOT CONNECTED
CK2	NOT CONNECTED
CK3	NOT CONNECTED
Q0	TCLK0
Q1	NOT CONNECTED
Q2	RCLK0
Q3	RFRAME

Table 3-16: RIO16_T clock and control signal channel assignments

Logic analyzer clock/qualifier channel	RapidIO support package channel name
CK0	TFRAME
CK1	RCLK1
CK2	NOT CONNECTED
CK3	TCLK1
Q0	TCLK0

Table 3-16: RIO16_T clock and control signal channel assignments (Cont.)

Logic analyzer clock/qualifier channel	RapidIO support package channel name
Q1	NOT CONNECTED
Q2	RCLK0
Q3	RFRAME

Signals not Required for Clocking and Disassembly for RIO8 and RIO16 Support

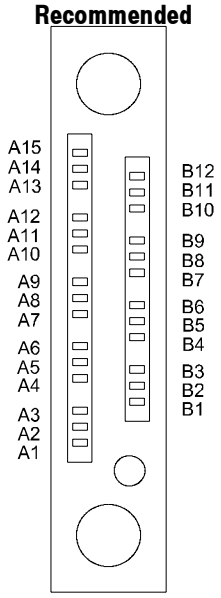
At least one among TCLK0, TCLK1, RCLK0, or RCLK1 clock signals must be acquired. The remaining one or three clocks (depending on the RIO8 or RIO16 support packages) are optional. When only a transmit or receive bus is acquired, all frame and data channels on the other bus are also optional.

Signal Source To Probe Connections

For design purposes, you may need to make connections between the Signal Source and the P6880 Logic Analyzer Probe. Refer to the *P6810, P6860, and P6880 Logic Analyzer Probes Instruction* manual, Tektronix part number 071-1059-XX, for more information on mechanical specifications. Tables 3–18 through 3–44 show the Signal Source to P6880 pin connections.

The recommended pin assignment is the P6880 pin assignment. See Table 3–17.

Table 3-17: Recommended pin assignments (component side)

Type of pin assignment	Comments
Recommended  **P6880 Pin Assignment**	Recommended. This pin assignment is what we recommend that you use.

Connections for RIO8 Support

Tables 3–18 through 3–27 show the pin connections for the RIO8 support.

Table 3-18: Clock and control signals channel assignments for transmit and receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
CK0	TFRAME	A13	CK0+	TFRAME+
		A15	CK0-	TFRAME-
Q0	TCLK0	A13	Q0+	TCLK0+
		A15	Q0-	TCLK0-
Q2	RCLK0	A13	Q2+	RCLK0+
		A15	Q2-	RCLK0-
Q3	RFRAME	A13	Q3+	RFRAME+
		A15	Q3-	RFRAME-

Table 3-19: Demuxed clock and control signal channel assignments for transmit and receive bus

Logic analyzer clock signal	RapidIO support package channel name
CK1	TCLK0_D
CK2	RFRAME_D
CK3	RCLK0_D
Q1	TFRAME_D

Table 3-20: A3 probe channel assignments for transmit bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
A3(7)	TD7	B12	A3:7+	TD7-
		B10	A3:7-	TD7+
A3(6)	TD6	A10	A3:6+	TD6+
		A12	A3:6-	TD6-
A3(5)	TD5	B9	A3:5+	TD5-
		B7	A3:5-	TD5+
A3(4)	TD4	A7	A3:4+	TD4+

Table 3-20: A3 probe channel assignments for transmit bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
		A9	A3:4-	TD4-
A3(3)	TD3	B6	A3:3+	TD3-
		B4	A3:3-	TD3+
A3(2)	TD2	A4	A3:2+	TD2+
		A6	A3:2-	TD2-
A3(1)	TD1	B3	A3:1+	TD1-
		B1	A3:1-	TD1+
A3(0)	TD0	A1	A3:0+	TD0+
		A3	A3:0-	TD0-

Table 3-21: A2 probe channel assignments for transmit bus demuxed from A3

Logic analyzer clock signal	RapidIO support package channel name
A2(7)	TD23
A2(6)	TD22
A2(5)	TD21
A2(4)	TD20
A2(3)	TD19
A2(2)	TD18
A2(1)	TD17
A2(0)	TD16

Table 3-22: D3 probe channel assignments for transmit bus demuxed from A3

Logic analyzer clock signal	RapidIO support package channel name
D3(7)	TD15
D3(6)	TD14
D3(5)	TD13
D3(4)	TD12
D3(3)	TD11

Table 3-22: D3 probe channel assignments for transmit bus demuxed from A3 (Cont.)

Logic analyzer clock signal	RapidIO support package channel name
D3(2)	TD10
D3(1)	TD9
D3(0)	TD8

Table 3-23: D2 probe channel assignments for transmit bus demuxed from A3

Logic analyzer clock signal	RapidIO support package channel name
D2(7)	TD31
D2(6)	TD30
D2(5)	TD29
D2(4)	TD28
D2(3)	TD27
D2(2)	TD26
D2(1)	TD25
D2(0)	TD24

Table 3-24: E3 probe channel assignments for receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
E3(7)	RD7	B12	E3:7+	RD7-
		B10	E3:7-	RD7+
E3(6)	RD6	A10	E3:6+	RD6+
		A12	E3:6-	RD6-
E3(5)	RD5	B9	E3:5+	RD5-
		B7	E3:5-	RD5+
E3(4)	RD4	A7	E3:4+	RD4+
		A9	E3:4-	RD4-
E3(3)	RD3	B6	E3:3+	RD3-
		B4	E3:3-	RD3+
E3(2)	RD2	A4	E3:2+	RD2+

Table 3-24: E3 probe channel assignments for receive bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
		A6	E3:2-	RD2-
E3(1)	RD1	B3	E3:1+	RD1-
		B1	E3:1-	RD1+
E3(0)	RD0	A1	E3:0+	RD0+
		A3	E3:0-	RD0-

Table 3-25: E2 probe channel assignments for receive bus demuxed from E3

Logic analyzer clock signal	RapidIO support package channel name
E2(7)	RD23
E2(6)	RD22
E2(5)	RD21
E2(4)	RD20
E2(3)	RD19
E2(2)	RD18
E2(1)	RD17
E2(0)	RD16

Table 3-26: E1 probe channel assignments for receive bus demuxed from E3

Logic analyzer clock signal	RapidIO support package channel name
E1(7)	RD15
E1(6)	RD14
E1(5)	RD13
E1(4)	RD12
E1(3)	RD11
E1(2)	RD10
E1(1)	RD9
E1(0)	RD8

Table 3-27: E0 probe channel assignments for receive bus demuxed from E3

Logic analyzer clock signal	RapidIO support package channel name
E0(7)	RD31
E0(6)	RD30
E0(5)	RD29
E0(4)	RD28
E0(3)	RD27
E0(2)	RD26
E0(1)	RD25
E0(0)	RD24

P6880 probe channels not connected. A0, A1, C0, C1, C2, C3, D0, and D1 probe channels are not connected and not used.

Connections for RIO16 Support

Tables 3–28 through 3–36 show the pin connections for the RIO16 support.

Table 3-28: Clock and control signals channel assignments for transmit and receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
CK0	TFRAME	A13	CK0+	TFRAME+
		A15	CK0-	TFRAME-
CK1	RCLK1	A13	CK1+	RCLK1+
		A15	CK1-	RCLK1-
CK2	NOT CONNECTED	A13	CK2+	NOT CONNECTED
		A15	CK2-	NOT CONNECTED
CK3	TCLK1	A13	CK3+	TCLK1+
		A15	CK3-	TCLK1-
Q0	TCLK0	A13	Q0+	TCLK0+
		A15	Q0-	TCLK0-
Q1	NOT CONNECTED	A13	Q1+	NOT CONNECTED
		A15	Q1-	NOT CONNECTED
Q2	RCLK0	A13	Q2+	RCLK0+
		A15	Q2-	RCLK0-

Table 3-28: Clock and control signals channel assignments for transmit and receive bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
Q3	RFRAME	A13	Q3+	RFRAME+
		A15	Q3-	RFRAME-

Table 3-29: A3 probe channel assignments for transmit bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
A3(7)	TD7	B12	A3:7+	TD7-
		B10	A3:7-	TD7+
A3(6)	TD6	A10	A3:6+	TD6+
		A12	A3:6-	TD6-
A3(5)	TD5	B9	A3:5+	TD5-
		B7	A3:5-	TD5+
A3(4)	TD4	A7	A3:4+	TD4+
		A9	A3:4-	TD4-
A3(3)	TD3	B6	A3:3+	TD3-
		B4	A3:3-	TD3+
A3(2)	TD2	A4	A3:2+	TD2+
		A6	A3:2-	TD2-
A3(1)	TD1	B3	A3:1+	TD1-
		B1	A3:1-	TD1+
A3(0)	TD0	A1	A3:0+	TD0+
		A3	A3:0-	TD0-

Table 3-30: A1 probe channel assignments for receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
A1(7)	RD15	B12	A1:7+	RD15-
		B10	A1:7-	RD15+
A1(6)	RD14	A10	A1:6+	RD14+
		A12	A1:6-	RD14-
A1(5)	RD13	B9	A1:5+	RD13-

Table 3-30: A1 probe channel assignments for receive bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
		B7	A1:5-	RD13+
A1(4)	RD12	A7	A1:4+	RD12+
		A9	A1:4-	RD12-
A1(3)	RD11	B6	A1:3+	RD11-
		B4	A1:3-	RD11+
A1(2)	RD10	A4	A1:2+	RD10+
		A6	A1:2-	RD10-
A1(1)	RD9	B3	A1:1+	RD9-
		B1	A1:1-	RD9+
A1(0)	RD8	A1	A1:0+	RD8+
		A3	A1:0-	RD8-

Table 3-31: D3 probe channel assignments for transmit bus demuxed from A3

Logic analyzer clock signal	RapidIO support package channel name
D3(7)	TD23
D3(6)	TD22
D3(5)	TD21
D3(4)	TD20
D3(3)	TD19
D3(2)	TD18
D3(1)	TD17
D3(0)	TD16

Table 3-32: D1 probe channel assignments for receive bus demuxed from A1

Logic analyzer clock signal	RapidIO support package channel name
D1(7)	RD31
D1(6)	RD30
D1(5)	RD29

Table 3-32: D1 probe channel assignments for receive bus demuxed from A1 (Cont.)

Logic analyzer clock signal	RapidIO support package channel name
D1(4)	RD28
D1(3)	RD27
D1(2)	RD26
D1(1)	RD25
D1(0)	RD24

Table 3-33: C3 probe channel assignments for transmit bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
C3(7)	TD15	B12	C3:7+	TD15-
		B10	C3:7-	TD15+
C3(6)	TD14	A10	C3:6+	TD14+
		A12	C3:6-	TD14-
C3(5)	TD13	B9	C3:5+	TD13-
		B7	C3:5-	TD13+
C3(4)	TD12	A7	C3:4+	TD12+
		A9	C3:4-	TD12-
C3(3)	TD11	B6	C3:3+	TD11-
		B4	C3:3-	TD11+
C3(2)	TD10	A4	C3:2+	TD10+
		A6	C3:2-	TD10-
C3(1)	TD9	B3	C3:1+	TD9-
		B1	C3:1-	TD9+

Table 3-33: C3 probe channel assignments for transmit bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
C3(0)	TD8	A1	C3:0+	TD8+
		A3	C3:0-	TD8-

Table 3-34: C1 probe channel assignments for transmit bus demuxed from C3

Logic analyzer clock signal	RapidIO support package channel name
C1(7)	TD31
C1(6)	TD30
C1(5)	TD29
C1(4)	TD28
C1(3)	TD27
C1(2)	TD26
C1(1)	TD25
C1(0)	TD24

Table 3-35: E3 probe channel assignments for receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
E3(7)	RD7	B12	E3:7+	RD7-
		B10	E3:7-	RD7+
E3(6)	RD6	A10	E3:6+	RD6+
		A12	E3:6-	RD6-
E3(5)	RD5	B9	E3:5+	RD5-
		B7	E3:5–	RD5+
E3(4)	RD4	A7	E3:4+	RD4+
		A9	E3:4-	RD4-
E3(3)	RD3	B6	E3:3+	RD3-
		B4	E3:3-	RD3+
E3(2)	RD2	A4	E3:2+	RD2+
		A6	E3:2-	RD2-
E3(1)	RD1	B3	E3:1+	RD1-

Table 3-35: E3 probe channel assignments for receive bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
		B1	E3:1-	RD1+
E3(0)	RD0	A1	E3:0+	RD0+
		A3	E3:0-	RD0-

Table 3-36: E1 probe channel assignments for receive bus demuxed from E3

Logic analyzer clock signal	RapidIO support package channel name
E1(7)	RD23
E1(6)	RD22
E1(5)	RD21
E1(4)	RD20
E1(3)	RD19
E1(2)	RD18
E1(1)	RD17
E1(0)	RD16

P6880 probe channels not connected. A0, A2, C0, C2, D0, D2, E0, and E2 probe channels are not connected and not used.

Connections for RIO8_T Support

Tables 3-37 through 3-39 show the pin connections for the RIO8_T support.

Table 3-37: Clock and control signals channel assignments for transmit and receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
CK0	TFRAME	A13	CK0+	TFRAME+
		A15	CK0-	TFRAME-
CK1	NOT CONNECTED	A13	CK1+	NOT CONNECTED
		A15	CK1-	NOT CONNECTED
CK2	NOT CONNECTED	A13	CK2+	NOT CONNECTED
		A15	CK2-	NOT CONNECTED

Table 3-37: Clock and control signals channel assignments for transmit and receive bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
CK3	NOT CONNECTED	A13	CK3+	NOT CONNECTED
		A15	CK3-	NOT CONNECTED
Q0	TCLK0	A13	Q0+	TCLK0+
		A15	Q0-	TCLK0-
Q1	NOT CONNECTED	A13	Q1+	NOT CONNECTED
		A15	Q1-	NOT CONNECTED
Q2	RCLK0	A13	Q2+	RCLK0+
		A15	Q2-	RCLK0-
Q3	RFRAME	A13	Q3+	RFRAME+
		A15	Q3-	RFRAME-

Table 3-38: A3 probe channel assignments for transmit bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
A3(7)	TD7	B12	A3:7+	TD7-
		B10	A3:7-	TD7+
A3(6)	TD6	A10	A3:6+	TD6+
		A12	A3:6-	TD6-
A3(5)	TD5	B9	A3:5+	TD5-
		B7	A3:5-	TD5+
A3(4)	TD4	A7	A3:4+	TD4+
		A9	A3:4-	TD4-
A3(3)	TD3	B6	A3:3+	TD3-
		B4	A3:3-	TD3+
A3(2)	TD2	A4	A3:2+	TD2+
		A6	A3:2-	TD2-
A3(1)	TD1	B3	A3:1+	TD1-
		B1	A3:1-	TD1+
A3(0)	TD0	A1	A3:0+	TD0+
		A3	A3:0-	TD0-

Table 3-39: E3 probe channel assignments for receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
E3(7)	RD7	B12	E3:7+	RD7-
		B10	E3:7-	RD7+
E3(6)	RD6	A10	E3:6+	RD6+
		A12	E3:6-	RD6-
E3(5)	RD5	B9	E3:5+	RD5-
		B7	E3:5-	RD5+
E3(4)	RD4	A7	E3:4+	RD4+
		A9	E3:4-	RD4-
E3(3)	RD3	B6	E3:3+	RD3-
		B4	E3:3-	RD3+
E3(2)	RD2	A4	E3:2+	RD2+
		A6	E3:2-	RD2-
E3(1)	RD1	B3	E3:1+	RD1-
		B1	E3:1-	RD1+
E3(0)	RD0	A1	E3:0+	RD0+
		A3	E3:0-	RD0-

P6880 probe channels not connected. A0, A1, A2, C0, C1, C2, C3, D0, D1, D2, D3, E0, E1, and E2 probe channels are not connected and not used.

Connections for RIO16_T Support

Tables 3-40 through 3-44 show the pin connections for the RIO16_T support.

Table 3-40: Clock and control signals channel assignments for transmit and receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
CK0	TFRAME	A13	CK0+	TFRAME+
		A15	CK0-	TFRAME-
CK1	RCLK1	A13	CK1+	RCLK1+
		A15	CK1-	RCLK1-
CK2	NOT CONNECTED	A13	CK2+	NOT CONNECTED
		A15	CK2-	NOT CONNECTED
CK3	TCLK1	A13	CK3+	TCLK1+

Table 3-40: Clock and control signals channel assignments for transmit and receive bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
		A15	CK3-	TCLK1-
Q0	TCLK0	A13	Q0+	TCLK0+
		A15	Q0-	TCLK0-
Q1	NOT CONNECTED	A13	Q1+	NOT CONNECTED
		A15	Q1-	NOT CONNECTED
Q2	RCLK0	A13	Q2+	RCLK0+
		A15	Q2-	RCLK0-
Q3	RFRAME	A13	Q3+	RFRAME+
		A15	Q3-	RFRAME-

Table 3-41: A3 probe channel assignments for transmit bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
A3(7)	TD7	B12	A3:7+	TD7-
		B10	A3:7-	TD7+
A3(6)	TD6	A10	A3:6+	TD6+
		A12	A3:6-	TD6-
A3(5)	TD5	B9	A3:5+	TD5-
		B7	A3:5-	TD5+
A3(4)	TD4	A7	A3:4+	TD4+
		A9	A3:4-	TD4-
A3(3)	TD3	B6	A3:3+	TD3-
		B4	A3:3-	TD3+
A3(2)	TD2	A4	A3:2+	TD2+
		A6	A3:2-	TD2-
A3(1)	TD1	B3	A3:1+	TD1-
		B1	A3:1-	TD1+
A3(0)	TD0	A1	A3:0+	TD0+
		A3	A3:0-	TD0-

Table 3-42: A1 probe channel assignments for receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
A1(7)	RD15	B12	A1:7+	RD15-
		B10	A1:7-	RD15+
A1(6)	RD14	A10	A1:6+	RD14+
		A12	A1:6-	RD14-
A1(5)	RD13	B9	A1:5+	RD13-
		B7	A1:5-	RD13+
A1(4)	RD12	A7	A1:4+	RD12+
		A9	A1:4-	RD12-
A1(3)	RD11	B6	A1:3+	RD11-
		B4	A1:3-	RD11+
A1(2)	RD10	A4	A1:2+	RD10+
		A6	A1:2-	RD10-
A1(1)	RD9	B3	A1:1+	RD9-
		B1	A1:1-	RD9+
A1(0)	RD8	A1	A1:0+	RD8+
		A3	A1:0-	RD8-

Table 3-43: C3 probe channel assignments for transmit bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
C3(7)	TD15	B12	C3:7+	TD15-
		B10	C3:7-	TD15+
C3(6)	TD14	A10	C3:6+	TD14+
		A12	C3:6-	TD14-
C3(5)	TD13	B9	C3:5+	TD13-
		B7	C3:5-	TD13+
C3(4)	TD12	A7	C3:4+	TD12+
		A9	C3:4-	TD12-
C3(3)	TD11	B6	C3:3+	TD11-
		B4	C3:3-	TD11+
C3(2)	TD10	A4	C3:2+	TD10+
		A6	C3:2-	TD10-
C3(1)	TD9	B3	C3:1+	TD9-

Table 3-43: C3 probe channel assignments for transmit bus (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
		B1	C3:1-	TD9+
C3(0)	TD8	A1	C3:0+	TD8+
		A3	C3:0-	TD8-

Table 3-44: E3 probe channel assignments for receive bus

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe channel name	RapidIO bus signal name
E3(7)	RD7	B12	E3:7+	RD7-
		B10	E3:7-	RD7+
E3(6)	RD6	A10	E3:6+	RD6+
		A12	E3:6-	RD6-
E3(5)	RD5	B9	E3:5+	RD5-
		B7	E3:5-	RD5+
E3(4)	RD4	A7	E3:4+	RD4+
		A9	E3:4-	RD4-
E3(3)	RD3	B6	E3:3+	RD3-
		B4	E3:3-	RD3+
E3(2)	RD2	A4	E3:2+	RD2+
		A6	E3:2-	RD2-
E3(1)	RD1	B3	E3:1+	RD1-
		B1	E3:1-	RD1+
E3(0)	RD0	A1	E3:0+	RD0+
		A3	E3:0-	RD0-

P6880 probe channels not connected. A0, A2, C0, C1, C2, D0, D1, D2, D3, E0, E1, and E2 probe channels are not connected and not used.

Connections for RIO8_34 Support

Tables 3-45 through 3-49 show the pin connections for the RIO8_34 support.

Table 3-45: Clock and control signals channel assignments

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe #3 probe head 4	RapidIO bus signal name
Clock:0	Clock:0	A15	CK0-	CLK0-
		A13	CK0+	CLK0+
Clock:3	Clock:3	A15	CK3-	FRAME-
		A13	CK3+	FRAME+

Table 3-46: C3 probe channel assignments

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe #1 probe head 4	RapidIO bus signal name
C3:7	Data 7	B12	C3:7+	DATA7+
		B10	C3:7-	DATA7-
C3:6	Data 6	A12	C3:6-	DATA6-
		A10	C3:6+	DATA6+
C3:5	Data 5	B9	C3:5+	DATA5+
		B7	C3:5-	DATA5-
C3:4	Data 4	A9	C3:4-	DATA4-
		A7	C3:4+	DATA4+
C3:3	Data 3	B6	C3:3+	DATA3+
		B4	C3:3-	DATA3-
C3:2	Data 2	A6	C3:2-	DATA2-
		A4	C3:2+	DATA2+
C3:1	Data 1	B3	C3:1+	DATA1+
		B1	C3:1-	DATA1-

Table 3-46: C3 probe channel assignments (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe #1 probe head 4	RapidIO bus signal name
C3:0	Data 0	A3	C3:0-	DATA0-
		A1	C3:0+	DATA0+

Table 3-47: C2 probe channel assignments demuxed from C3

Logic analyzer clock signal	RapidIO support package channel name
C2:7	DATA15
C2:6	DATA14
C2:5	DATA13
C2:4	DATA12
C2:3	DATA11
C2:2	DATA10
C2:1	DATA9
C2:0	DATA8

Table 3-48: A3 probe channel assignments demuxed from C3

Logic analyzer clock signal	RapidIO support package channel name
A3:7	DATA23
A3:6	DATA22
A3:5	DATA21
A3:4	DATA20
A3:3	DATA19
A3:2	DATA18

Table 3-48: A3 probe channel assignments demuxed from C3 (Cont.)

Logic analyzer clock signal	RapidIO support package channel name
A3:1	DATA17
A3:0	DATA16

Table 3-49: A2 probe channel assignments demuxed from C3

Logic analyzer clock signal	RapidIO support package channel name
A2:7	DATA31
A2:6	DATA30
A2:5	DATA29
A2:4	DATA28
A2:3	DATA27
A2:2	DATA26
A2:1	DATA25
A2:0	DATA24

Connections for RIO16_34 Support

Tables 3–50 through 3–54 show the pin connections for the RIO16_34 support.

Table 3-50: Clock and control signals channel assignments

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe #2 probe head 4	RapidIO bus signal name
Clock:0	Clock:1	A15	CK0-	CLK1-
		A13	CK0+	CLK1+
Clock:3	Clock:3	A15	CK3-	FRAME-
		A13	CK3+	FRAME+

Table 3-51: C3 probe channel assignments

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe head 4	RapidIO bus signal name
C3:7	Data 7	B12	C3:7+	DATA7+
		B10	C3:7-	DATA7-
C3:6	Data 6	A12	C3:6-	DATA6-
		A10	C3:6+	DATA6+
C3:5	Data 5	B9	C3:5+	DATA5+
		B7	C3:5-	DATA5-
C3:4	Data 4	A9	C3:4-	DATA4-
		A7	C3:4+	DATA4+
C3:3	Data 3	B6	C3:3+	DATA3+
		B4	C3:3-	DATA3-
C3:2	Data 2	A6	C3:2-	DATA2-
		A4	C3:2+	DATA2+
C3:1	Data 1	B3	C3:1+	DATA1+
		B1	C3:1-	DATA1-
C3:0	Data 0	A3	C3:0-	DATA0-
		A1	C3:0+	DATA0+

Table 3-52: C2 probe channel assignments

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe head 3	RapidIO bus signal name
C2:7	Data 15	B12	C2:7+	DATA15+
		B10	C2:7-	DATA15-
C2:6	Data 14	A12	C2:6-	DATA14-
		A10	C2:6+	DATA14+
C2:5	Data 13	B9	C2:5+	DATA13+
		B7	C2:5-	DATA13-
C2:4	Data 12	A9	C2:4-	DATA12-
		A7	C2:4+	DATA12+
C2:3	Data 11	B6	C2:3+	DATA11+
		B4	C2:3-	DATA11-
C2:2	Data 10	A6	C2:2-	DATA10-
		A4	C2:2+	DATA10+
C2:1	Data 9	B3	C2:1+	DATA9+

Table 3-52: C2 probe channel assignments (Cont.)

Logic analyzer acquisition channel	RapidIO support package channel name	P6880 pad name	P6880 probe head 3	RapidIO bus signal name
		B1	C2:1-	DATA9-
C2:0	Data 8	A3	C2:0-	DATA8-
		A1	C2:0+	DATA8+

Table 3-53: A3 probe channel assignments demuxed from C3

Logic analyzer clock signal	RapidIO support package channel name
A3:7	DATA23
A3:6	DATA22
A3:5	DATA21
A3:4	DATA20
A3:3	DATA19
A3:2	DATA18
A3:1	DATA17
A3:0	DATA16

Table 3-54: A2 probe channel assignments demuxed from C3

Logic analyzer clock signal	RapidIO support package channel name
A2:7	DATA31
A2:6	DATA30
A2:5	DATA29
A2:4	DATA28
A2:3	DATA27
A2:2	DATA26
A2:1	DATA25
A2:0	DATA24

Signal Acquisition

This section contains timing diagrams and tables that list details about how to acquire the relevant address, data, and control signals in TMS805 RapidIO support package.

Signal Acquisition in RIO8

The TMS805 RapidIO support package takes advantage of the four-way demux feature of the logic analyzer hardware to acquire the RapidIO bus signals and create a perfectly aligned 32-bit bus word per logic analyzer sample.

When combined, the 8-bit Tx and Rx RapidIO buses contain four unique pumps of data per transaction. The bus defines a unique clock edge for each pump of data as well (two clocks with two edges each). However, the module hardware can only clock based on one of the two clock domains (the hardware cannot synchronize two different clock domains). This support package uses TCLK0 or RCLK0 as source clock domain depending on the custom clocking options selected during combined clocking. Use RCLK0 for the Rx Only clocking option and TCLK0 for the Tx Only clocking option.

This allows the logic analyzer to detect two out of four clock edges. The other two clock edges are not used.

Since only two clock edges can be used for latching data, you must define phase offsets from TCLK0/RCLK0 to pick up the remaining two data pumps. You can do this through the setup/hold user interface. The support package provides default windows assuming 0 ps skew between the different clocks. Since the logic analyzer can detect both a rising and a falling edge, the clock period is not a variable in the offset equation.

Since the logic analyzer performs a 4x demux on the 8-bit double-pumped bus, each logic analyzer sample contains two bus clock cycles. In this case, it is possible for the bus word to be shifted by 16 bits relative to the logic analyzer sample. The CSM is used to guarantee that this case is corrected before samples are stored in memory.

The FRAME signal must be demuxed by two to maintain alignment with its respective data bus. However, it is really only asserted on 32-bit boundaries. Again, the CSM is used to ensure that the assertion of the FRAME signal always occurs in the first bus cycle in the logic analyzer sample. The extra FRAME signal is named FRAME_D and is meaningless outside of the CSM.

***NOTE**. The support package assumes that the TCLK and RCLK domains are based on the same clock crystal to eliminate clock phase drift between the two clock domains. A static skew between the clock domains is acceptable, since you can calibrate to the skew.*

Figure 3–1 shows a bus timing diagram for the RIO8 support package.

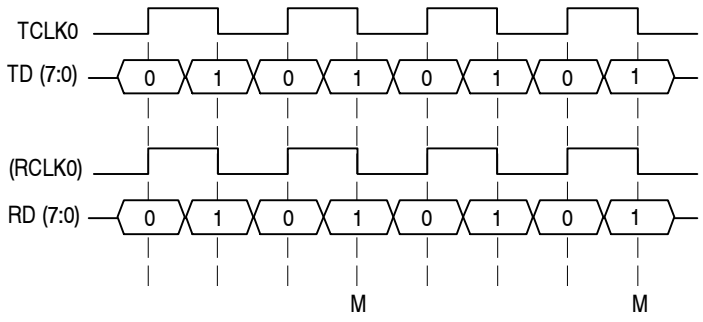


Figure 3-1: Bus timing diagram for the RIO8 support package

Table 3–55 shows the sample points in the RIO8 support package.

Table 3-55: Sample points in the RIO8 support

Master point	Signals
M	TCLK0, TD[7:0], TFRAME, RCLK0, RD[7:0], RFRAME

Signal Acquisition in RIO16

The TMS805 RapidIO support takes advantage of the two-way demux feature of the logic analyzer hardware to acquire the RapidIO bus and create a perfectly aligned 32-bit bus word per logic analyzer sample.

When combined, the 16-bit Tx and Rx RapidIO buses contain eight unique pumps of data per transaction. The bus defines a unique clock edge for each pump of data as well (four clocks with two edges each). However, the module hardware can only clock based on one of the four clock domains (the hardware cannot synchronize between two different clock domains). This support package uses TCLK0, TCLK1, RCLK0 or RCLK1 as source clock domain depending on the custom clocking options selected during combined clocking. Use RCLK0 or RCLK1 for the Rx Only clocking option and TCLK0 or TCLK1 for the Tx Only clocking option.

This allows the logic analyzer to detect two out of eight clock edges. The other six clock edges are not used.

Since only two clock edges can be used for latching data, you must define phase offsets from the source clock to pick up the remaining six data pumps. You can do this through the setup/hold user interface.

The support package provides default windows assuming 0 ps skew between the different clocks. Since the logic analyzer can detect both a rising and a falling edge, the clock period is not a variable in the offset equation.

***NOTE**. The support package assumes that the TCLK and RCLK domains are based on the same clock crystal to eliminate clock phase drift between the two clock domains. A static skew between the clock domains is acceptable, since you can calibrate to the skew.*

Figure 3-2 shows a bus timing diagram for the RIO16 support package.

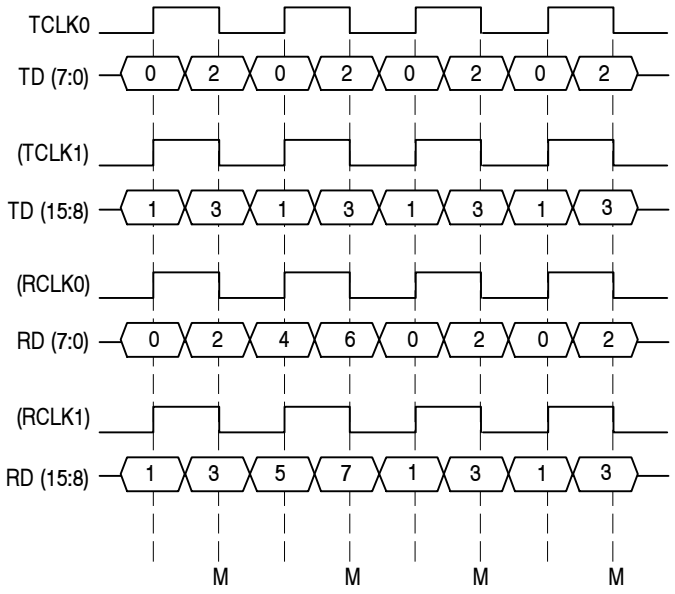


Figure 3-2: Bus timing diagram for the RIO16 support package

Table 3-56 shows the sample points in the RIO16 support package.

Table 3-56: Sample points in the RIO16 support

Master point	Signals
M	TCLK0, TD[7:0], TCLK1, TD[15:8], TFRAME, RCLK0, RD[7:0], RCLK1, RD[15:8], RFRAME

Signal Acquisition in RIO8_34

The TMS805 RapidIO support package takes advantage of the four-way demux feature of the logic analyzer hardware to acquire the RapidIO bus signals and create a perfectly aligned 32-bit bus word for each logic analyzer sample.

When combined, the 8-bit RapidIO buses contain four unique pumps of data per transaction. The bus defines a unique clock edge for each pump of data as well. This support package uses CLK0 as the source clock domain.

This allows the logic analyzer to detect two out of four clock edges. The other two clock edges are not used.

Since only two clock edges can be used for latching data, you must define phase offsets from CLK0 to pick up the remaining two data pumps. You can use AutoDeskew to adjust the Setup/Hold window. The support package provides default windows assuming 0 ps skew between the different clocks. Since the logic analyzer can detect both a rising and a falling edge, the clock period is not a variable in the offset equation.

Figure 3–3 shows a bus timing diagram for the RIO8_34 support package.

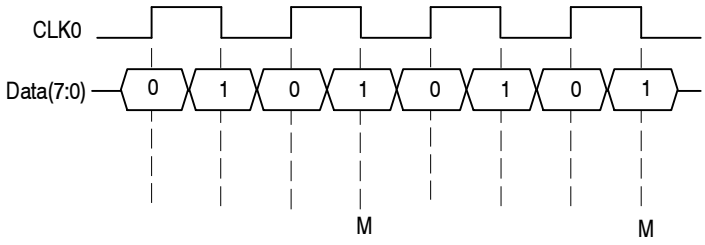


Figure 3-3: Bus timing diagram for the RIO8_34 support package

Table 3–57 shows the sample points in the RIO8_34 support package.

Table 3-57: Sample points in the RIO8_34 support

Master point	Signals
M	CLK0, Data[7:0], FRAME

Signal Acquisition in RIO16_34

The TMS805 RapidIO support takes advantage of the two-way demux feature of the logic analyzer hardware to acquire the RapidIO bus and create a perfectly aligned 32-bit bus word for each logic analyzer sample.

When combined, the 16-bit RapidIO buses contain four unique pumps of data per transaction. The bus defines a unique clock edge for each pump of data as well (two clocks with two edges each). This support package uses CLK1 as source clock domain.

Since only one clock edge can be used for latching data, you must define phase offsets from the source clock to pick up the remaining three data pumps. You can do this through the setup/hold user interface.

The support package provides default windows assuming 0 ps skew between the different clocks. Since the logic analyzer can detect both a rising and a falling edge, the clock period is not a variable in the offset equation.

Figure 3-4 shows a bus timing diagram for the RIO16_34 support package.

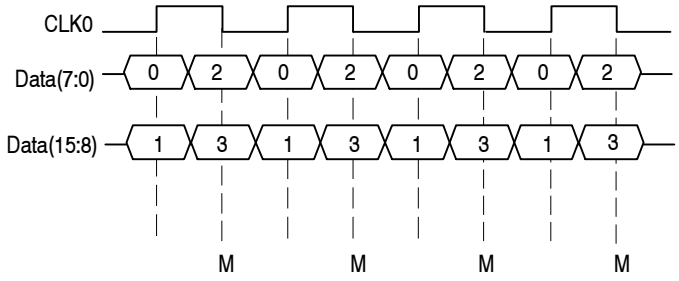


Figure 3-4: Bus timing diagram for the RIO16_34 support package

Table 3-58 shows the sample points in the RIO16_34 support package.

Table 3-58: Sample points in the RIO16_34 support

Master point	Signals
M	CLK1, Data[7:0], Data[15:8], FRAME

Specifications

Specifications

This section contains the specifications for the support package.

Specification Table

Table 4–1 lists the electrical requirements that the target system must produce for the support to acquire correct data.

Table 4-1: Electrical specifications

Characteristics	Requirements
Target system clock rate	
TMS805 specified clock rate for state acquisition supports for RIO8, RIO16, RIO8_34, and RIO16_34	Maximum 375 MHz[1]
TMS805 specified clock rate for timing only supports for RIO8_T and RIO16_T	Maximum 500 MHz
Minimum data valid window required for state acquisition (measured at threshold)	750 ps (typical)

1 **This is the specification at the time of printing. Contact your Tektronix representative for current information on the fastest bus supported.**

Index

Index

E

F

I

L

M

N

O

P

R

S

T

U

V

W